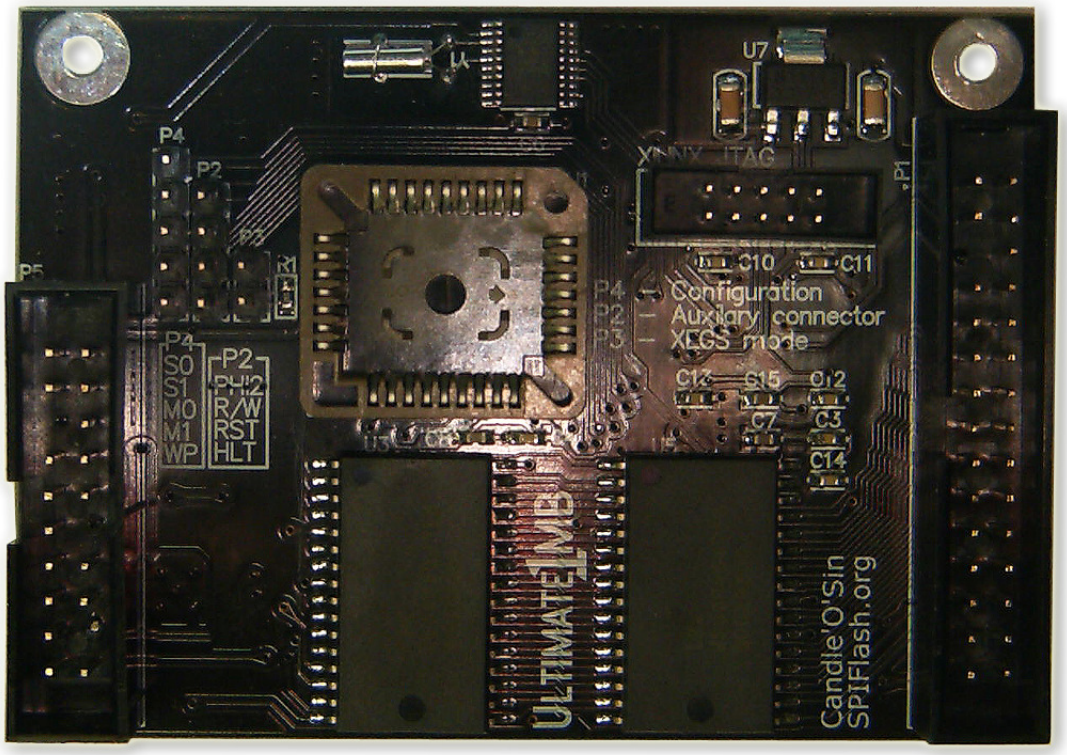
Ultimate1MB expansion features

Ultimate1MB expansion was designed with few things in my mind:

- to be as much solderless as possible (only RW, PHI2, HALT and RESET lines need soldering)
- fully flashable SpartaDOS-X with up to 320kbytes for its purposes
- RTC module for SDX with battery backup and NVRAM
- fully flashable 4 OS ROM slots
- hardware WRITE PROTECT for whole Flash array
- configurable memory expansion with 4 modes of operation:
    - disabled - no extra memory is visible to the system
    - 320k RAMBO - 256k of extra memory is visible both to CPU and ANTIC chips
    - 578k COMPY SHOP - 512k of extra memory is visible to CPU and ANTIC chip, bit 4 and 5 works in 130XE compatibility mode
    - 1088k RAMBO - 1MB of extra memory is visible to CPU and ANTIC chips
- customizable BASIC and MISSLE COMMAND slots (also flashable)
- BIOS to enable jumperless operation and configuration for the board, plus some means of controling external hardware (VBXE, SimpleStereo, or any other hardware that takes binary signals for configuration)



How it works?

Since solderless approach was the main driving force behind this, some portions of PIA and GTIA chips had to be simulated within the CPLD chip.

When PORTB write is detected, hardware checks if internal shadow of PBCTL (D303) allows writes, and if so, value from Data bus is written to PORTB shadow. In the parallel, last value of PORTB shadow registers is stored into internal MMU CONTROL register to preserve current status of system rom, basic, self-test and missle command rom chips mappings, thus allowing flowless acces to whole extended memory array.

Since there is internal SDX module care had to be taken for GTIA TRIG3 register.

Normally RD5 line from cartridge port is connected both to MMU chip and GTIA TRIG3 lines and since the goal was to incorporate this extension without the need of cutting any traces on motherboard, this register had to be shadowed (OS checks for TRIG3 status on every NMI, if there is a change on state of this line, OS assumes that cartridge was put in/removed and to prevent failures goes into endless loop).
With this shadow of TRIG3 register system can be fooled, and enabling or disabling "external" (to SDX module) cartridges can be done.

Lastly, there is configuration register which is used for configuring the extension according to configuration data stored in NVRAM - user can choose which OS ROM should be booted on power-on, what memory size machine should have and if SDX and RTC modules should be enabled.

Every time RESET button is pressed, Ultimate1MB BIOS kicks in, and checks if HELP key is pressed. If so, then interactive menu pops up, enabling user to change current configuration. Otherwise, checksum is calculated from the bytes read from NVRAM, if this matches checksum read from NVRAM, then configuration is assumed as valid one, and written into configuration registers. Then normal boot follows.

Registers description

D301 PORTBS (WO)

Bits are mapped according to Atari mappings

D303 PBCTLS (WO)

Bit 2 - if set to zero, PORTB writes are disabled

D380 UCTL (WO)

Bits 1-0 - Memory expansion configuration mode

- 00 - Memory disabled
- 01 - 320k RAMBO
- 10 - 576k COMPY SHOP
- 11 - 1088K RAMBO

Bits 3-2 - System Select

- 00 - ROM Slot 1
- 01 - ROM Slot 2
- 10 - ROM Slot 3
- 11 - ROM Slot 4

Bit 4 - SDX disable, when set, SDX module is disabled

Bit 5 - reserved, should be written 0

Bit 6 - IO_RAM - enables (1) or disables (0) RAM in D600-D7FF address space. Used internally by BIOS code.

Bit 7 - CONFIG_L - configuration LOCK, when set, data in UCTL cannot be altered. At RESET this bit is set to 0 enabling BIOS code to alter configuration

D381 UAUX (WO)

Bit 0 - Controls pin M0 of P4 connector, BIOS default is SimpleStereo Enable/Disable

Bit 1 - Controls pin M1 of P4 connector, BIOS default is COVOX Enable/Disable

Bit 2 - Controls pin S0 of P4 connector

Bit 3 - Controls pin S1 of P4 connector

Bit 4 - when 0, WP Pin of P4 connector becomes D6xx signal for VBXE, when 1 D7xx

Bit 5 - when 0, VBXE decoder logic at pin WP is enabled, when 1 - Disabled

D381 UCOLDF (RW)

Bits 0-6 reserved, will read 0

Bit 7 - COLDF - 1 at power on, BIOS check this flag to see if Atari was just powered on, then writes 0.

All writes to Ultimate1MB registers are only possible when bit 7 of UCTL (CONFIG_L) is 0.

SDX Registers

D5E0 BANKNO (WO)

Bits 5-0	Bank number. Banks 0-53 are valid for SDX module. Bank 54 is BASIC ROM, bank 55 is MISSLE COMMAND or any other 8k game ROM image, banks 56-63 are for OS ROM slots. Access to all banks is provided through this port for flashing purposes
Bits 7-6	Reserved for future use, should be wrtitten 0

D5E1 SDXCTL (WO)

Bit 0	External Cartridge. When set, and Bit 1 is set, external cartridge is OFF, SDX is OFF When reset, and bit 1 is set, external cardridge is ON, SDX is OFF
Bit 1	SDX Enable. When set, SDX is ON, External cartridge is always OFF
Bits 7-2	Reserved for future use, should be written 0

D3E2 RTCOUT (W)

Bit 0	Chip Enable
Bit 1	SPI Clock
Bit 2	SPI MOSI (Master Out, Slave In)
Bits 7-3	Reserved

D3E2 RTCIN (R)

Bit 0-2	Reserved
Bit 3	SPI MISO (Master In, Slave Out)
Bit 7-4	Reserved

Ultimate1MB FLASH Chip Memory Map

0x000000-0x04FFFF	SDX
0x050000-0x053FFF	BIOS code space
0x054000-0x05FFFF	reserved
0x060000-0x061FFF	BASIC
0x062000-0x063FFF	8k GAME cartridge
0x064000-0x06FFFF	reserved
0x070000-0x073FFF	1st OS slot
0x074000-0x077FFF	2nd OS slot
0x078000-0x07BFFF	3rd OS slot
0x07C000-0x07FFFF	4th OS slot