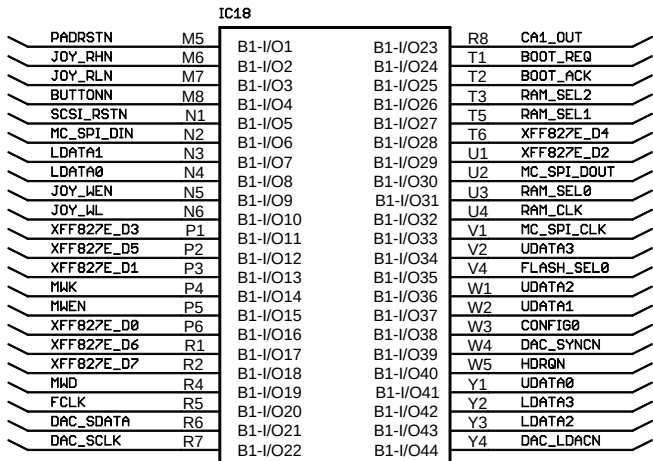
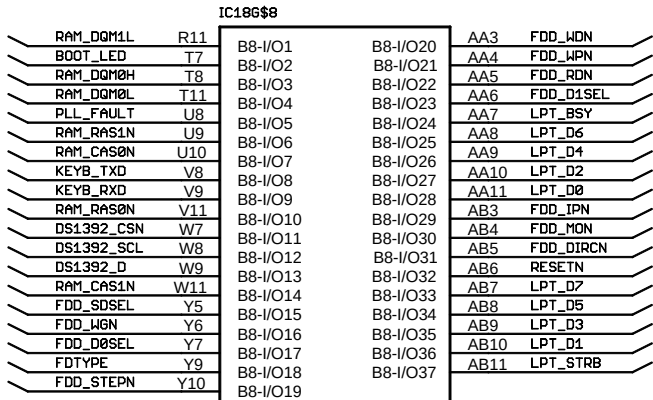
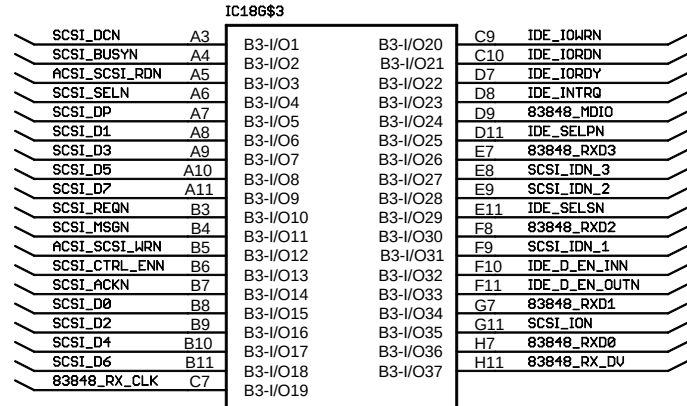




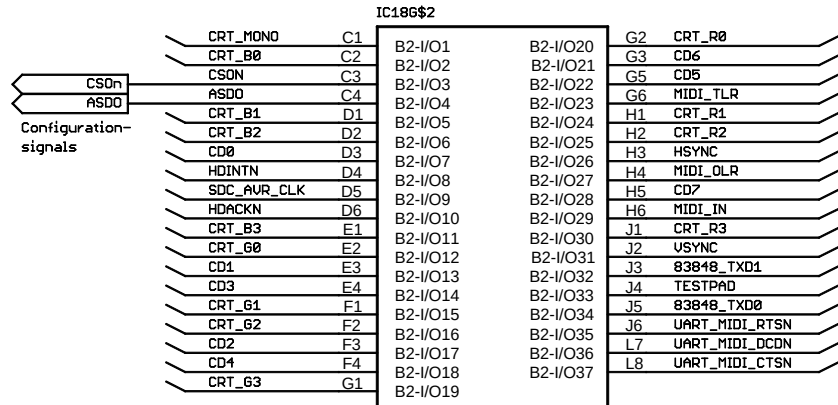
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experiment-S - Wolfgang Foerster

FPGA (part1)

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IC186\$4			
ADR15	A13	B4-I/O1	B4-I/O18
ADR13	A14	B4-I/O2	B4-I/O19
ADR11	A15	B4-I/O3	B4-I/O20
ADR9	A16	B4-I/O4	B4-I/O21
ADR7	A17	B4-I/O5	B4-I/O22
ADR5	A18	B4-I/O6	B4-I/O23
ADR3	A19	B4-I/O7	B4-I/O24
ADR1	A20	B4-I/O8	B4-I/O25
ADR16	B13	B4-I/O9	B4-I/O26
ADR14	B14	B4-I/O10	B4-I/O27
ADR12	B15	B4-I/O11	B4-I/O28
ADR10	B16	B4-I/O12	B4-I/O29
ADR8	B17	B4-I/O13	B4-I/O30
ADR6	B18	B4-I/O14	B4-I/O31
ADR4	B19	B4-I/O15	B4-I/O32
ADR2	B20	B4-I/O16	B4-I/O33
ADR17	C13	B4-I/O17	B4-I/O34

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IC186\$6			
LFS	M15	B6-I/O1	B6-I/O21
LLCLK	M16	B6-I/O2	B6-I/O22
CLK_AUX	M18	B6-I/O3	B6-I/O23
CODEC_SSYNC	M19	B6-I/O4	B6-I/O24
UDCLK	N15	B6-I/O5	B6-I/O25
RWN	N21	B6-I/O6	B6-I/O26
BERRN	N22	B6-I/O7	B6-I/O27
SDC_AVR_D7	P15	B6-I/O8	B6-I/O28
SDC_AVR_D6	P17	B6-I/O9	B6-I/O29
SDC_AVR_D5	P18	B6-I/O10	B6-I/O30
SDC_AVR_D4	P19	B6-I/O11	B6-I/O31
SDC_AVR_D3	P20	B6-I/O12	B6-I/O32
UDSN	P21	B6-I/O13	B6-I/O33
LDSN	P22	B6-I/O14	B6-I/O34
SDC_AVR_D2	R17	B6-I/O15	B6-I/O35
SDC_AVR_D1	R18	B6-I/O16	B6-I/O36
SDC_AVR_D0	R19	B6-I/O17	B6-I/O37
HDCSN	R20	B6-I/O18	B6-I/O38
HALTN	R21	B6-I/O19	B6-I/O39
ASN	R22	B6-I/O20	

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IC186\$5			
3421_MOSI	C19	B5-I/O1	B5-I/O22
83848_TX_EN	C20	B5-I/O2	B5-I/O23
DATA1	C21	B5-I/O3	B5-I/O24
DATA0	C22	B5-I/O4	B5-I/O25
3421_MISO	D19	B5-I/O5	B5-I/O26
83848_TXD2	D20	B5-I/O6	B5-I/O27
DATA3	D21	B5-I/O7	B5-I/O28
DATA2	D22	B5-I/O8	B5-I/O29
3421_SCLK	E18	B5-I/O9	B5-I/O30
3421_SS_	E19	B5-I/O10	B5-I/O31
83848_TXD3	E20	B5-I/O11	B5-I/O32
DATA5	E21	B5-I/O12	B5-I/O33
DATA4	E22	B5-I/O13	B5-I/O34
83848_MDC	F20	B5-I/O14	B5-I/O35
DATA7	F21	B5-I/O15	B5-I/O36
DATA6	F22	B5-I/O16	B5-I/O37
CODEC_SCLK	G17	B5-I/O17	B5-I/O38
CODEC_SDIN	G18	B5-I/O18	B5-I/O39
3421_INT	G20	B5-I/O19	B5-I/O40
DATA9	G21	B5-I/O20	B5-I/O41
DATA8	G22	B5-I/O21	B5-I/O42

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IC186\$7			
RAM_BA0	R14	B7-I/O1	B7-I/O18
RAM_ADR3	R15	B7-I/O2	B7-I/O19
RAM_ADR2	R16	B7-I/O3	B7-I/O20
RAM_ADR1	T16	B7-I/O4	B7-I/O21
RAM_D1	U13	B7-I/O5	B7-I/O22
RAM_WEN	U14	B7-I/O6	B7-I/O23
RAM_DQM1H	U15	B7-I/O7	B7-I/O24
RAM_BA1	V14	B7-I/O8	B7-I/O25
RAM_ADR0	V15	B7-I/O9	B7-I/O26
RAM_ADR10	W14	B7-I/O10	B7-I/O27
RAM_D4	W15	B7-I/O11	B7-I/O28
RAM_D5	W16	B7-I/O12	B7-I/O29
RAM_D2	Y13	B7-I/O13	B7-I/O30
RAM_D3	Y14	B7-I/O14	B7-I/O31
RAM_D6	Y16	B7-I/O15	B7-I/O32
RAM_D7	Y17	B7-I/O16	B7-I/O33
RAM_D0	AA12	B7-I/O17	B7-I/O34

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FPGA (part 2)

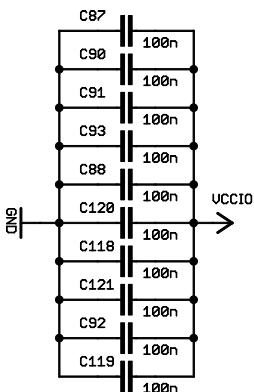
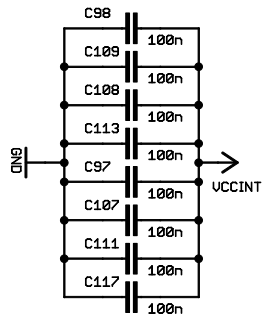
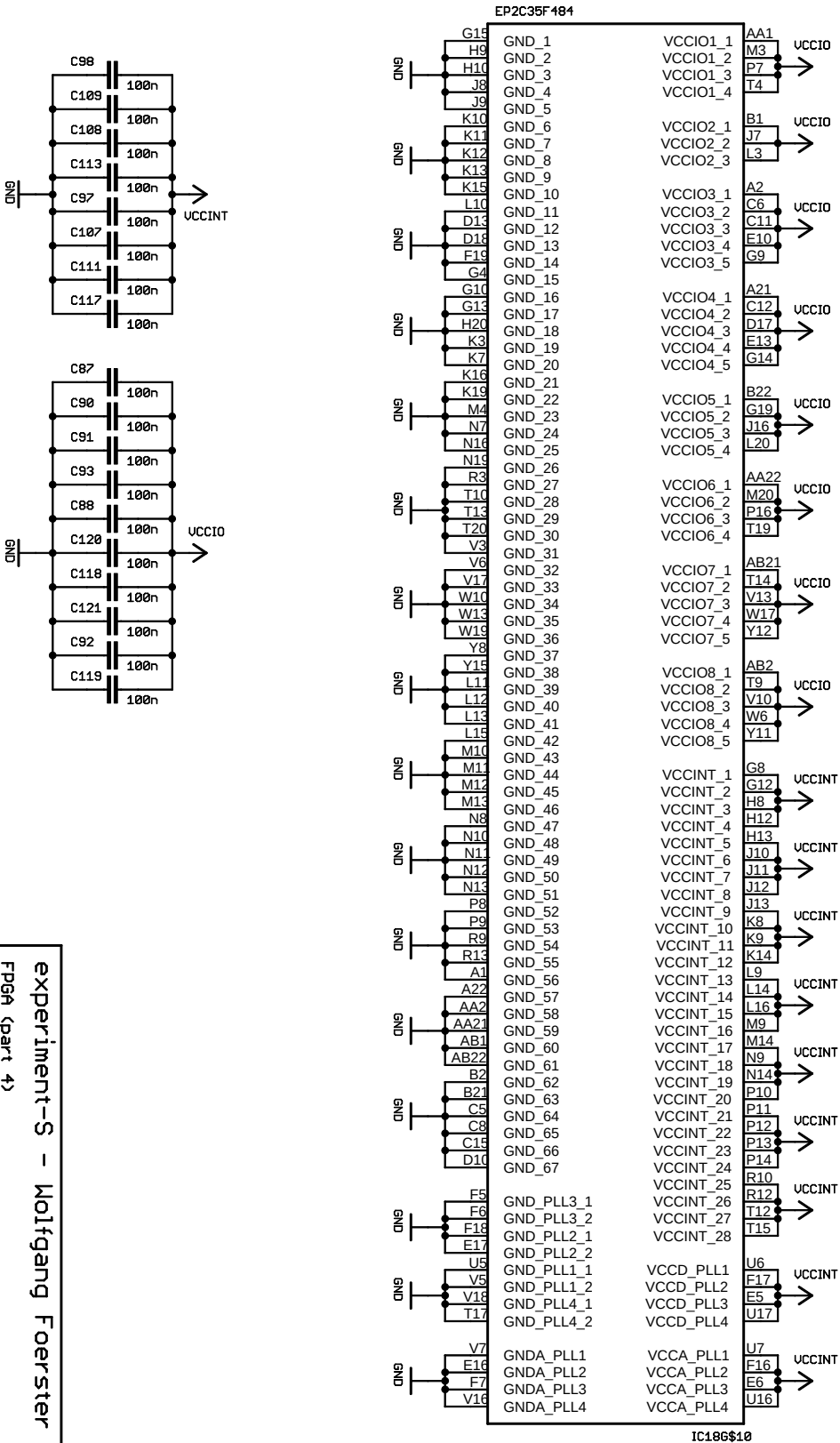
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FPGA (part 4)

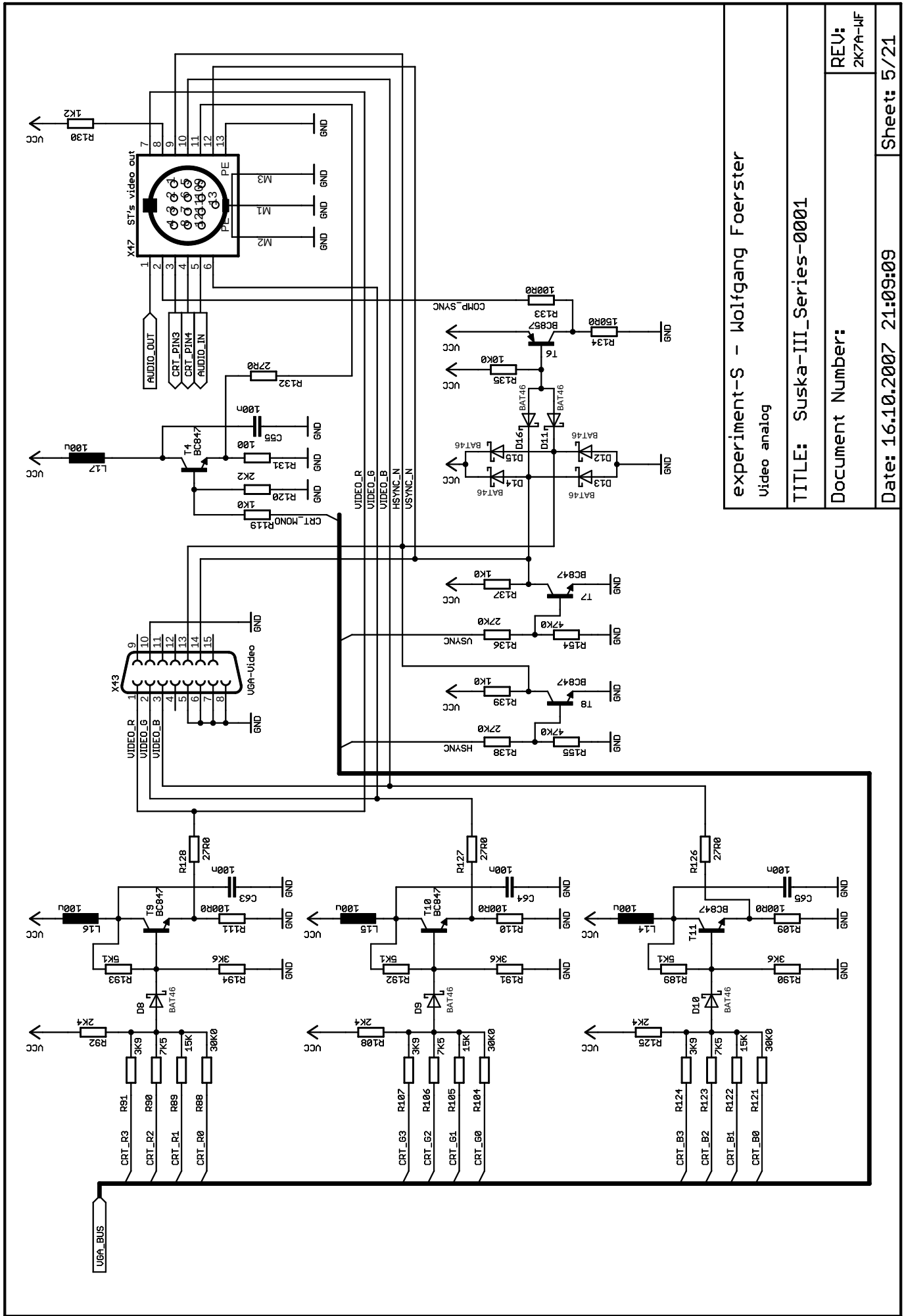
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Video analog

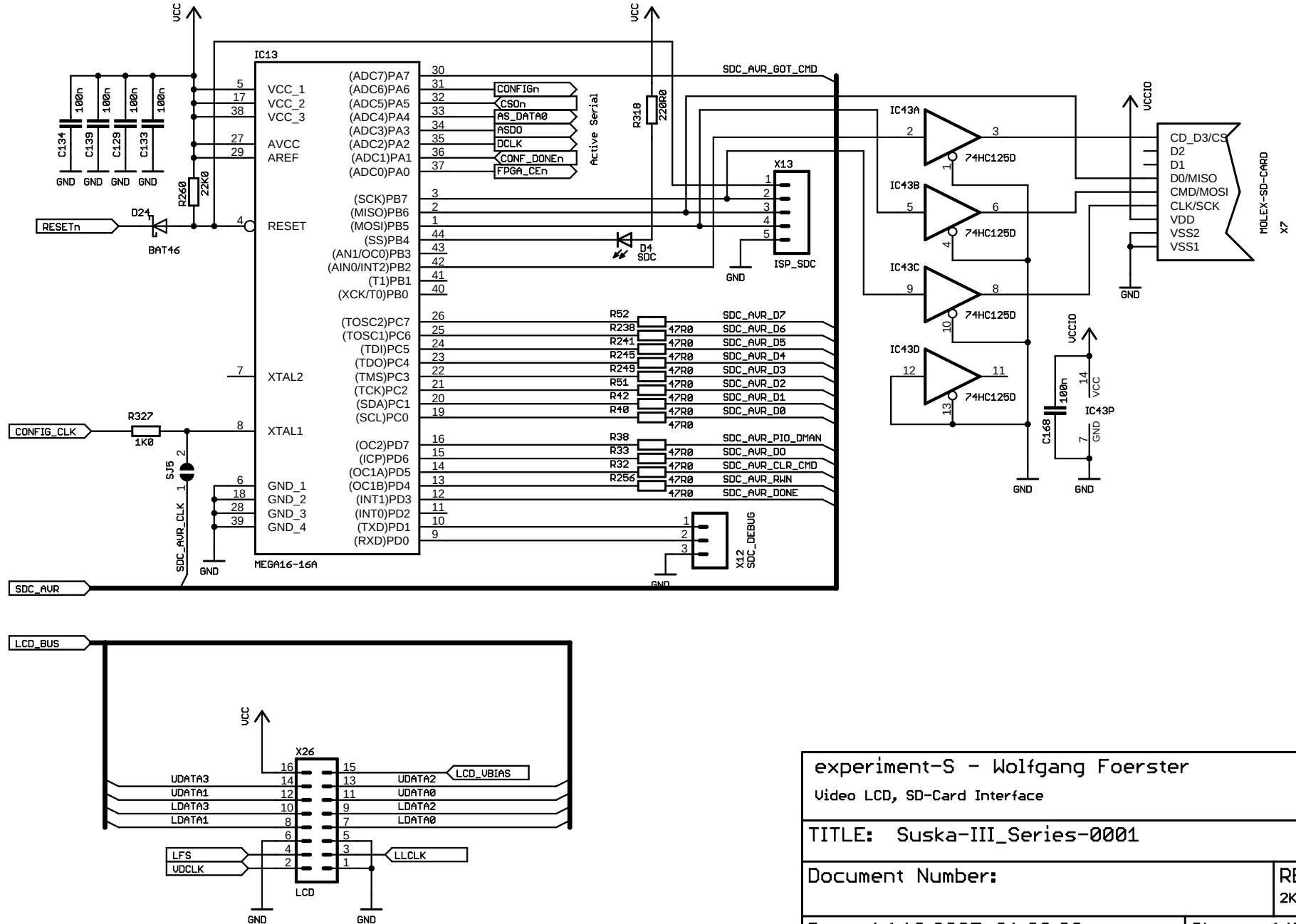
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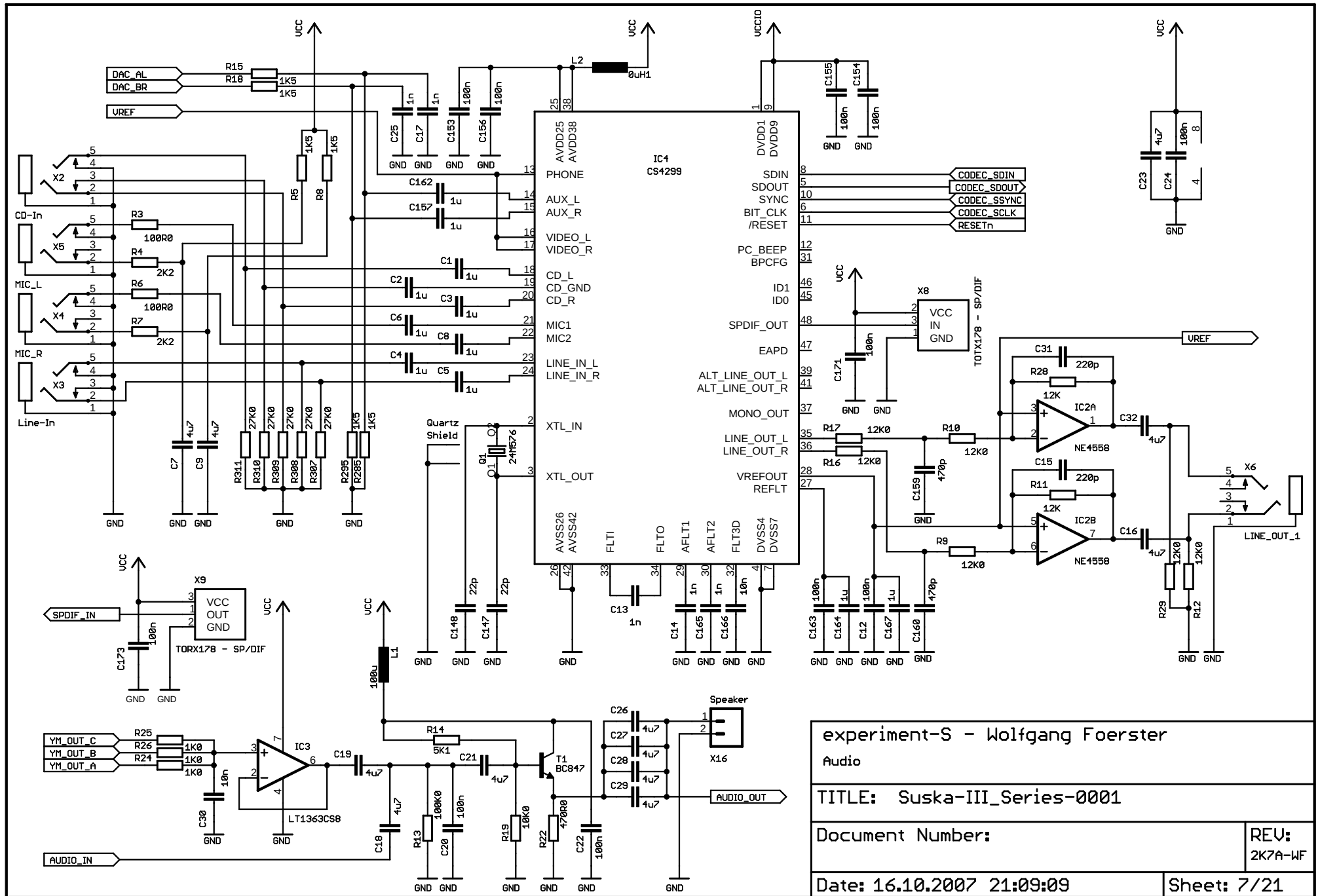
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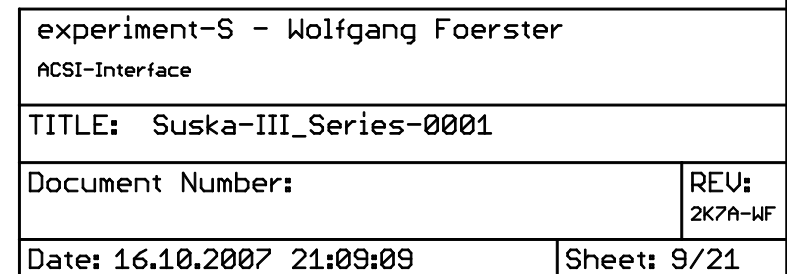
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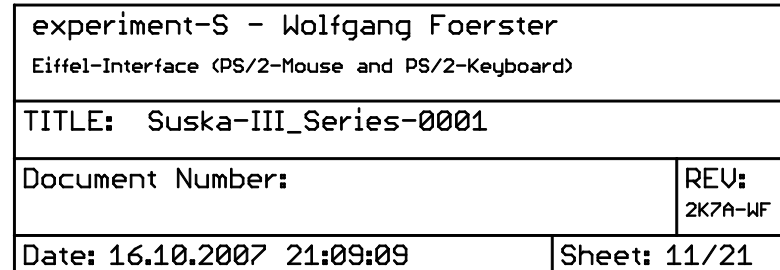
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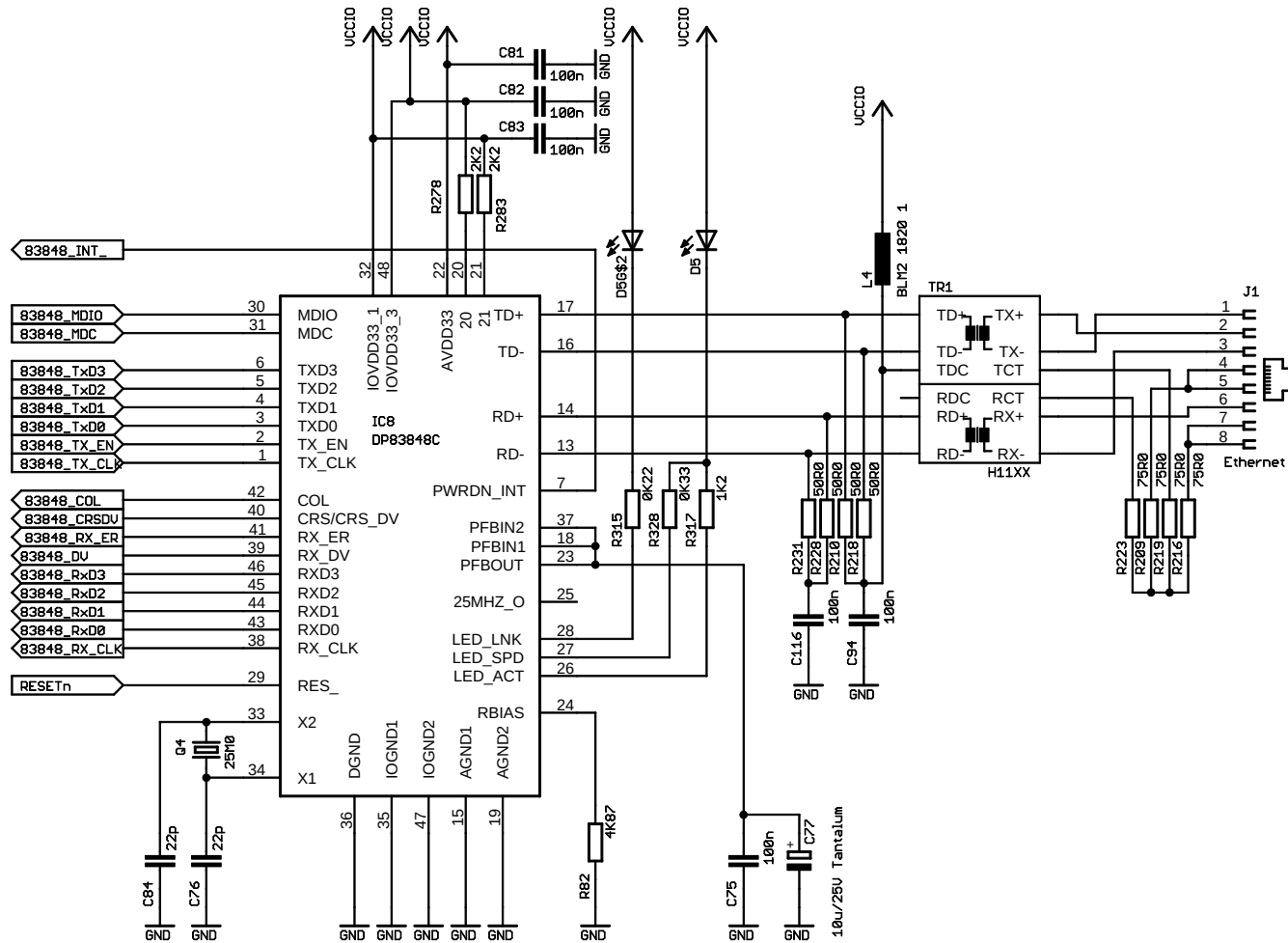


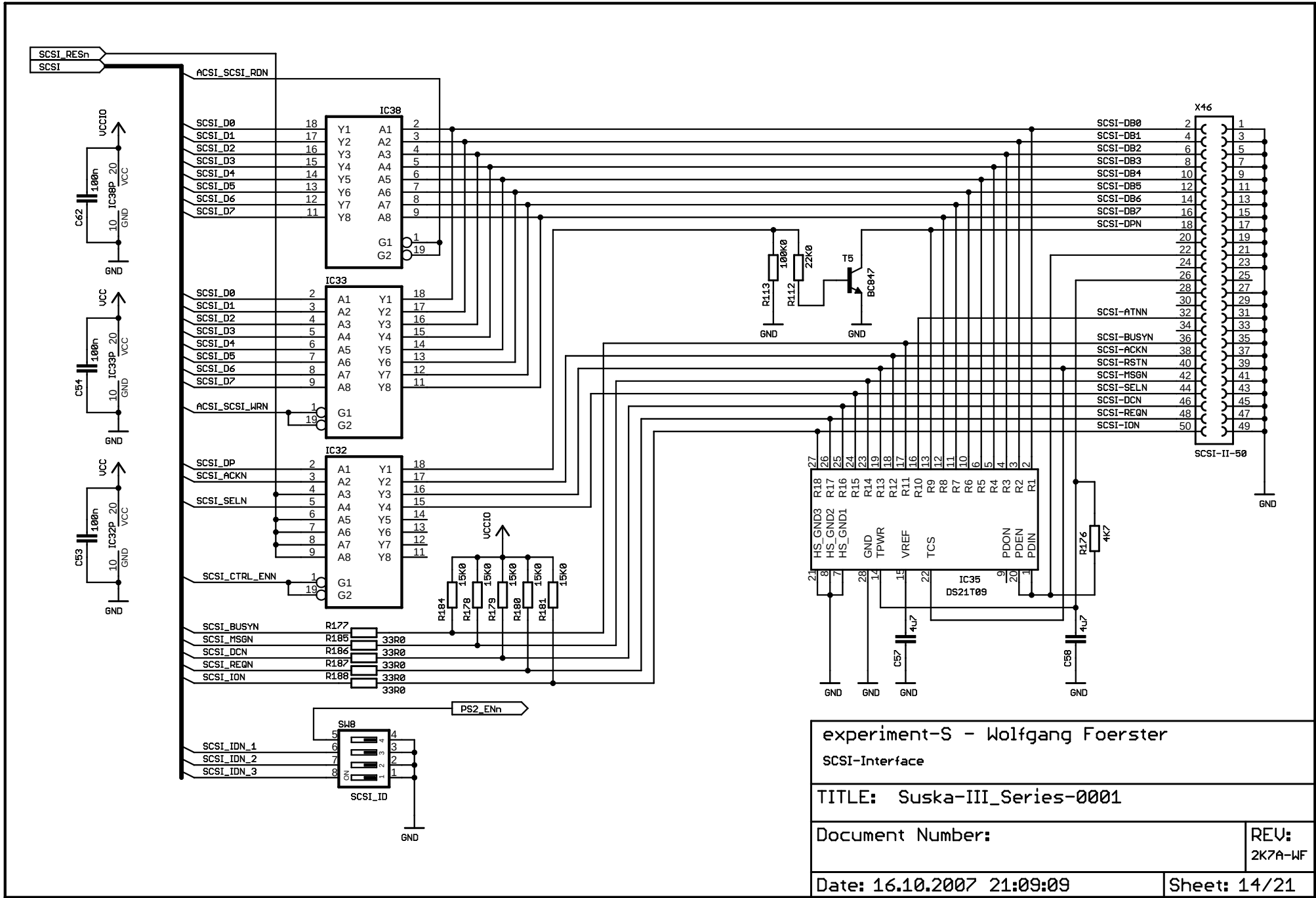
experiment-S - Wolfgang Foerster	
Video LCD, SD-Card Interface	
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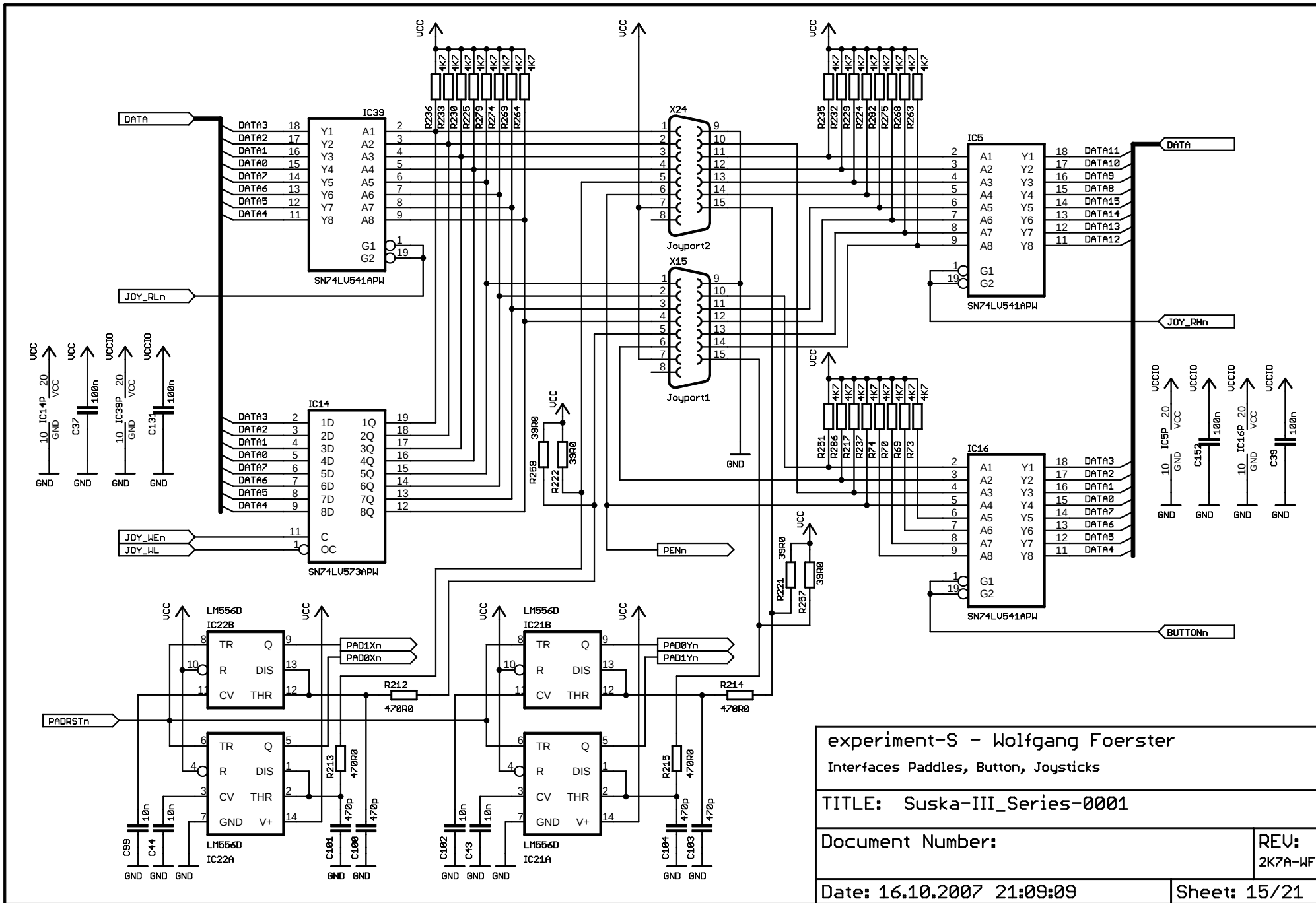


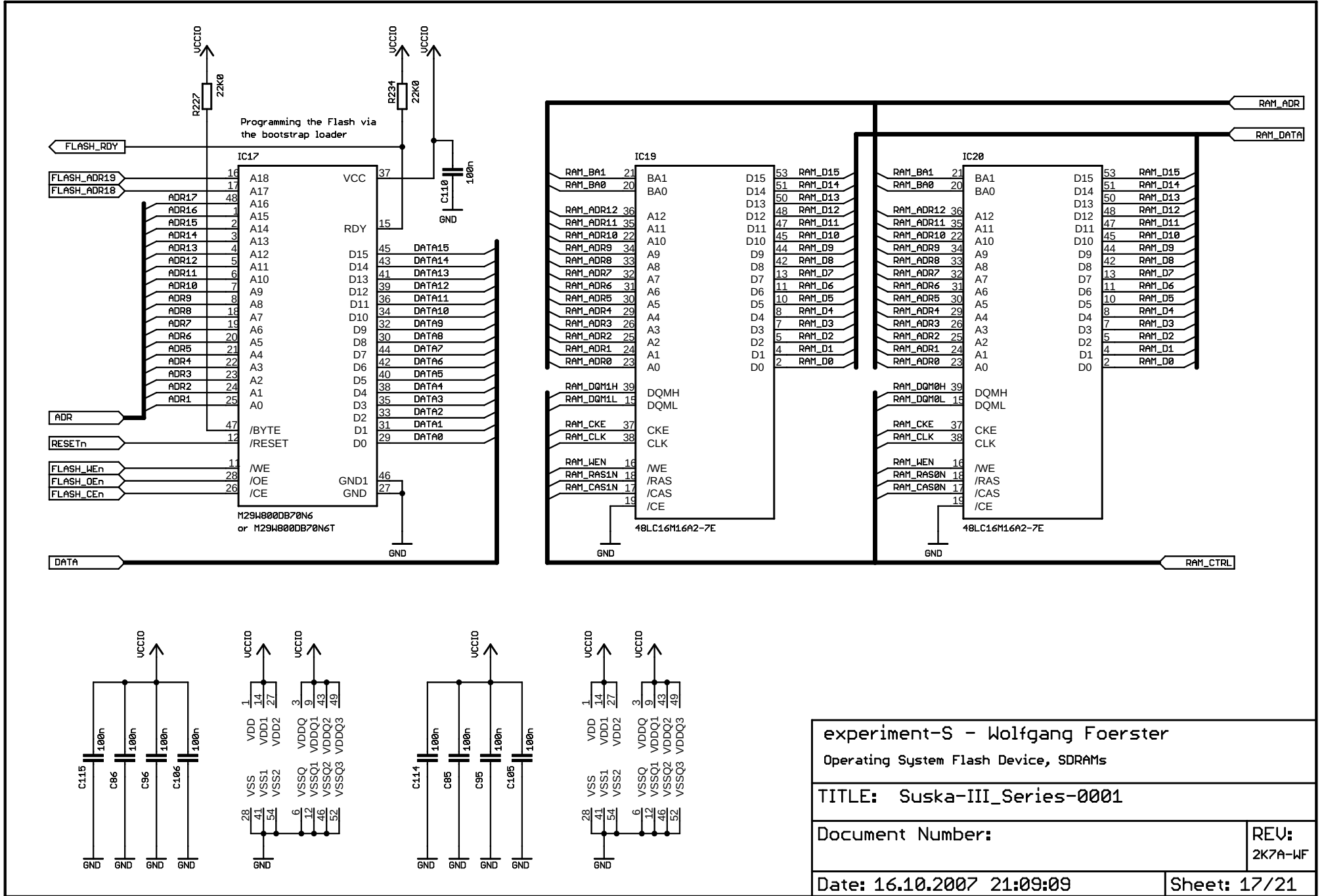










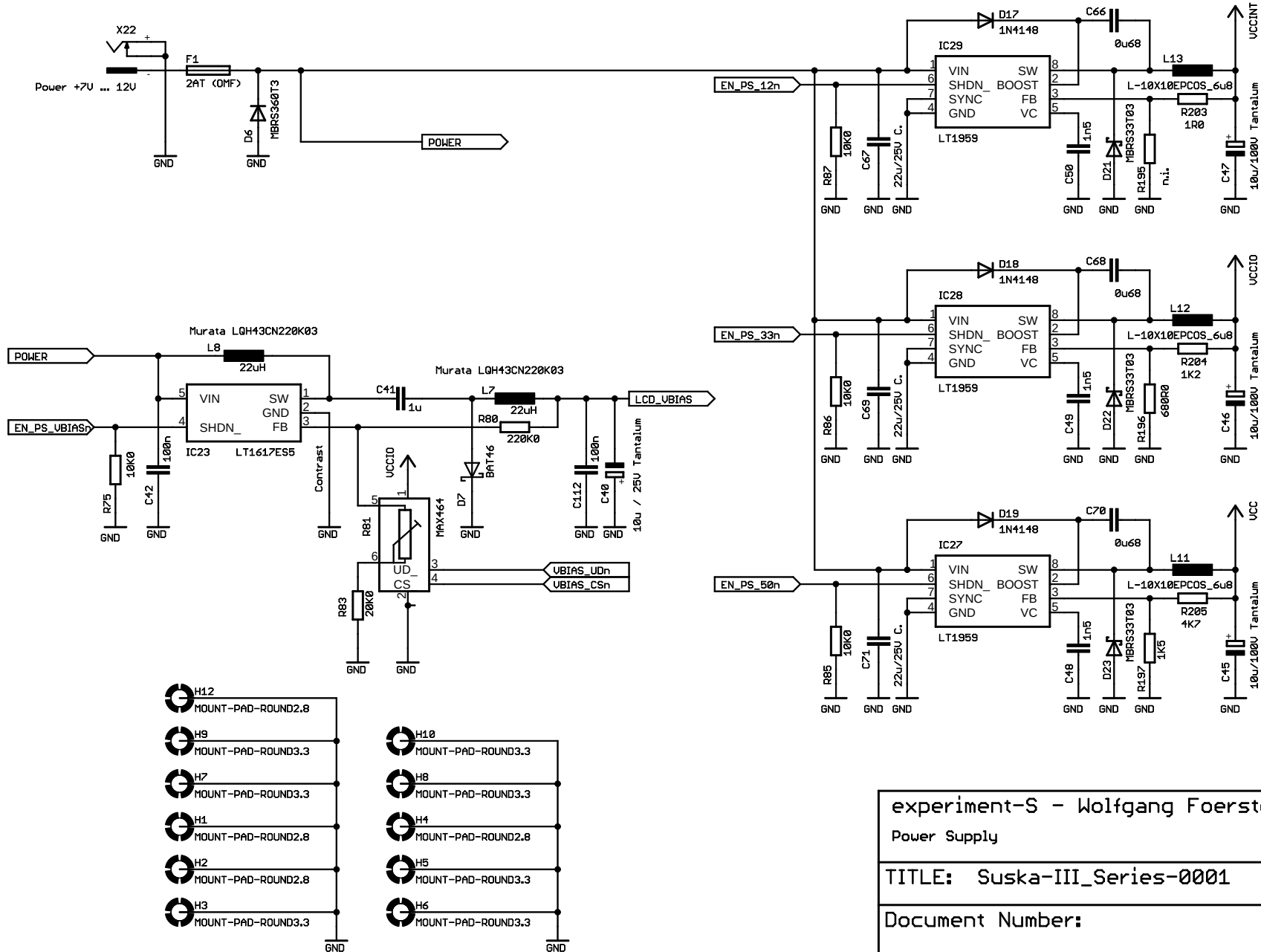


experiment-S - Wolfgang Foerster	
Operating System Flash Device, SDRAMs	
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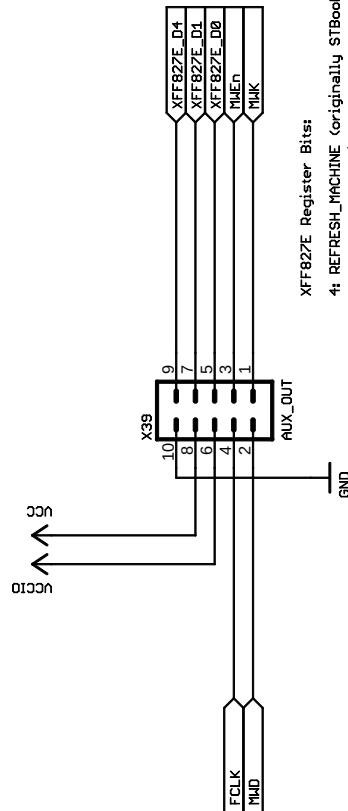
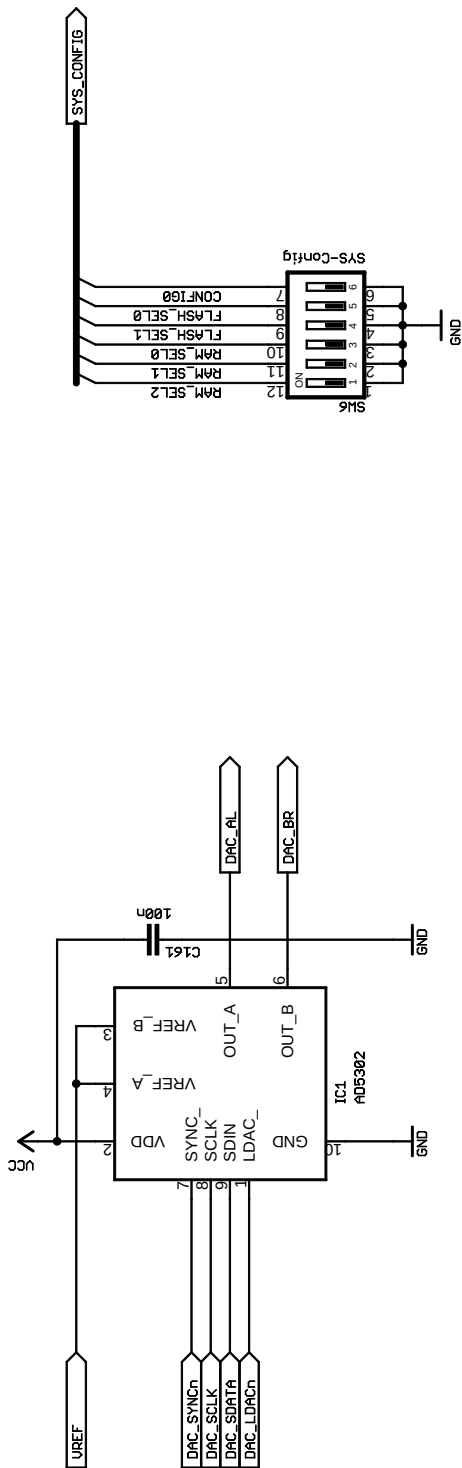


XFF827E Register Bits:

- 7: MTR_POWER_ON (Turns on IDE drive motor).
- 6: Not further specified.
- 5: RS232_OFF.
- 3: LAMP (LCD backlight, STBook).
- 2: POWER_OFF



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Power Supply	
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Audio-DA-Converter, Spares

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