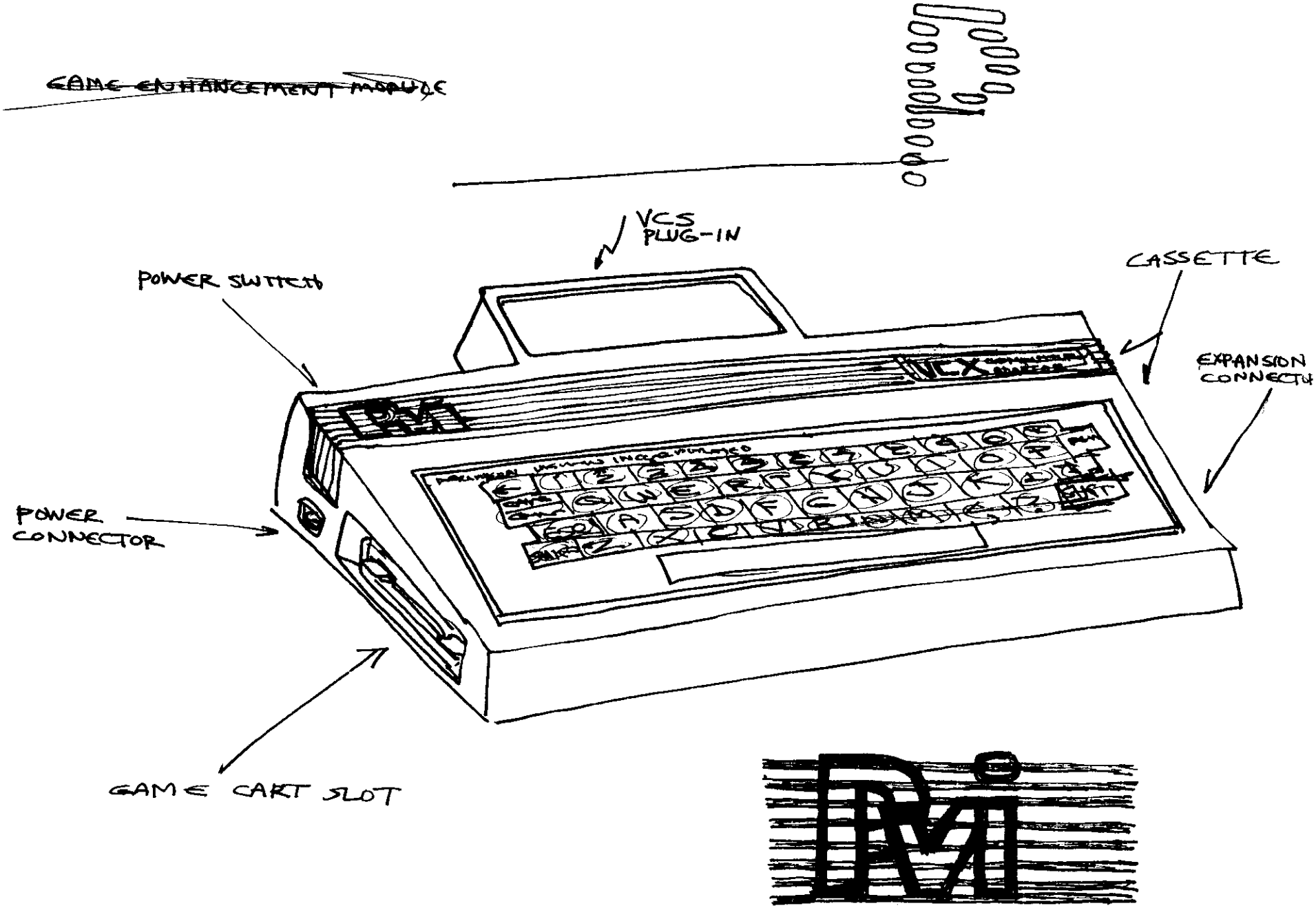
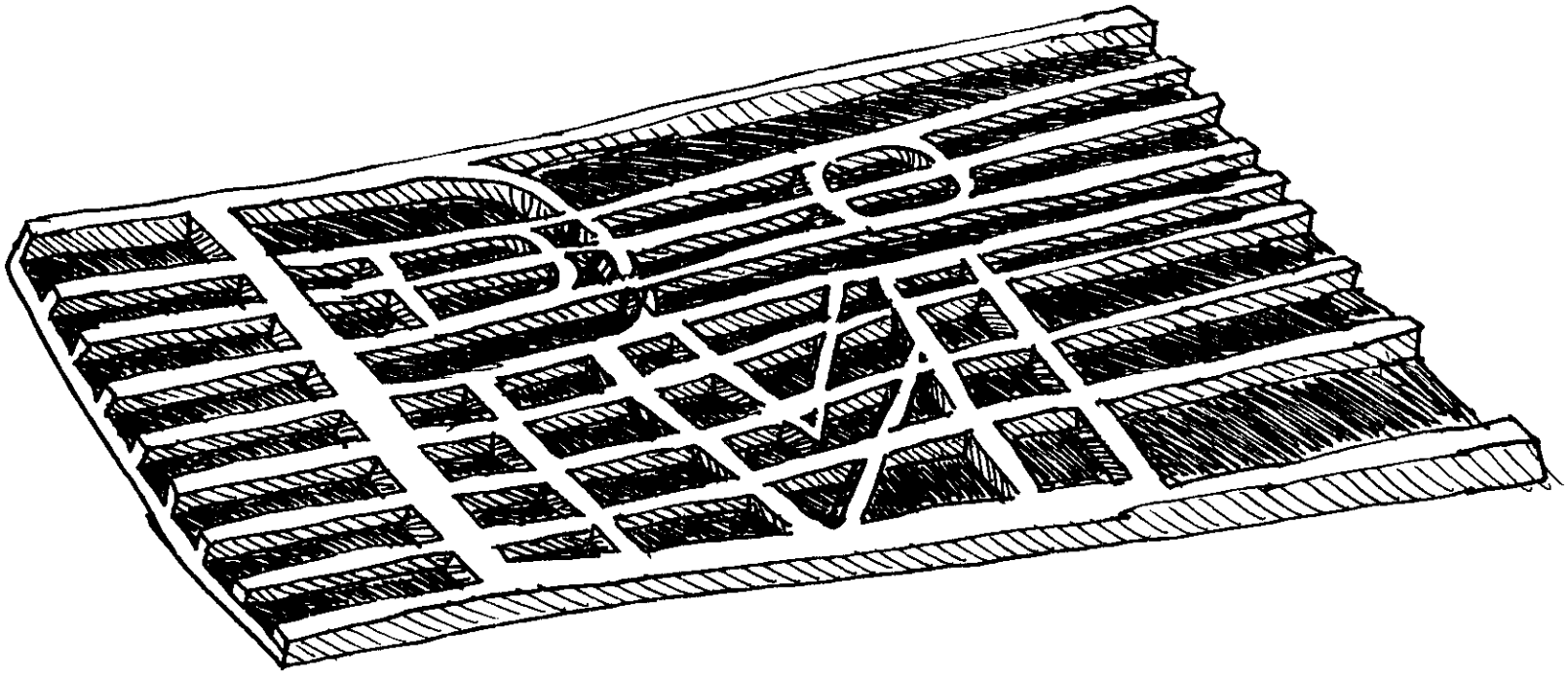
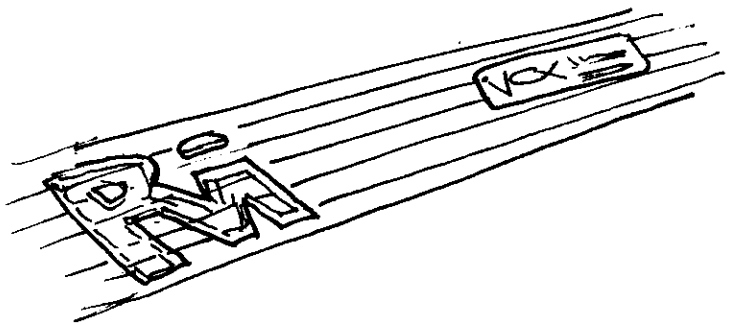
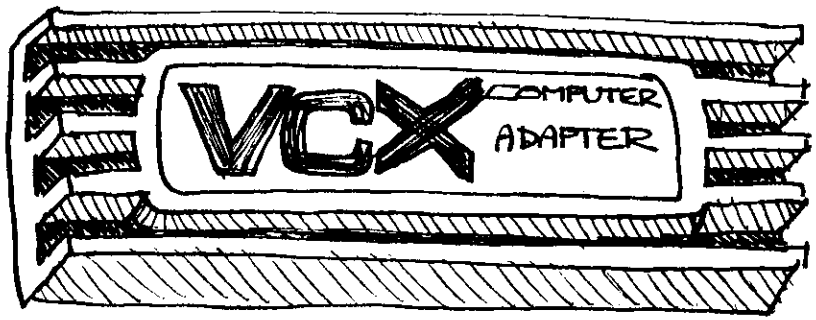
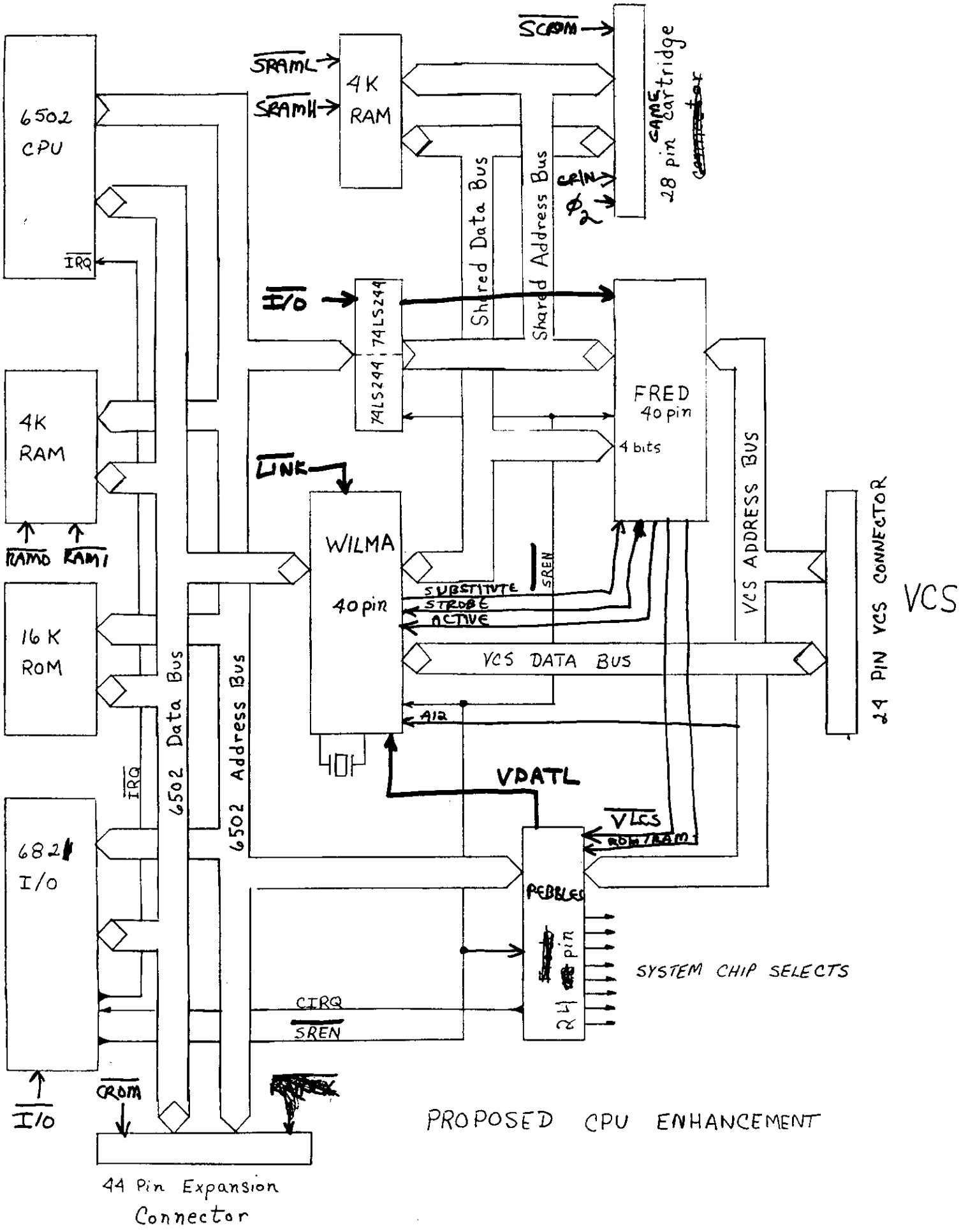
~~GAME ENHANCEMENT MODULE~~






VCX


VCX
COMPUTER
ADAPTER



PROPOSED CPU ENHANCEMENT

The Enhanced Graphics Instruction Set.

1. STA Immediate

WILMA HAS TO REMEMBER THAT CHAIN IS ON/OFF

1ST BYTE	0 0 T T T T T T	unchained
	0 1 T T T T T T	chained →
2ND BYTE	D D D D D D D D	Data

2. Load/Operate Immediate Indirect

1st Byte	1 0 0 c c c/p p p (OP CODE TO SUBS)	unchained
	1 0 1 c c c/p p p	chained
2ND Byte	x x x x x x x x	dummy data

3. STA Indirect

1ST Byte 1 1 T T T T T T

2ND Byte

0 0 0 x x p p p

0 0 1 x x p p p

0 1 0 x x p p p

● 1 1 x x p p p

1 0 0 x x p p p

1 0 1 x x p p p

1 1 0 x x p p p

1 1 1 x x p p p

bit 7 = TRANSPOSE

bit 6 = nibble swap

bit 5 = chain

c = substitute opcode

p = pointer

D = DATA

T = TIA ADDRESS

The Enhanced Graphics Instruction Set

1. STA Immediate **TIA+$40**

1ST BYTE	0 0 T T T T T T	UNchained
	0 1 T T T T T T	chained →
2ND BYTE	D D D D D D D D	Data

2. Load/Operate Immediate Indirect

1ST Byte	1 0 0 c c q/p p p	unchained
	1 0 1 c c q/p p p	chained
2ND Byte	x x x x x x x x	dummy data

3. STA Indirect

1ST Byte 1 1 T T T T T T

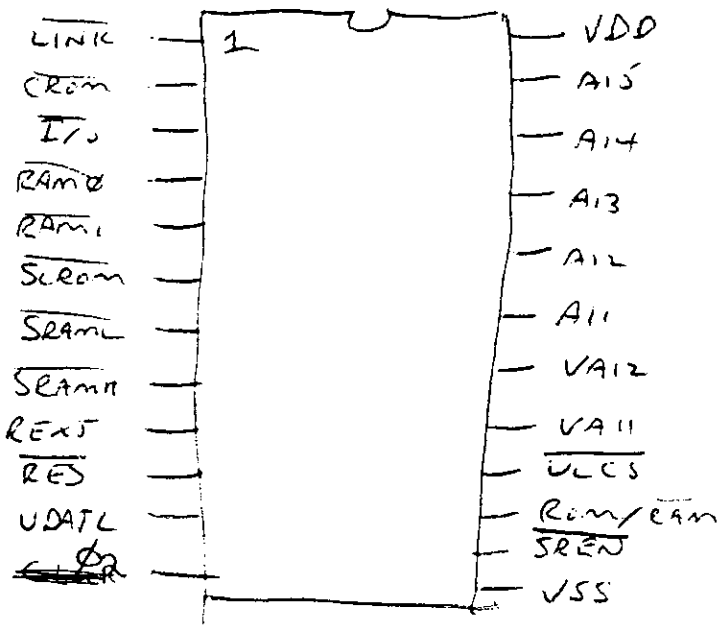
2ND Byte

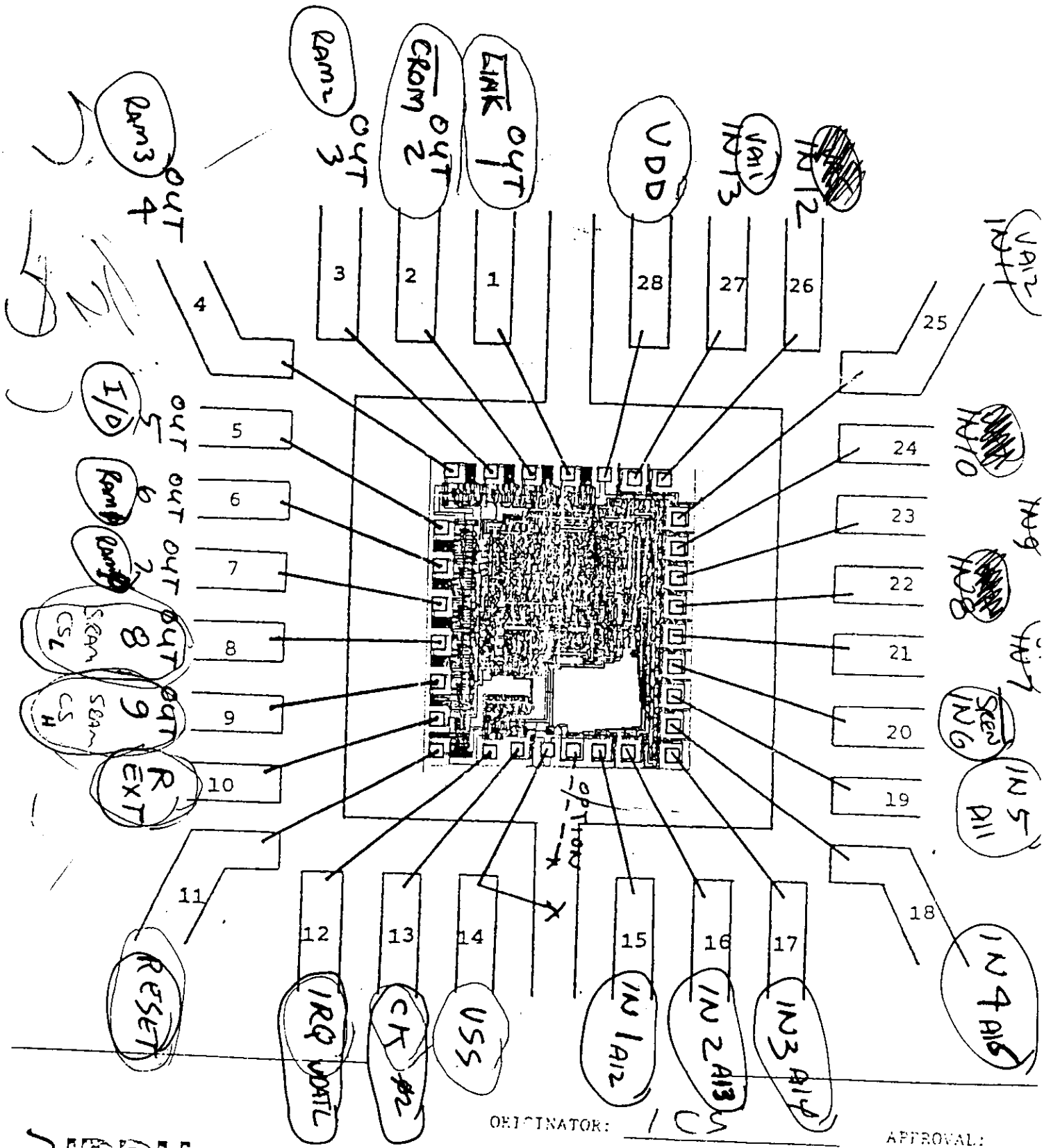
0 0 0 x x p p p	
0 0 1 x x p p p	
0 1 0 x x p p p	
● 1 1 x x p p p	
1 0 0 x x p p p	
1 0 1 x x p p p	
1 1 0 x x p p p	
1 1 1 x x p p p	

bit 7 = TRANSPOSE
bit 6 = nibble swap
bit 5 = chain

c = substitute opcode
p = pointer
D = DATA
T = TIA ADDRESS

Pebbles


LINK
CROM
I/O
RAM0
RAM1
SCROM
SRAML
SRAMH
REXT
RES
UDATL
1
VDD
A15
A14
A13
A12
A11
VA12
VA11
UCCS
ROM/RAM
SREN
VSS



SCALE: 20X

ORIGINATOR: [illegible]

CUSTOMER: PVI

DEVICE TYPE:

PACKAGE TYPE: 28 Leads Plastic

DIE SIZE: 118 X 101 ~

PAD SIZE: 150 X 150

APPROVAL:

ENG:

OP :

QA :

EFF DATE: 1/5/

THIS [illegible] BONDING DIAGRAM

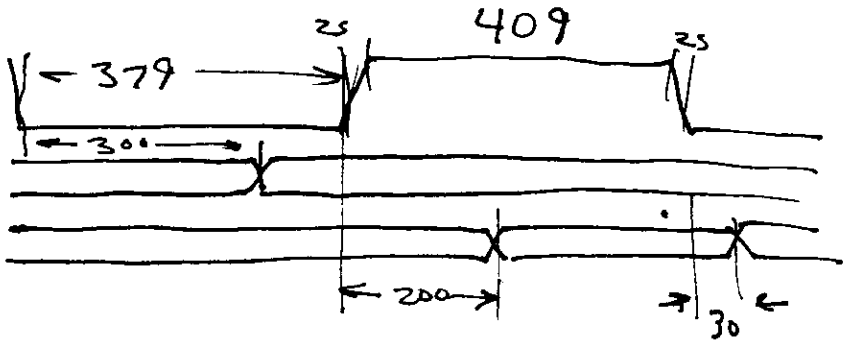
NO. _____ FORMS A PART OF

[illegible] AND WILL BE USED

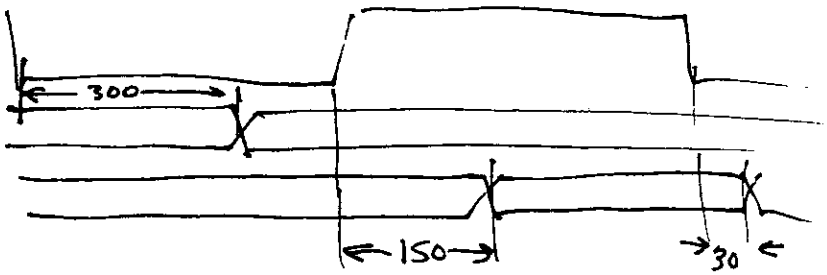
IN PLACE OF [illegible] P/O NO. _____

IEI FORM 0220-1331

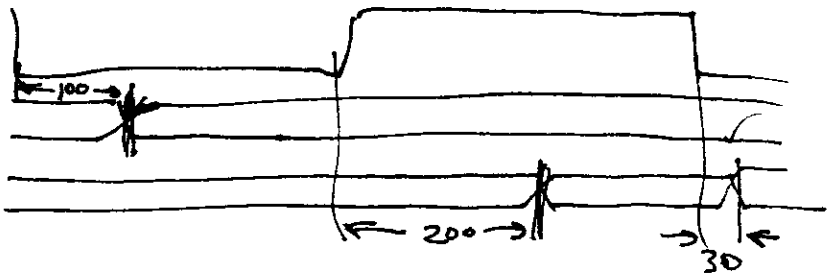
MAX CLOCK
MAX ADDR SETUP
MAX DATA SETUP



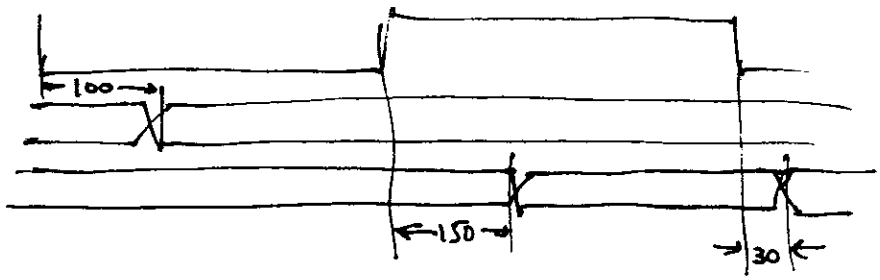
MAX CLOCK
MAX ADDR
TYP DATA



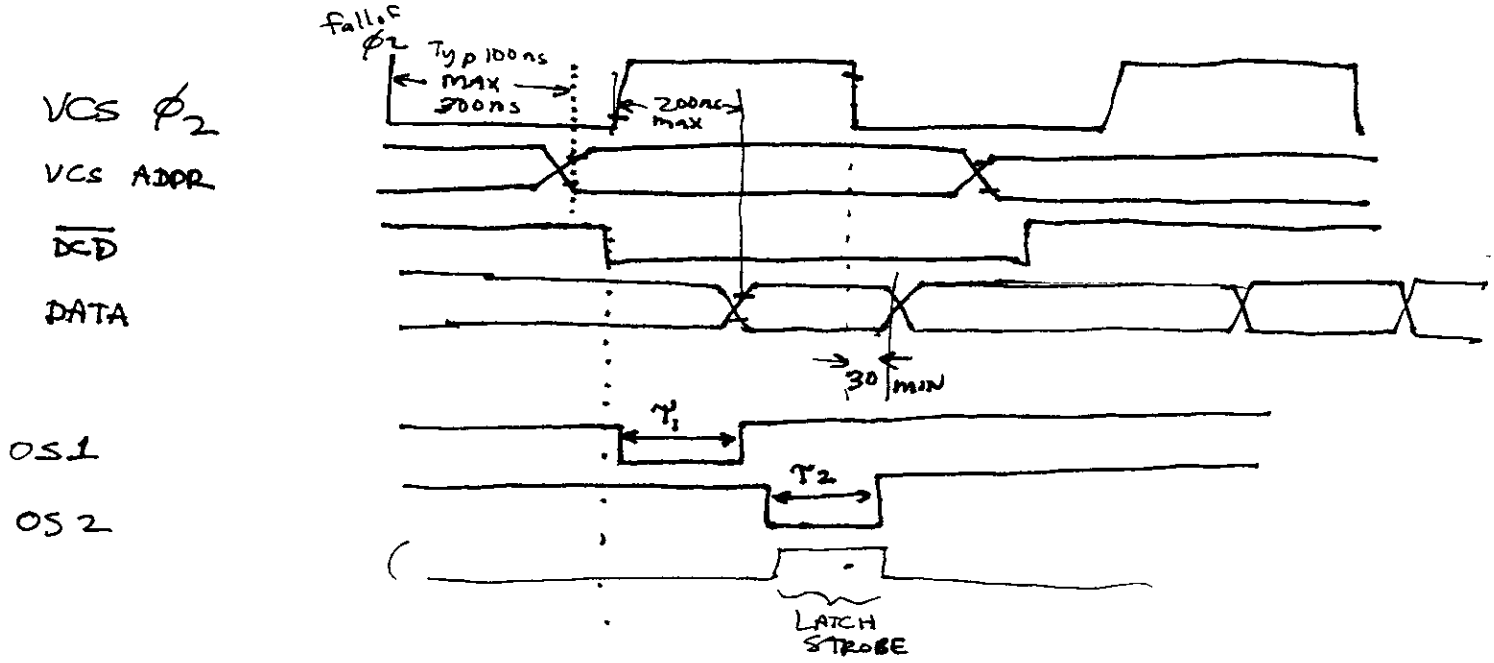
MAX CLOCK
TYP ADDR
MAX DATA



MAX CLOCK
TYP ADDR
TYP DATA

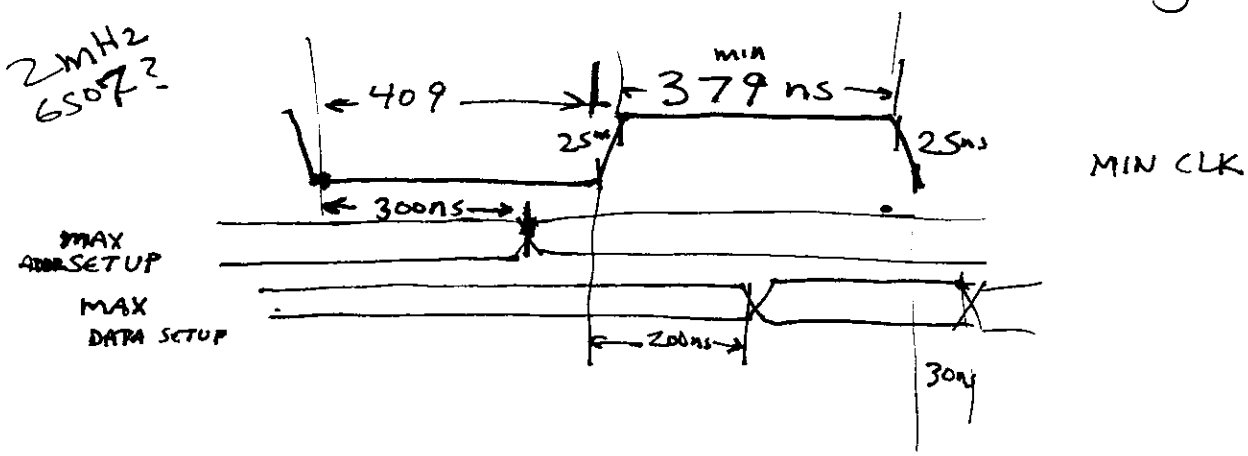


THIS IS THE TIMING:



CYCLE IN VCS IS BURST/3 = 1.19 ~~MHz~~

= 838.09 ns cycle time



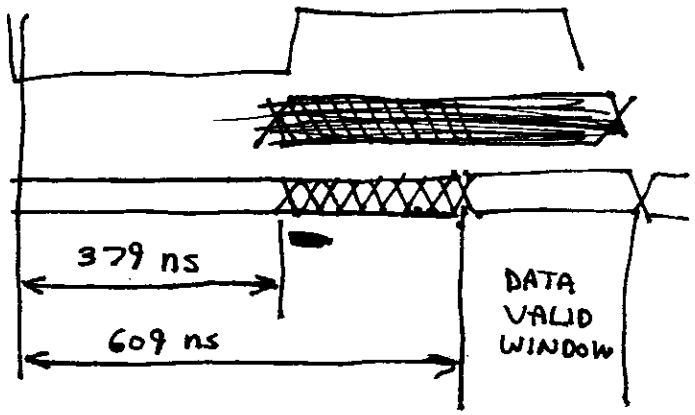
THE LINK CIRCUIT MUST GUARANTEE THAT THE DATA STROBE OCCURS WITHIN THE DATA VALID WINDOW

1.) ADDRESS CAN BE VALID ANYWHERE FROM 30ns TO 300ns into cycle (typ 100ns)

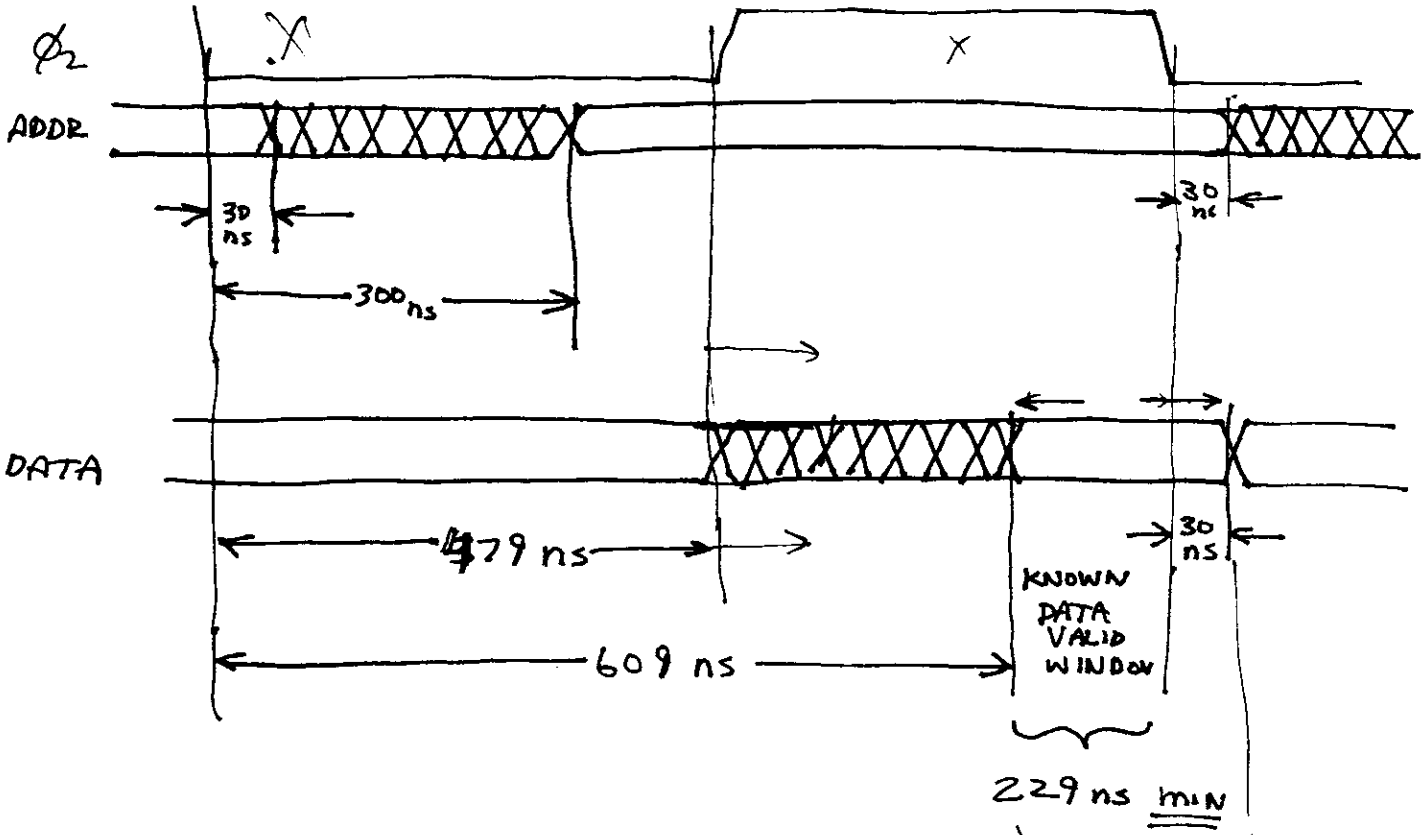
2.) RISING EDGE OF ϕ_2 CAN FALL ANYWHERE FROM 379ns TO 409ns into cycle

3.) DATA VALID CAN OCCUR ANYWHERE FROM 0 TO 200 ns AFTER RISING EDGE OF ϕ_2 (typ 150)

∴ DATA CAN BE VALID STARTING ANYWHERE FROM 379 ns TO 609 ns into cycle



135 100 min data valid



VALID ADDRESS ~~*~~ CAN OCCUR

AS CLOSE AS 379 ns to ϕ_2 RISING EDGE

OR AS FAR AS 379 to ϕ_2 RISING EDGE

∴ VALID ADDRESS CAN OCCUR

AS CLOSE ~~AS~~ 309 ns to ~~⇔~~ known valid data

OR AS FAR AS 579 ns to known valid data

IF YOU PICK 579 ns and system is ~~best~~ worst case

YOUR DATA STROBE WILL OCCUR 879 ns AFTER START OF CYCLE

WHICH IS OUTSIDE OF A KNOWN DATA VALID WINDOW (by 10ns)

IF YOU PICK 309 ns and system is best case

YOUR DATA STROBE WILL OCCUR 339 ns AFTER START of CYCLE WHICH IS OUTSIDE of KNOWN DATA VALID WINDOW ~~by~~ (by 270 ns).

WITH 550 ns O.S.

1.- Typical case (TADS = 100, TMDS = 150)

2.- WORST CASE (UNREALISTIC)

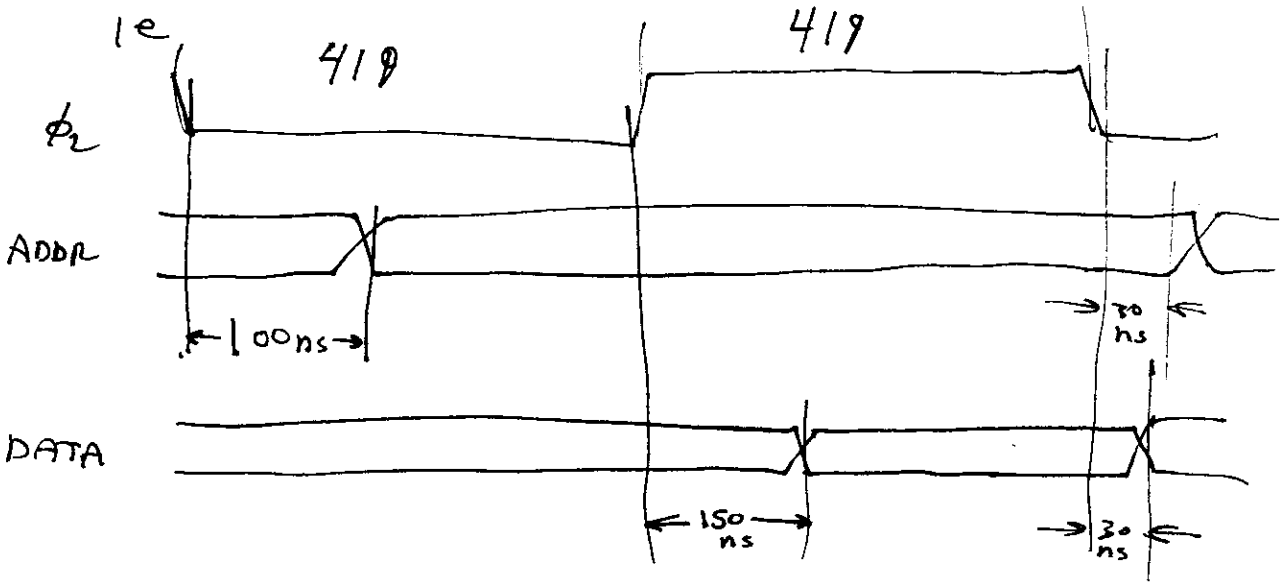
3.- BEST CASE (UNREALISTIC)

4.- WORST CASE TRACKING

5.- BEST CASE TRACKING

IF O.S. IS 550 ns
typ case is

If typical case is used,



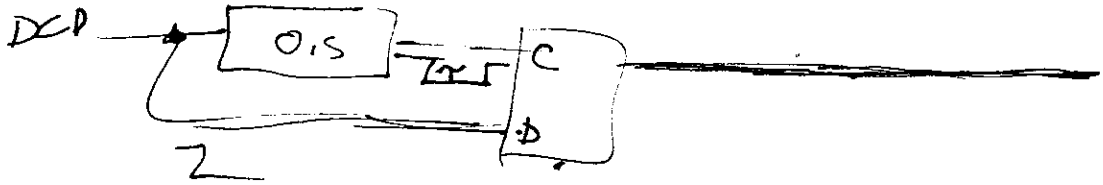
O.S. = 469 ns TO START OF DATA VALID

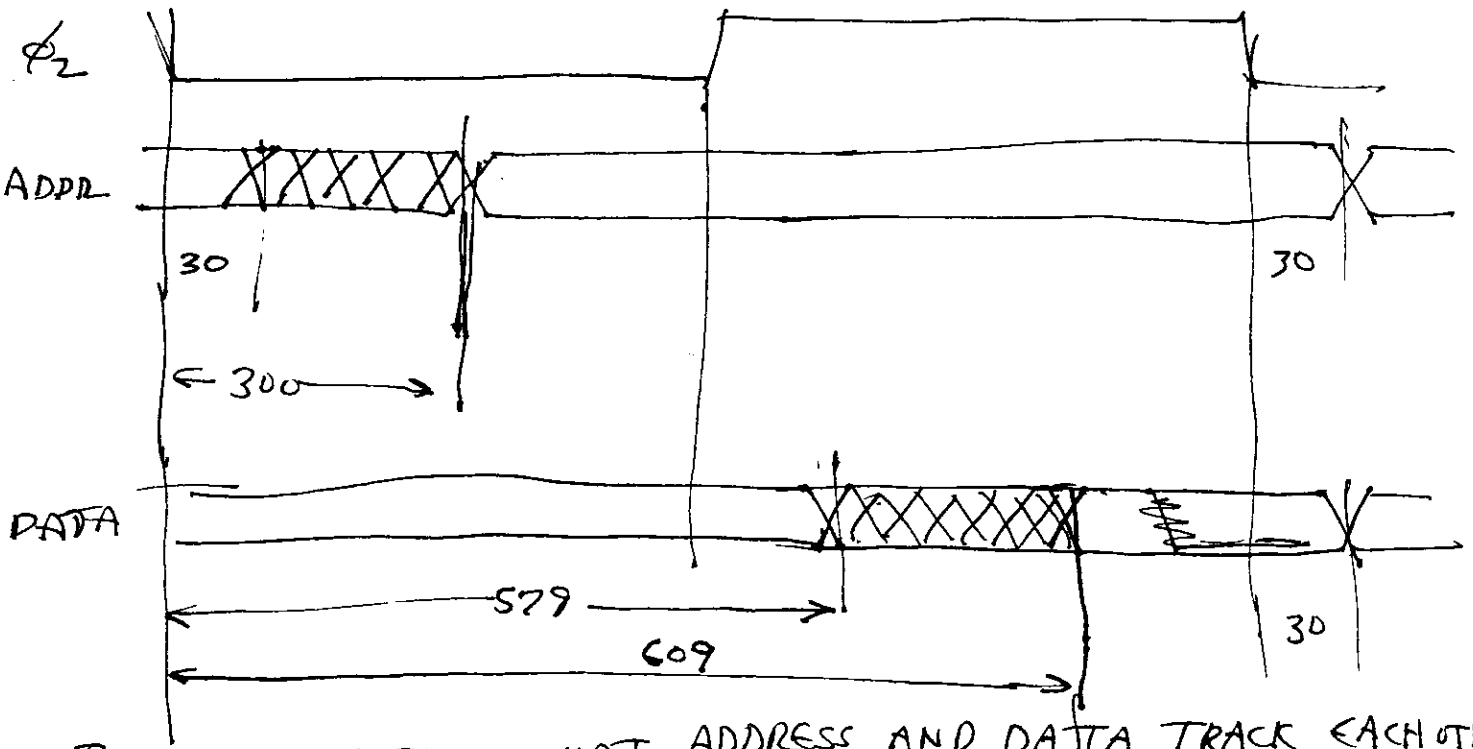
TRIGGER OFF ADDR DECODE AND WAIT
619 ns

YOU WANT A NUMBER YOU CAN ADD TO 300 and get less than or equal to 868
and which you can add to 30 and get greater than or equal to 609

$$\begin{cases} 609 < A + 300 < 868 \\ 609 < A + 30 \leq 868 \end{cases}$$

I need 10 ns!!





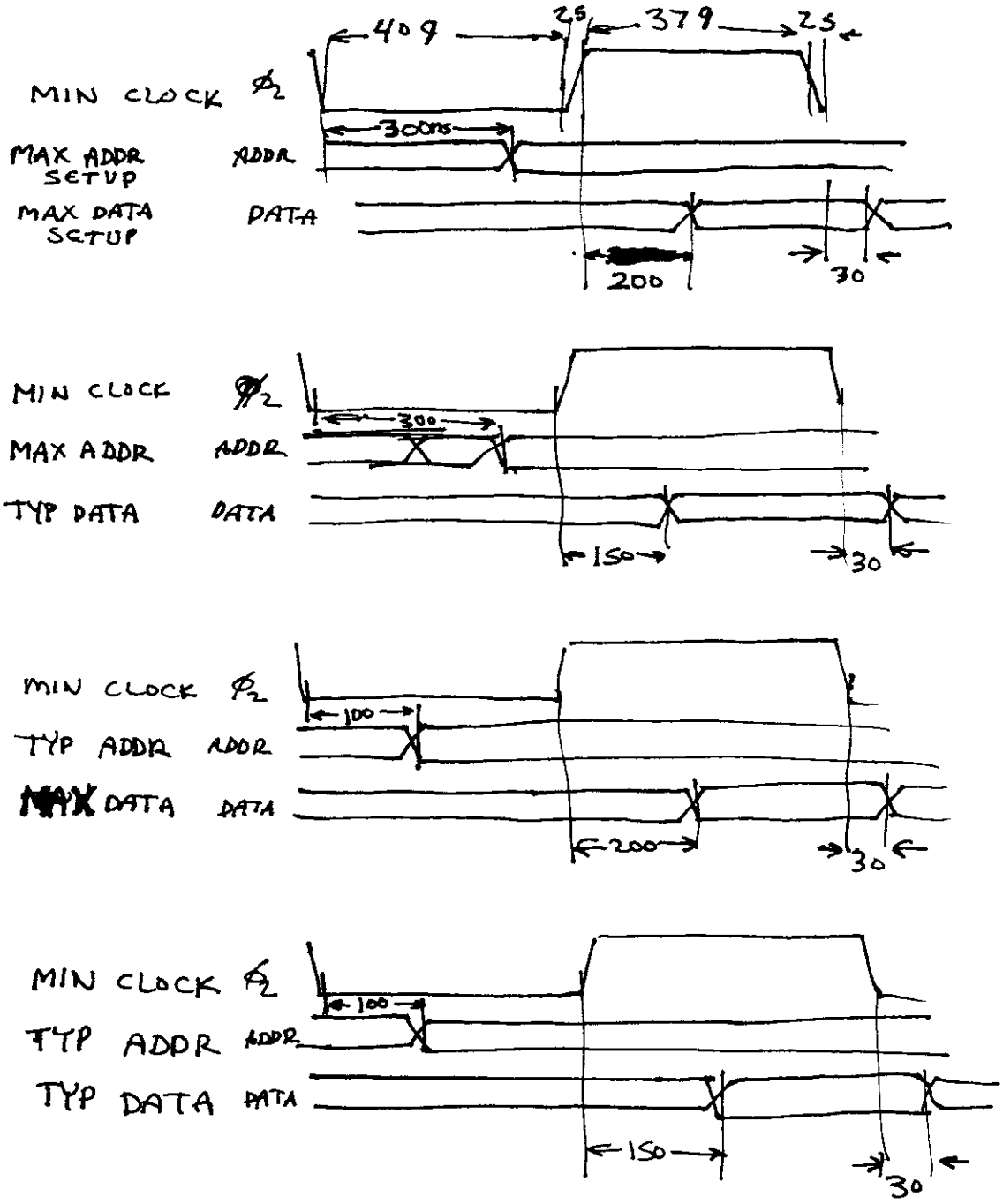
~~3~~ USING THE FACT THAT ADDRESS AND DATA TRACK EACH OTHER:

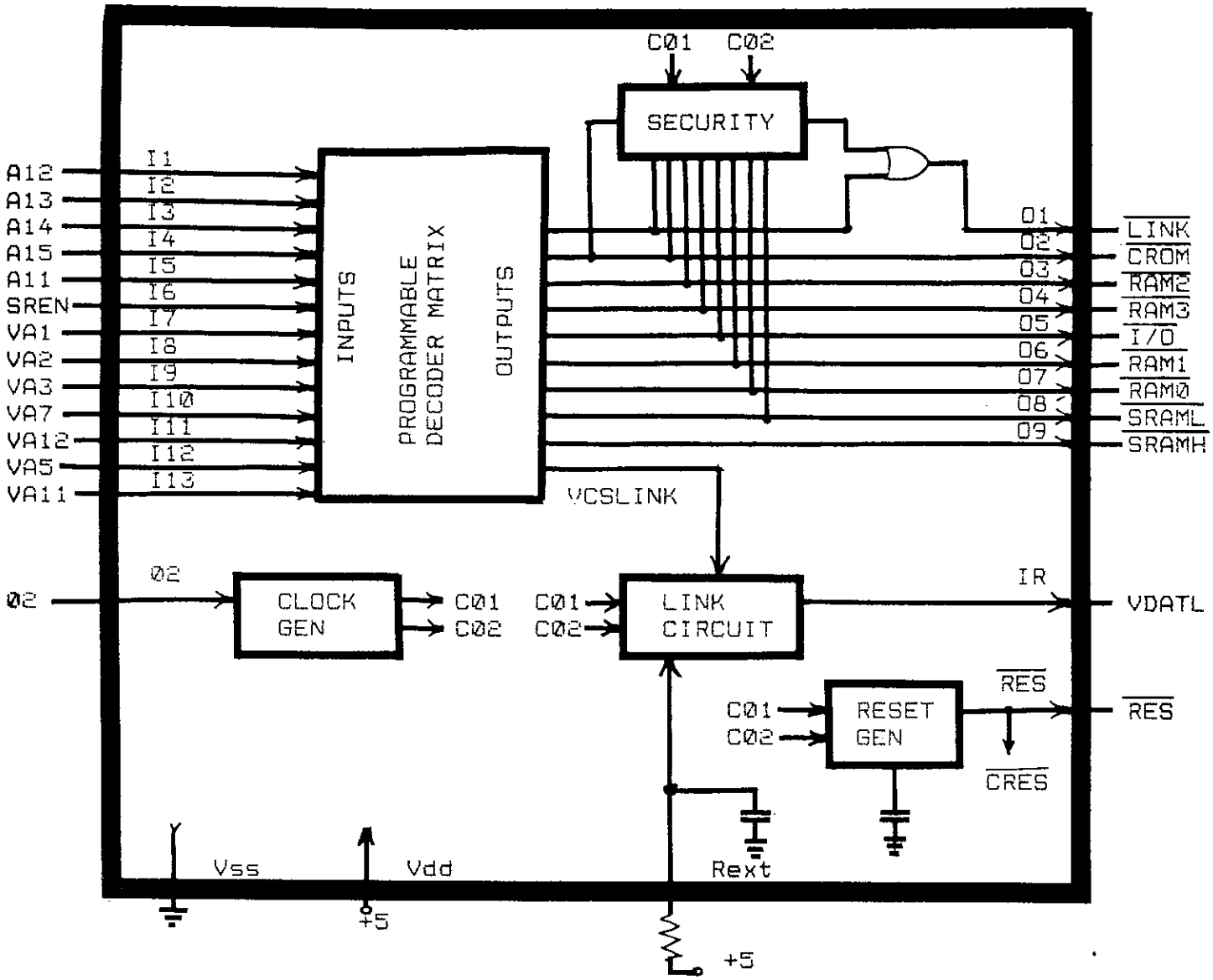
IF ~~ADDR IS~~ 300ns DATA IS PROBABLY 200 (TDS) ∴ $609 < 300 + A < 868$

IF ADDR IS 30 DATA IS PROBABLY 100 (TDS) ∴ ~~$509 < 30 + A < 868$~~

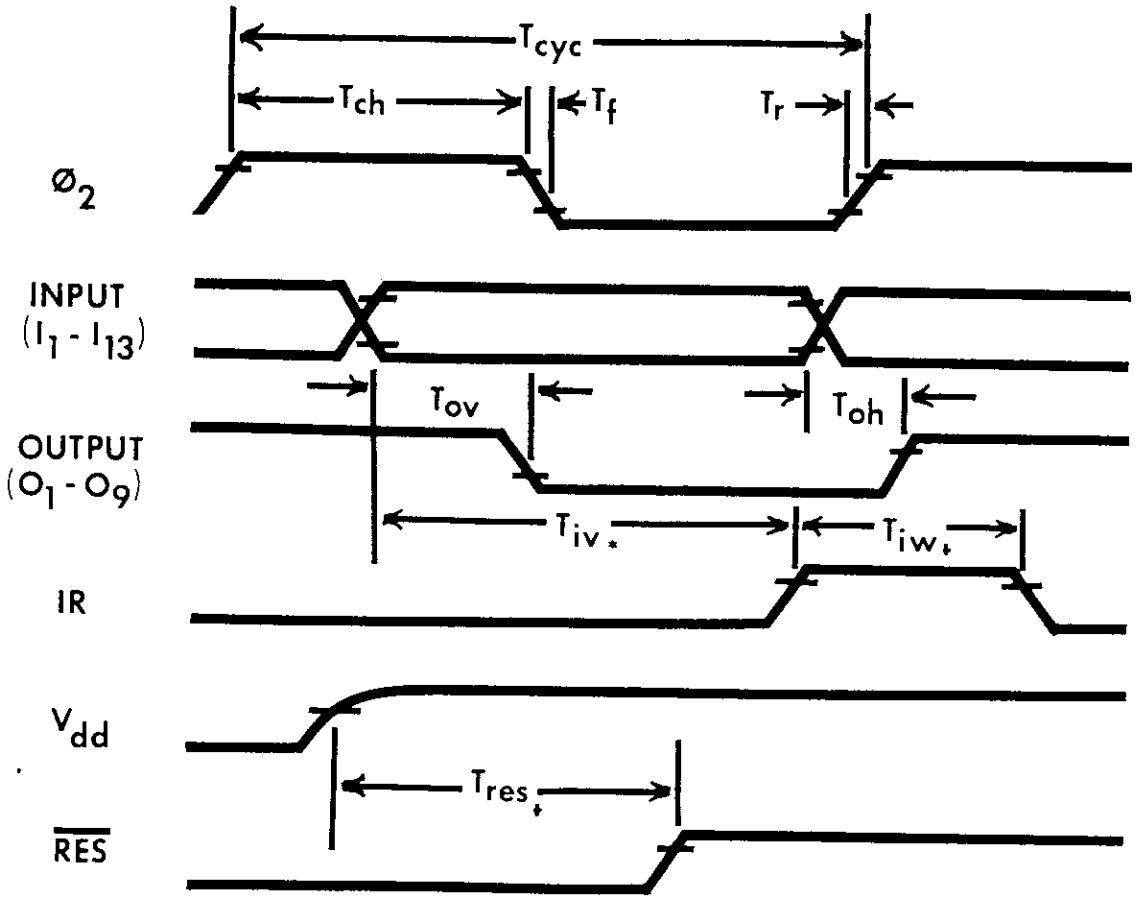
$509 < 30 + A < 868$

~~A~~ SET STROBE FOR 500 ns


MIN CLOCK
MAX ADDR SETUP
MAX DATA SETUP
ADDR
DATA
409
25
379
25
300ns
200
30
MIN CLOCK
MAX ADDR
TYP DATA
ADDR
DATA
300
150
30
MIN CLOCK
TYP ADDR
MAX DATA
ADDR
DATA
100
200
30
MIN CLOCK
TYP ADDR
TYP DATA
ADDR
DATA
100
150
30



FRODOCHIP BLOCK DIAGRAM



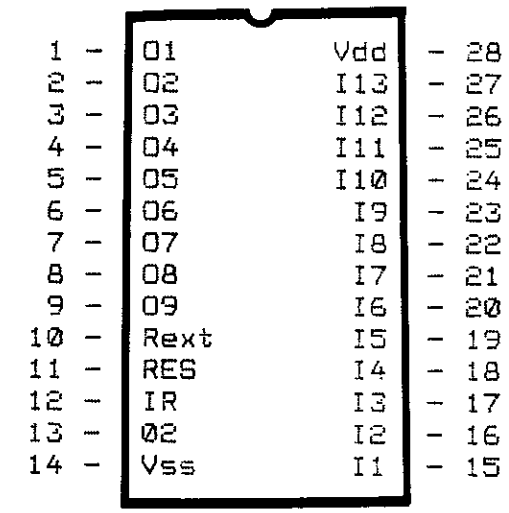
AC CHARACTERISTICS (Ta= 0°C to 70°C, Vdd= +5 ±10% Volts)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Tcyc	Clock Cycle Time	40	—	1.0	uS
Tch	Clock High Width	400	500	600	nS
Tr, Tf	Rise/Fall Time	—	—	50	nS
Tov	Input to Output Valid Delay	—	—	150	nS
Toh	Output Hold Time	30	—	150	nS
Tiv *	Input to IR Strobe Delay	530	560	590	nS
Tiw +	IR Strobe Width	600	—	1200	nS
Tres +	RES Pulse Width	8	—	—	mS

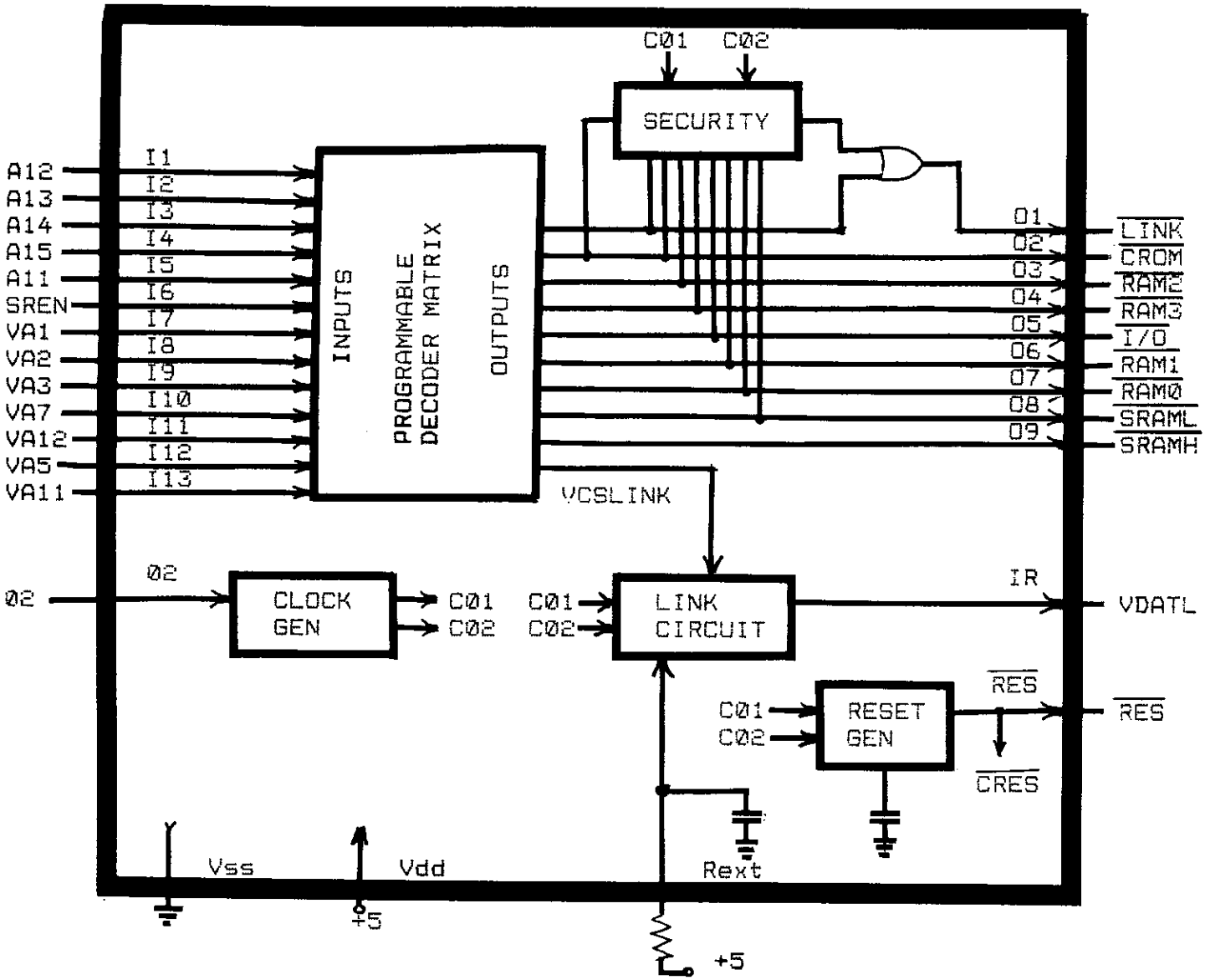
* Measured with Rext= ±1.0%
\+ Measured with Ø2= 1.0 MHz
All outputs measured driving one TTL load and 100 pf.

DC CHARACTERISTICS (Ta= 0°C to 70°C, Vdd= +5 ±10% Volts)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vil	Input Low Voltage	—	—	0.8	V
Vih	Input High Voltage	2.0	—	—	V
Ild	Input Load Current	—	—	10	uA
Vol	Output Low Voltage	V_{SS}	—	0.4	V
Voh	Output High Voltage	2.4	—	V_{DD}	V
Iol	Output Low Current (Sinking)	1.6	—	—	mA
Ioh	Output High Current (Sourcing)	200	—	—	uA
Idd	Supply Current	—	—	50	mA
Cp	Input/Ouput Capacitance	—	—	10	pf



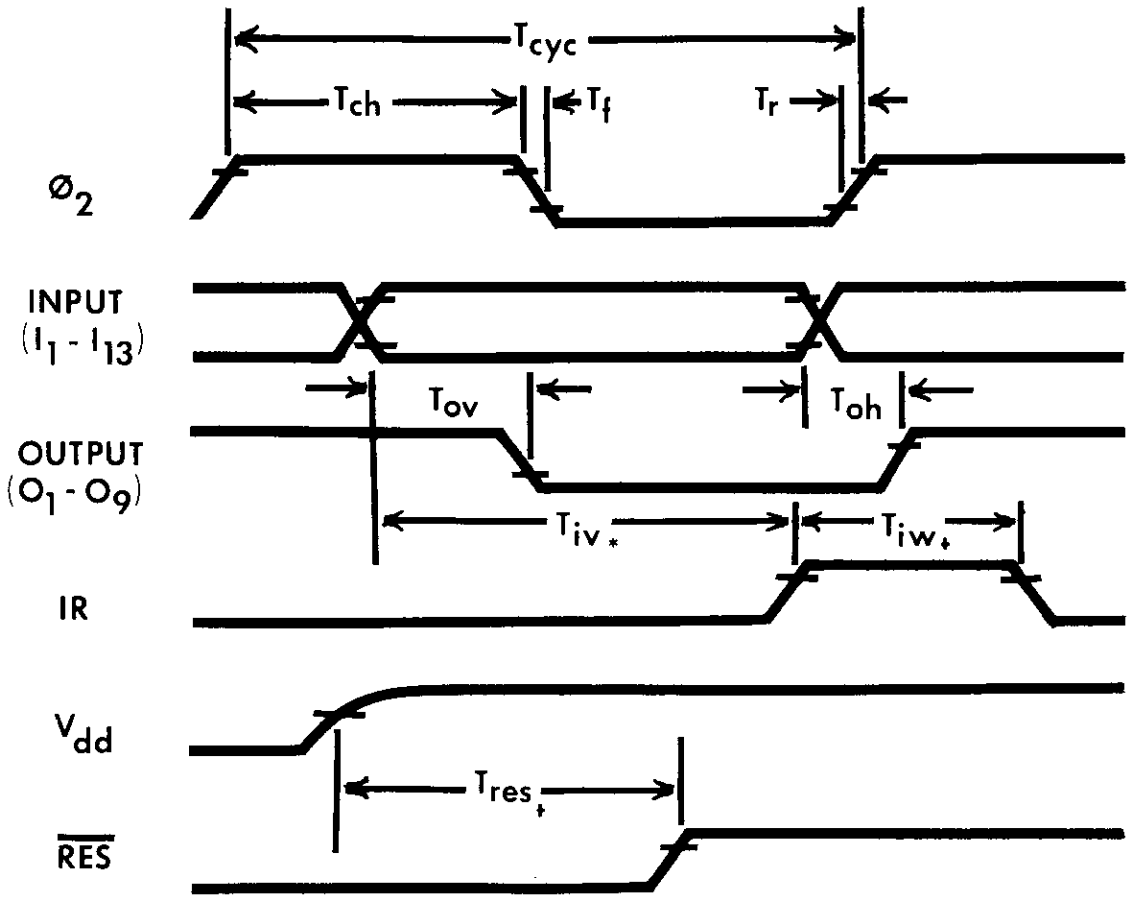
FRODOCHIP PIN CONFIGURATION



FRODOCHIP BLOCK DIAGRAM

DC CHARACTERISTICS (Ta= 0 C to 70 C, Vdd= 5 ±10% Volts)

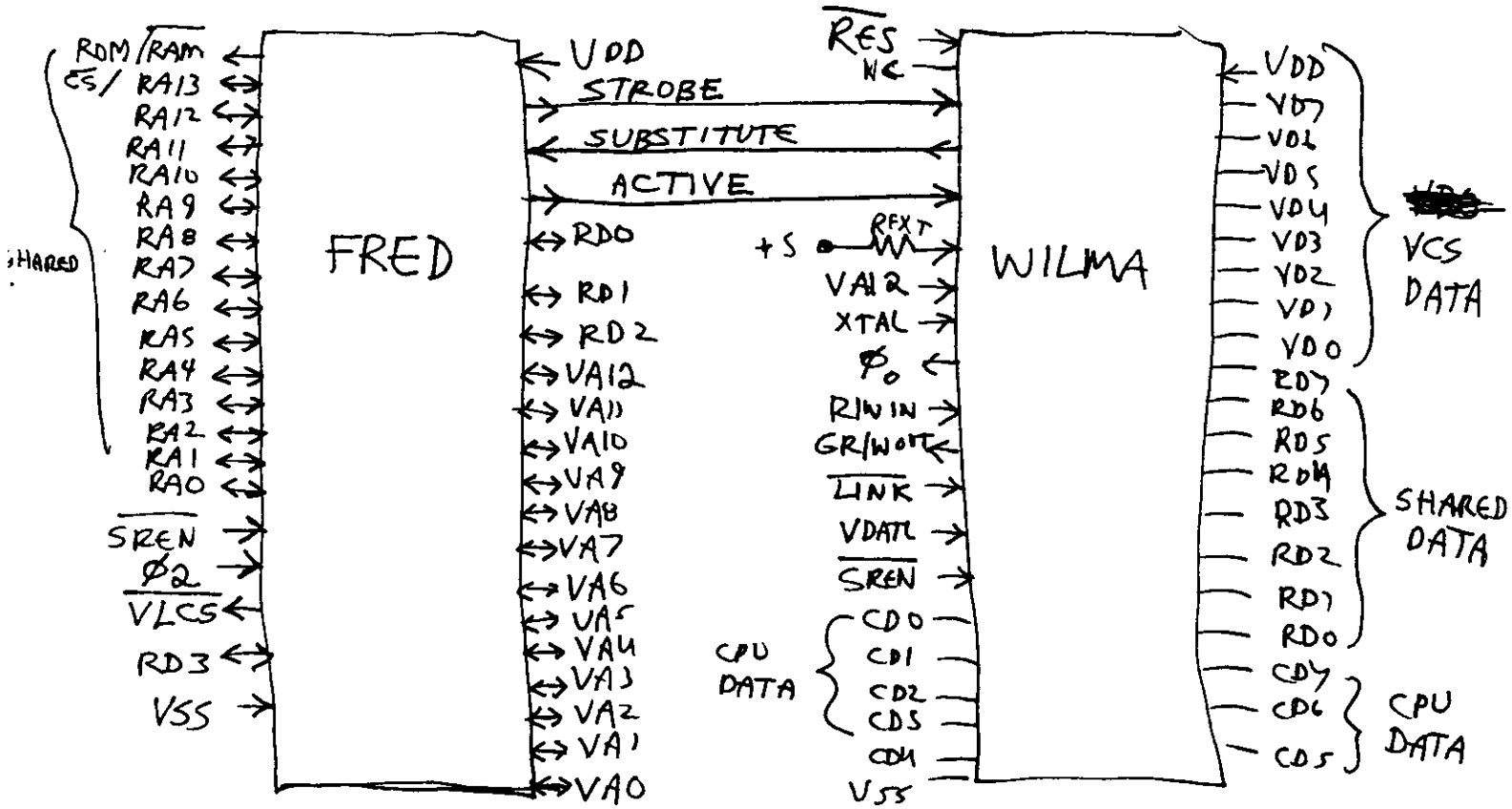
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vil	Input Low Voltage				V
Vih	Input High Voltage				V
Ild	Input Load Current				uA
Vol	Output Low Voltage				V
Voh	Output High Voltage				V
Iol	Output Low Current (Sinking)				mA
Ioh	Output High Current (Sourcing)				uA
Idd	Supply Current				mA
Cp	Input/Ouput Capacitance				pf

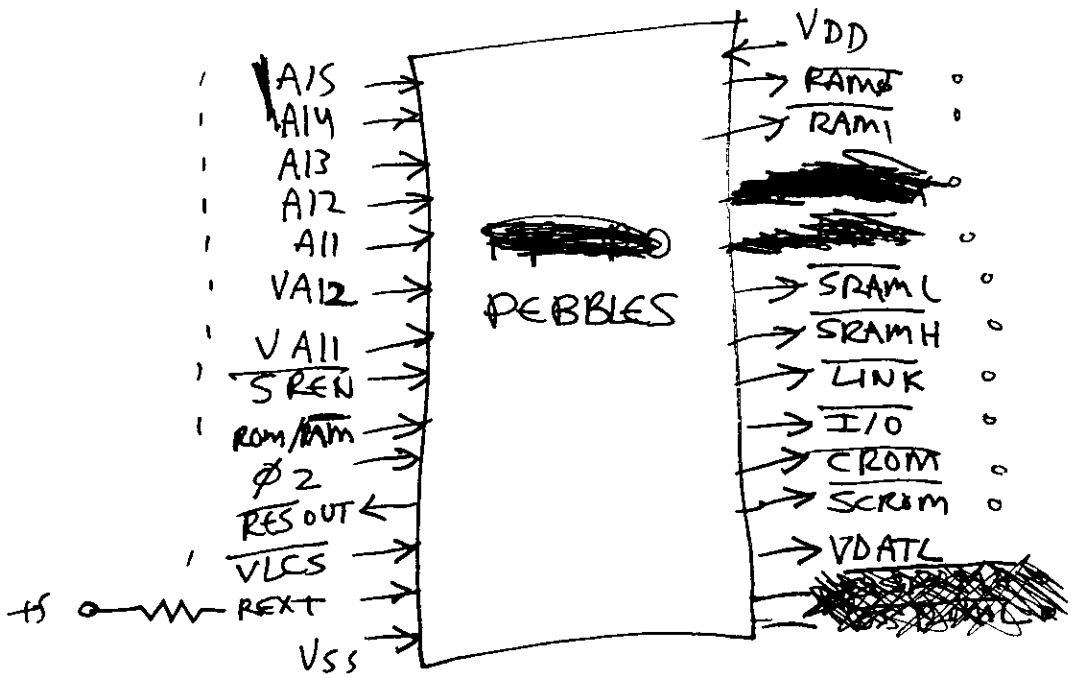


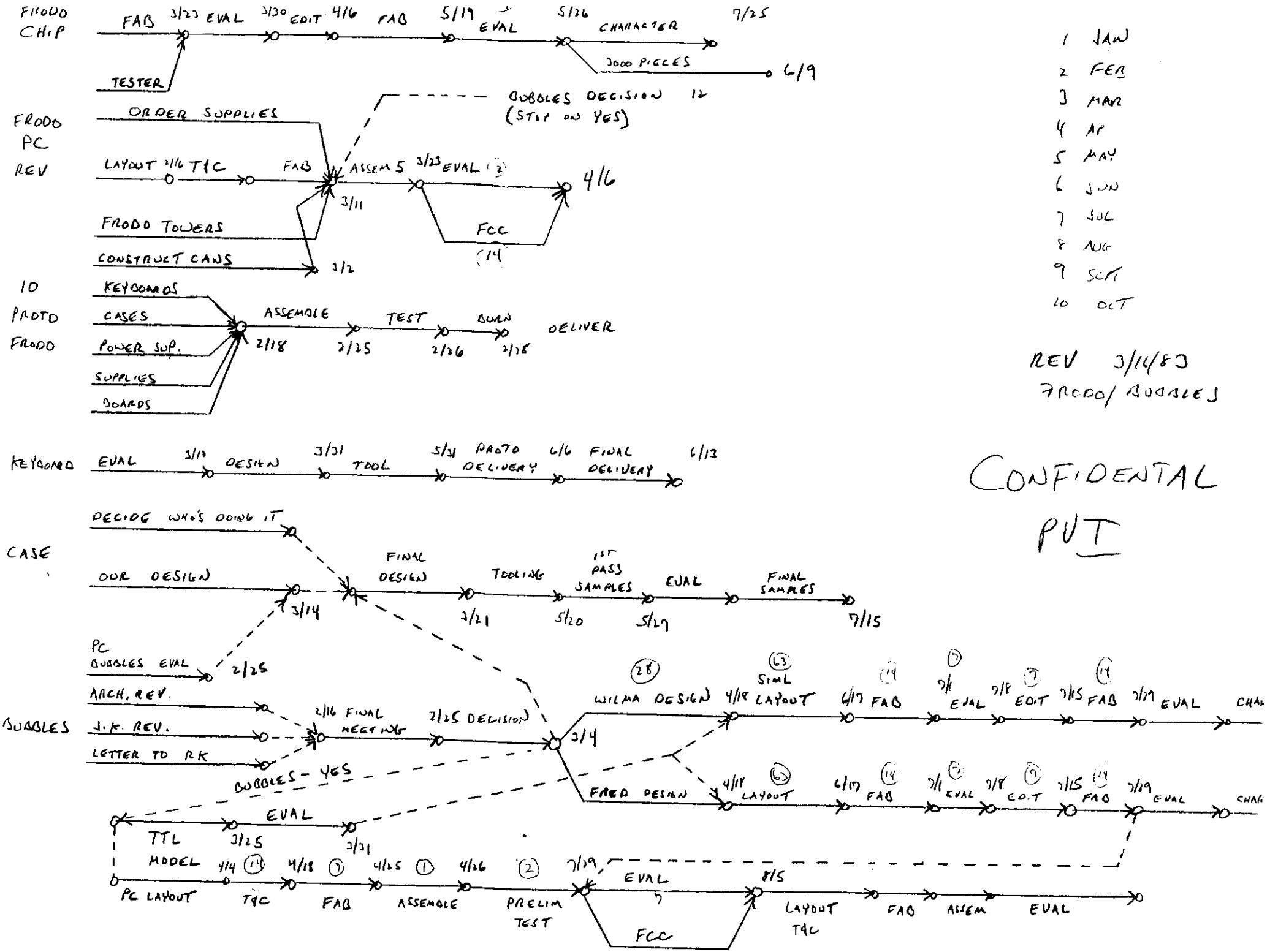
AC CHARACTERISTICS (Ta= 0°C to 70°C, Vdd= +5 ±10% Volts)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Tcyc	Clock Cycle Time				uS
Tch	Clock High Width				nS
Tr, Tf	Rise/Fall Time				nS
Tov	Input to Output Valid Delay				nS
Toh	Output Hold Time				nS
Tiv *	Input to IR Strobe Delay				nS
Tiw +	IR Strobe Width				nS
Tres +	RES Pulse Width				mS

* Measured with Rext= ±1.0%
\+ Measured with Ø2= 1.0 MHz
All outputs measured driving one TTL load and 100 pf.


FRED
WILMA
ROM/RAM
CS/
RA13
RA12
RA11
RA10
RA9
RA8
RA7
RA6
RA5
RA4
RA3
RA2
RA1
RA0
SHARED
SREN
Ø2
VLCS
RD3
VSS
VDD
STROBE
SUBSTITUTE
ACTIVE
RD0
RD1
RD2
VA12
VA11
VA10
VA9
VA8
VA7
VA6
VA5
VA4
VA3
VA2
VA1
VA0
RES
NC
+5
REXT
VA12
XTAL
Ø0
RIWIN
GR/WOUT
LINK
VDATL
SREN
CPU DATA
CD0
CD1
CD2
CD3
CD4
VSS
VDD
VD7
VD6
VD5
VD4
VD3
VD2
VD1
VD0
VCS DATA
RD7
RD6
RD5
RD4
RD3
RD2
RD1
RD0
SHARED DATA
CD7
CD6
CD5
CPU DATA


PEBBLES
A15
A14
A13
A12
A11
VA12
VA11
SREN
ROM/RAM
Ø2
RESOUT
VLCS
+5
REXT
VSS
VDD
RAM0
RAM1
SRAML
SRAMH
LINK
I/O
CROM
SCRAM
VDATL

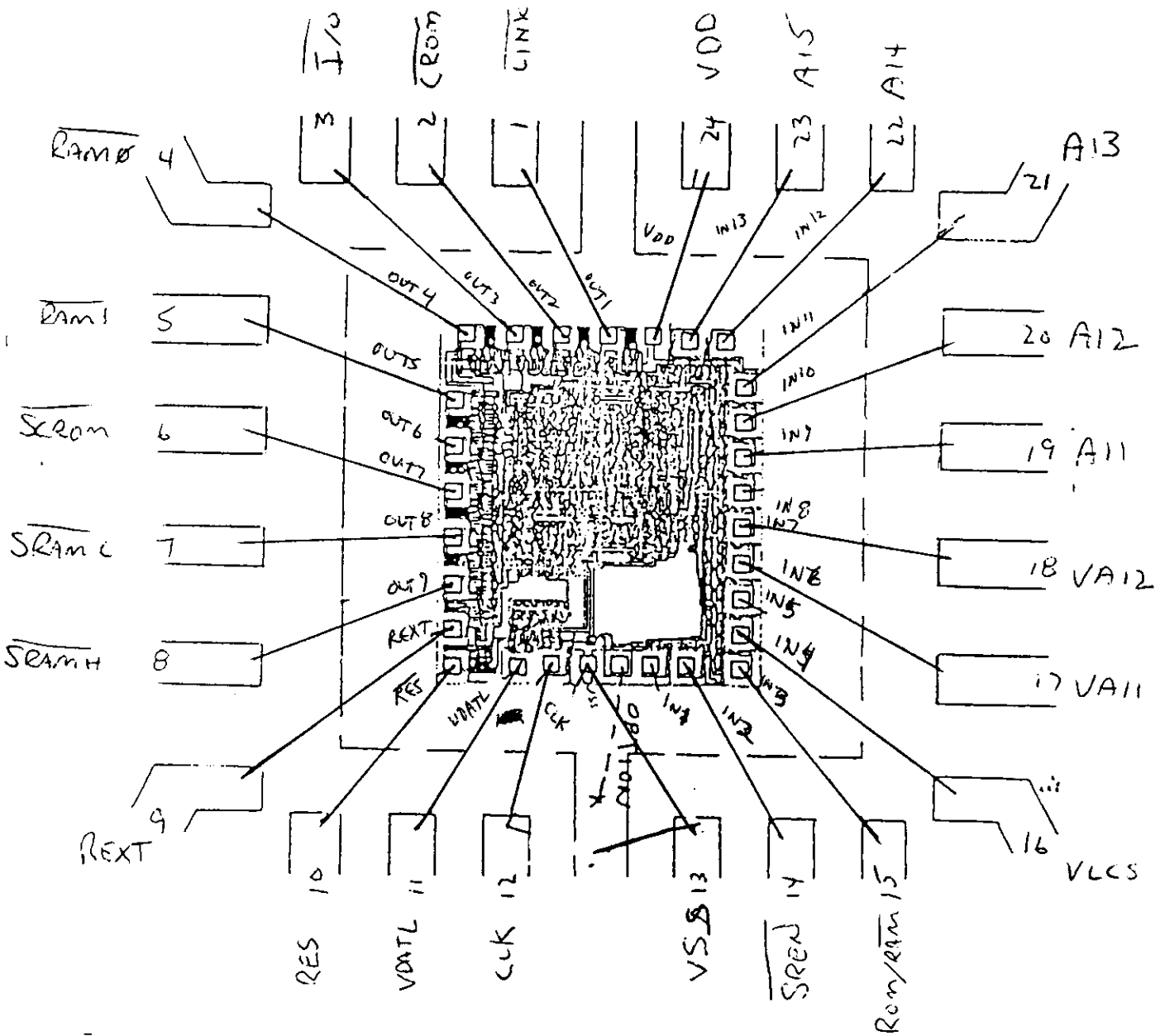


1 JAN
2 FEB
3 MAR
4 APR
5 MAY
6 JUN
7 JUL
8 AUG
9 SEPT
10 OCT

REV 3/14/83
FRODO/BUBBLES

CONFIDENTAL

PUT



SCALE: 20X

BONDING DIAGRAM

FORMS A PART OF

AND WILL BE USED

IN PLACE OF ATOMICS P.O NO. _____

DESIGNATOR: 1 2 6

CUSTOMER: PVI

DEVICE TYPE: _____

PACKAGE TYPE: 28 Leads Plastic

DIE SIZE: 118 X 101 ~

PAD SIZE: 150 X 150

APPROVALS:

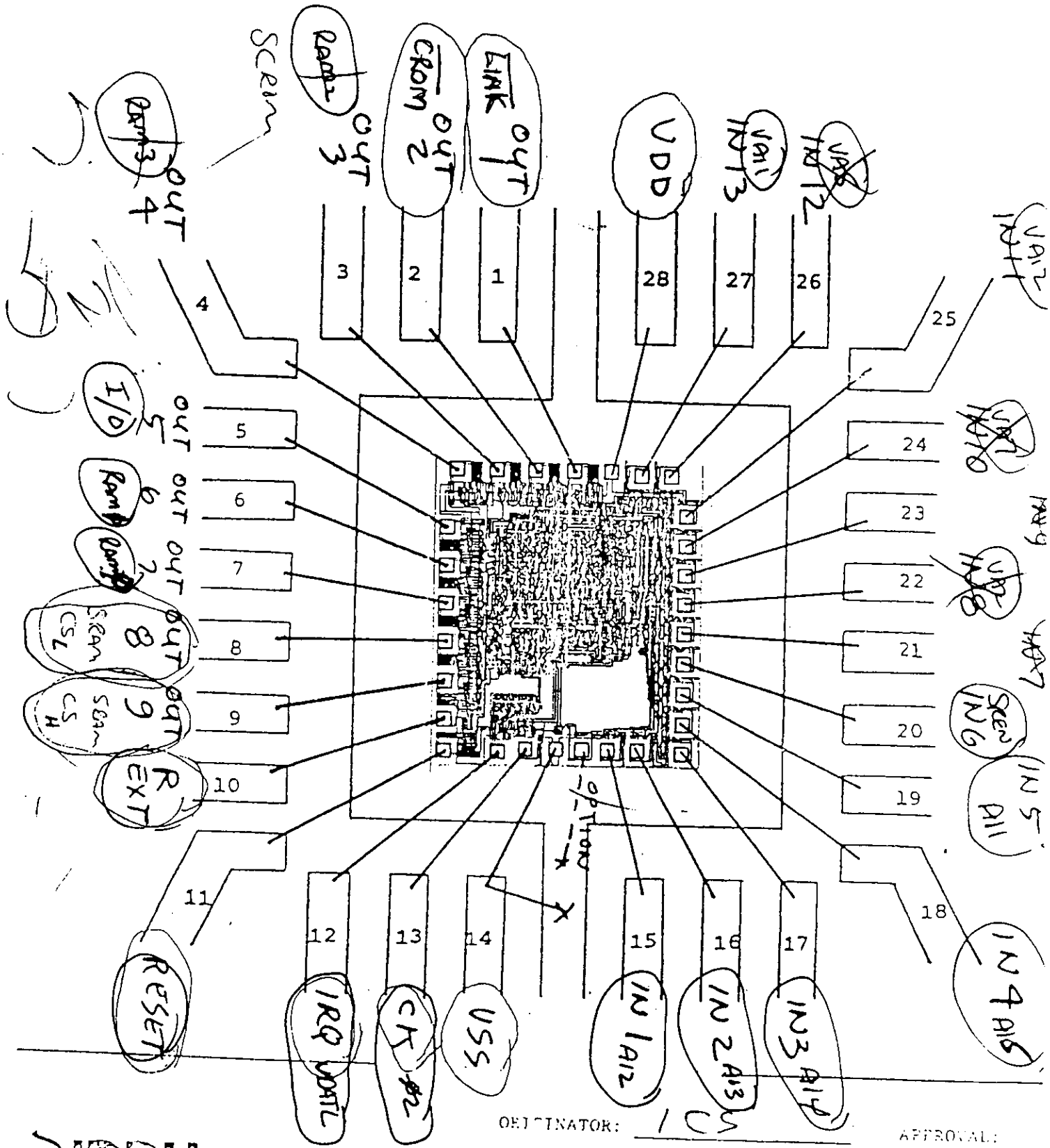
ENG: _____

OP: _____

QA: _____

EFF DATE: 1/5/

TEI FORM 0220-1331



SCALE: 20X

THIS [illegible] BONDING DIAGRAM

NO. _____ FORMS A PART OF

[illegible] AND WILL BE USED

IN PLACE OF [illegible] P/O NO. _____

ORIGINATOR: [illegible]

CUSTOMER: PVI

DEVICE TYPE: _____

PACKAGE TYPE: 28 Leads Plastic

DIE SIZE: 118 X 101 ~

PAD SIZE: 150 X 150

APPROVAL:

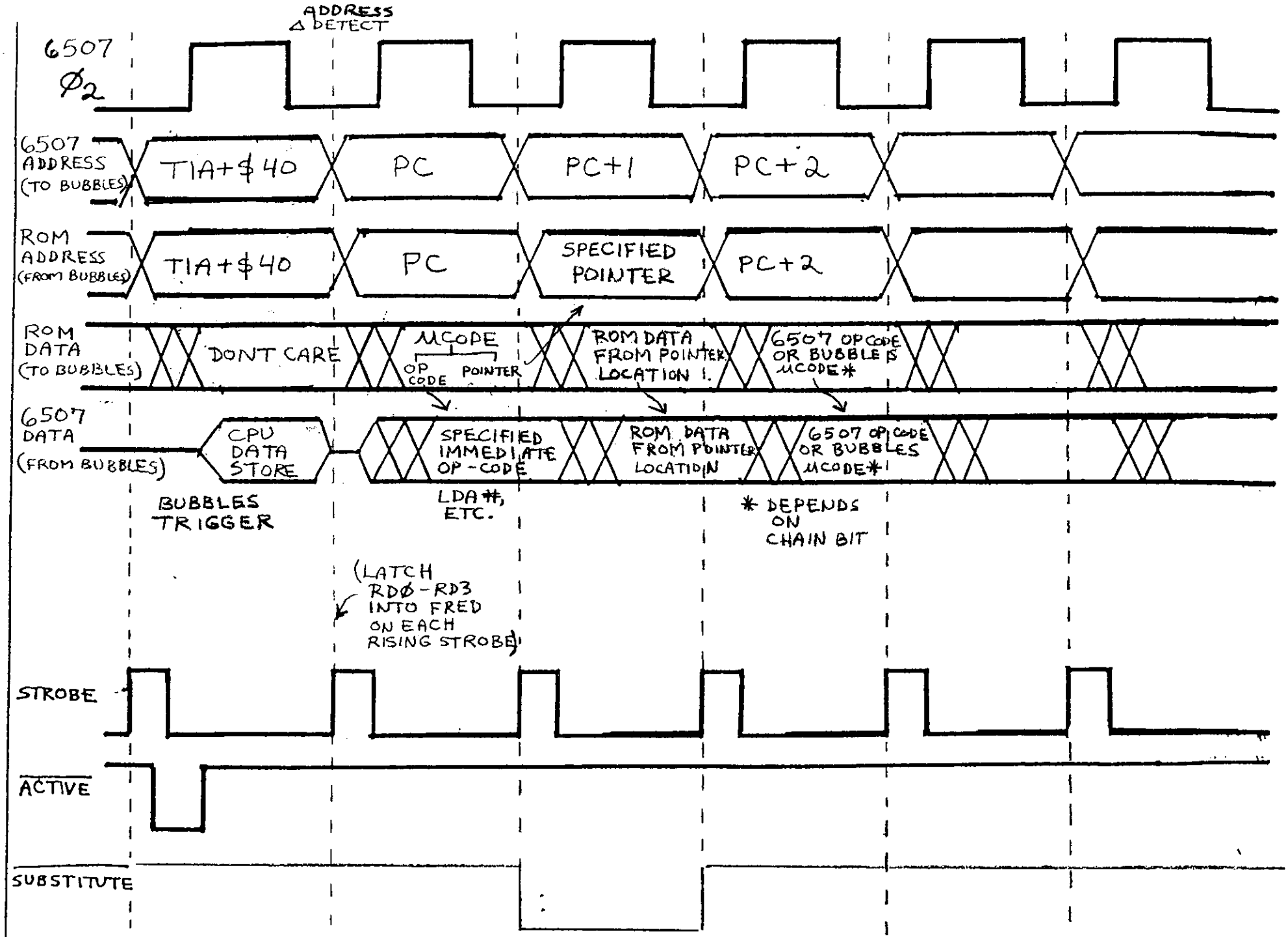
ENG: _____

OP : _____

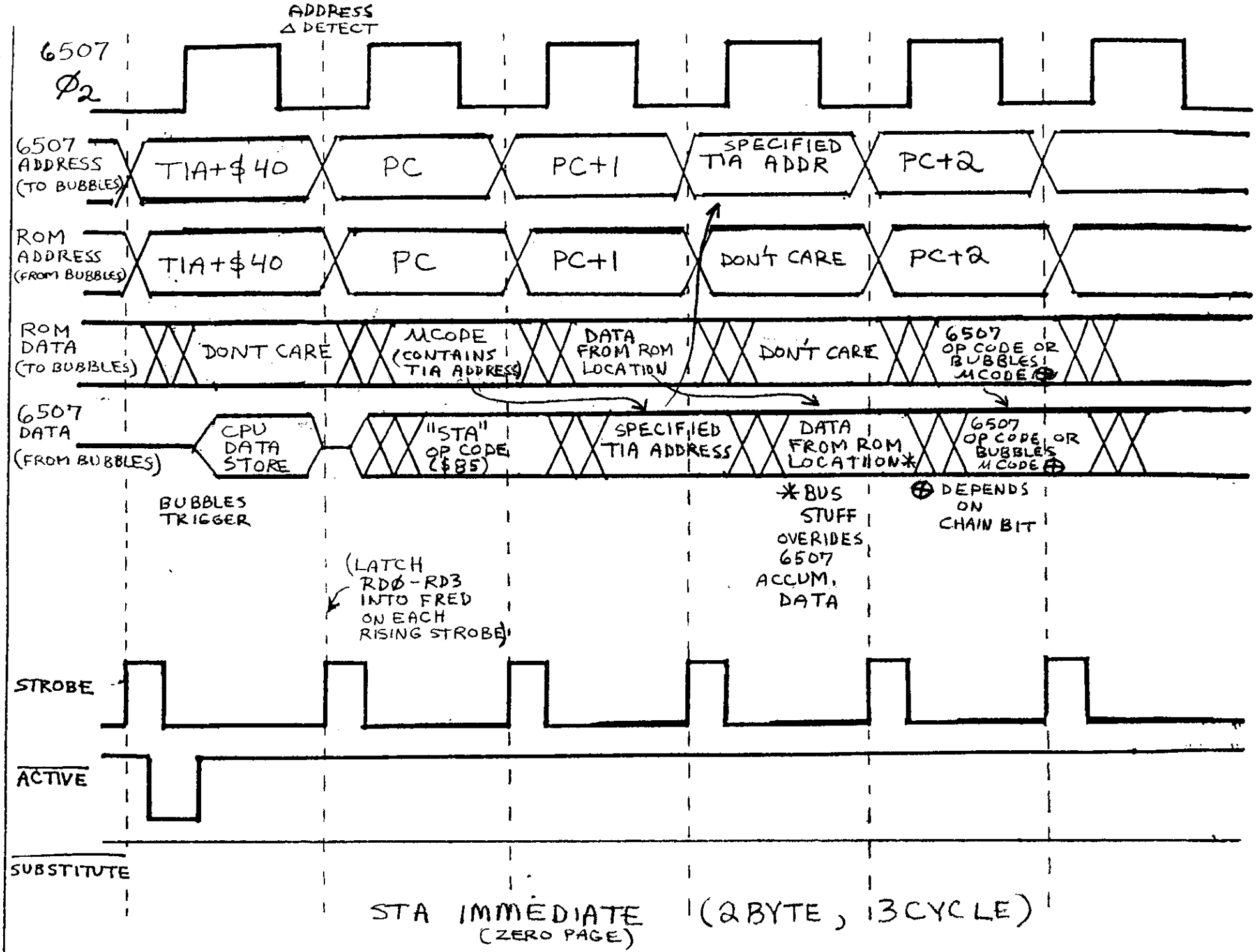
QA : _____

EFF DATE: 1/5/

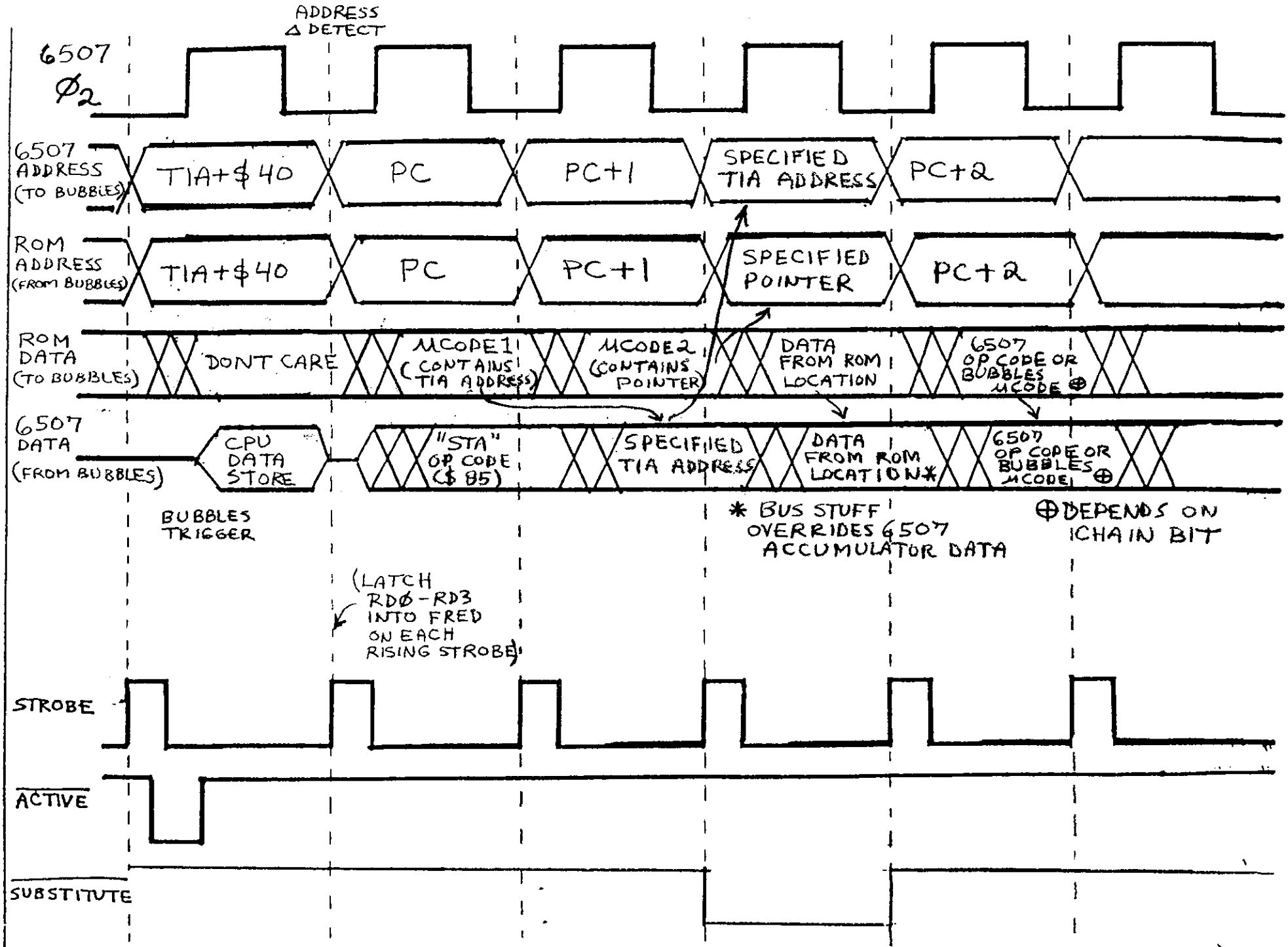
IEI FORM 0220-1331



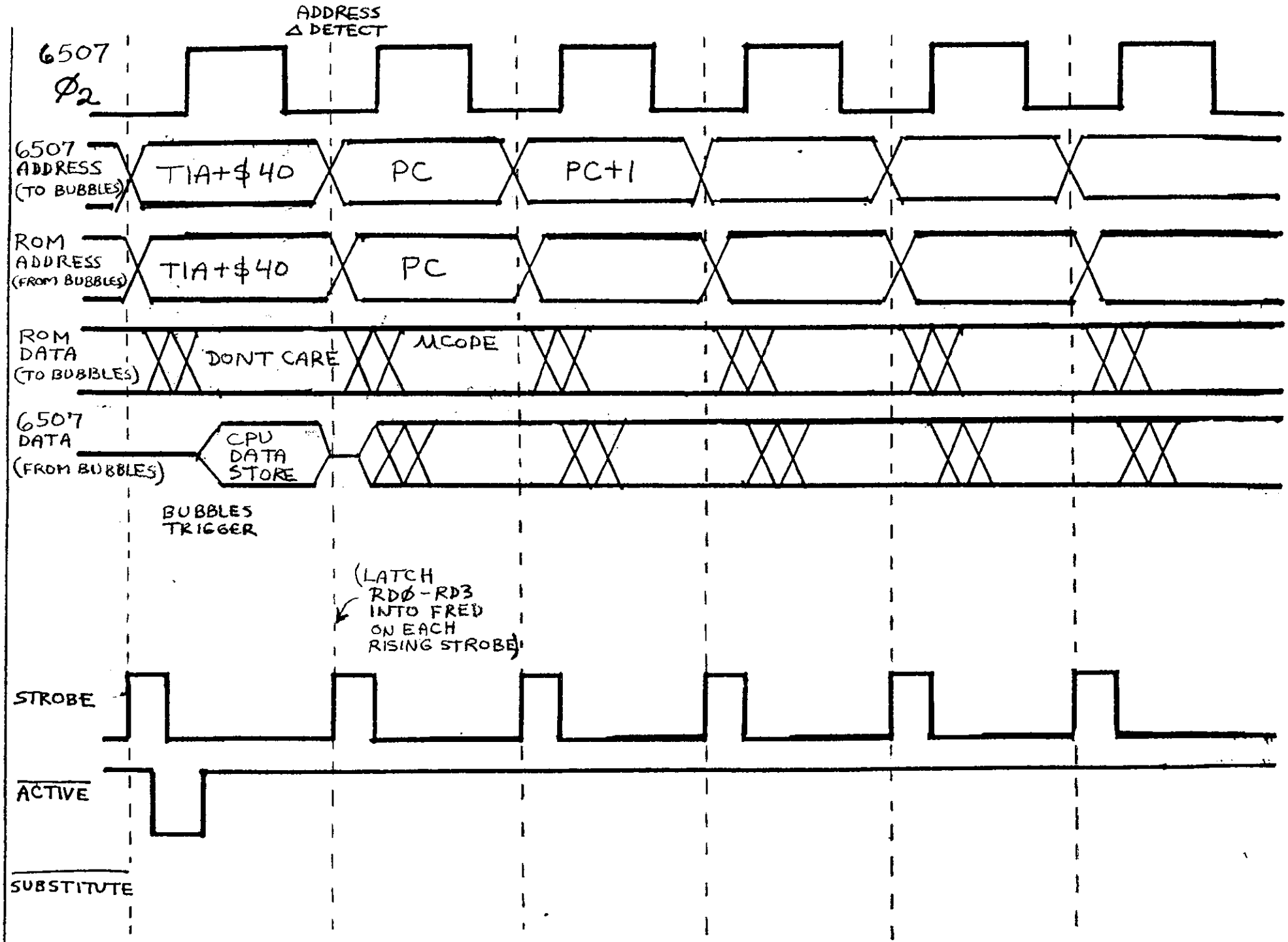
LOAD/OPERATE IMMEDIATE (2 BYTE, 2 CYCLE)

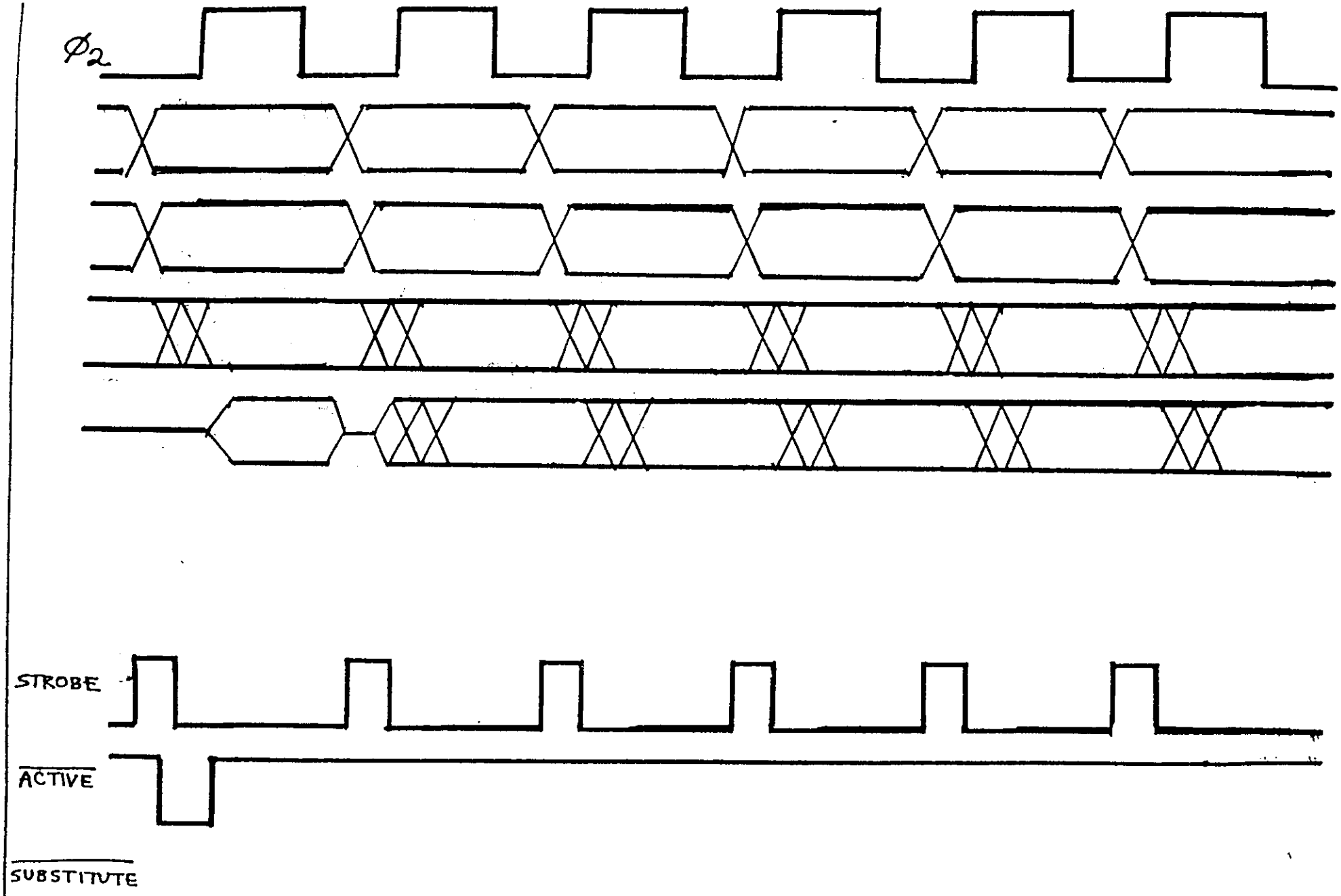


STA IMMEDIATE (2 BYTE, 3 CYCLE)
(ZERO PAGE)



STA IMMEDIATE INDIRECT (3 BYTE, 3 CYCLE)
(ZERO PAGE)


ADDRESS Δ DETECT
6507 Ø2
6507 ADDRESS (TO BUBBLES)
TIA+$40
PC
PC+1
ROM ADDRESS (FROM BUBBLES)
TIA+$40
PC
ROM DATA (TO BUBBLES)
DONT CARE
MCODE
6507 DATA (FROM BUBBLES)
CPU DATA STORE
BUBBLES TRIGGER
(LATCH RDØ-RD3 INTO FRED ON EACH RISING STROBE)
STROBE
ACTIVE
SUBSTITUTE


ϕ_2
STROBE
$\overline{\text{ACTIVE}}$
$\overline{\text{SUBSTITUTE}}$

INSTRUCTIONS FOR USE OF 16K ROM EMULATOR BOARD

The ROM Emulator board is a dual-port 16K byte RAM board. This board uses a COMMODORE 8032 computer as a host for primary software developement. After code has been generated, it is downloaded into the dual-port RAM where the target system is then able to execute the code. Connection to the 8032 is made using dual 50-conductor ribbon cables which attach to the MEMORY EXPANSION BUS (J4 and J9) of the 8032. Alternate lines of the cables are grounded on the 8032 and carry the common ground connection to the Emulator board. The 8032 has an external memory expansion capacity of only 4K bytes. Because of this limitation, the 16K byte RAM is treated as four independent 4K banks which are manually selected using a rotary switch. The unoccupied 4K address space in the 8032 is located from $9000 through $9FFF. Normally this space is used for internal ROM expansion and buffers prevent accessing data from the external bus. In order to use the Emulator board, a jumper in the 8032 (Jumper M, "ROM 9 OUT") must be installed. Dipswitches provided on the Emulator allow the board to be located on any 4K boundary of the host system. Additional dipswitches allow the bank size to be selected. The Emulator can be configured as one 16K bank (starting on one of the system's four 16K boundaries), two 8K banks (starting on one of the eight 8K boundaries) or four 4K banks (starting on one of the sixteen 4K boundaries). Switching between banks is accomplished manually using the rotary switch. The high order addresses are automatically taken from the host or the rotary switch, depending on the bank configuration selected. This approach allows the Emulator to work with any host system having at least 4K, 8K or 16K bytes of open address space. For operation with the 8032, the address switches should be set to locate the board starting at $9000 and the bank size switches should be set to four 4K banks. The bank presently accessible to the 8032 is manually selected using the rotary switch.

The Emulator connects to the target system using ribbon cable. Connection can be made to the 44-pin connector, or 24-pin dip header cables can be run from the ROM sockets on the target system to the 24-pin sockets on the Emulator. The board can be configured as either a contiguous 16K byte ROM or two independent 8K byte ROMs. A dipswitch is provided to select the configuration, however certain jumper connections must also be made at the 44-pin connector. Because of this, it is recommended that a special cable be made up for each different ROM application (i.e. contiguous 16K bytes, dual contiguous 8K bytes or dual non-contiguous 8K bytes). Regardless of the configuration selected, there is no limit to the start/end boundaries or the ROM size, as the Emulator is totally controlled by the Chip Selects (negative active) generated by the target system. In other words, the user is free to select any ROM size (16K bytes or less) located anywhere in the target system address space provided the appropriate chip select is generated by the target system. The emulator expects the chip select signals to be brought in via the ribbon cables.

Note that from the point of view of the host system, the Emulator looks like RAM--no write protect is provided. From the point of view of the target system, the Emulator looks like ROM only. The read/write signal from the target system does not go to the Emulator, therefore the target system is not capable of modifying the contents of the Emulator RAM. Whenever a valid select address comes from the host system, the host is automatically given control of the Emulator. That is, the addresses from the host are sent to the Emulator memory and data will either be written or read by the host. If the target system was running out of the Emulator at the time the host access occurred, operation of the target system will most likely be disrupted. Normally the Emulator is accessed by the target system and the host system only gains access when needed, however a switch is provided to remove the Emulator from the target system address space and place it only in the host address space. This switch can be used to prevent bus fights, without disconnecting the Emulator, should another device be installed temporarily in the Emulator address area.

The following tables list the switches and their functions:

The dip switch pack is defined as follows:

```
1        Ø

[[[[[]]]]]  A12   When set to "Ø", address line 12 of the host
                    sytem must be low to select the Emulator.
[[[[[]]]]]  A13   Same as above for host address line 13.

[[[[[]]]]]  A14   Same as above for host address line 14.

[[[[[]]]]]  A15   Same as above for host address line 15.

[[[[[]]]]]  16K   When set to "Ø", the Emulator appears as
                    one 16K bank to the HOST system.
[[[[[]]]]]   8K   When set to "Ø", the Emulator appears as
                    two 8K banks to the HOST.
[[[[[]]]]] 128K   When set to "Ø", the Emulator appears as
                    one 16K bank to the TARGET system.
```

The switches A12, A13, A14 and A15 are the address selector switches which determine where the Emulator appears in the host address space. When a switch is set to "1", the corresponding address line must be high to select the Emulator, when a switch is set to "Ø", the corresponding address must be low to select the Emulator. Note that as bank size changes, the setting of switch A12 (with two 8K banks) and switch A13 (with one 16K bank) become "don't cares". For use with the 8Ø32, the address switches should be set to $9ØØØ. This is accomplished by setting switch A15 to "1", switch A14 to "Ø", switch A13 to "Ø" and switch A12 to "1" (i.e. binary "1ØØ1" or decimal "9").

The switches 16K and 8K determine the size of the RAM banks as they appear to the host system. If switch 16K is set to "Ø", the RAM appears as one 16K bank, the setting of switches A12 and

A13 are irrelevant and the bank selector rotary switch is irrelevant. If switch 8K is set to "Ø", the RAM appears as two 8K banks, the setting of switch A12 is irrelevant and only positions "Ø" and "1" of the rotary switch are needed to select one of the two 8K banks. The 8K switch overides the 16K switch, so if both switches are set to "Ø", the board appears as two 8K banks. If both switches are set to "1", the RAM appears as four 4K banks, all address switches are active and positions "Ø" through "3" of the rotary switch are used to select one of the four banks (this is the mode used with the 8Ø32).

The 128K switch should be set to "Ø" if the Emulator is to appear as 16K contiguous bytes to the TARGET system. If the Emulator is to appear as two independent 8K ROMs, this switch should be set to "1". Appopriate connections must also be made to the 44-pin connector to select the desired configuration (described later).

The "PET ONLY" toggle switch is used to switch the Emulator in or out of the target system memory space. When set to "PET ONLY", the Emulator will not appear in the target system address space and only the host has access. When set to the other position, the Emulator appears in the target system address space at the location determined by the chip selects generated by the target system. The host system will gain access to the Emulator whenever necessary (shutting out the target system at the time of the host access).

The bank select rotary switch is used to select which of the RAM banks is accessible to host system when the Emulator is in a bank mode. If the board is set for two 8K banks, position "Ø" selects the lower 8K bank for access while position "1" selects the higher 8K bank. Only 8K of the Emulator is accessible to the host in this mode and selection of the desired bank is made manually using the rotary switch. If the board is set for four 4K banks, position "Ø" selects the lowest 4K bank, position "1" the next 4K bank, postion "2" the next 4K bank and postion "3" the highest 4K bank. On the 8Ø32, with the Emulator appearing in the 16K block of the target system from $CØØØ-$FFFF, the following bank configuration is used:

8Ø32 Address	Rotary Switch Position	Target System Address
$9ØØØ-$9FFF	"Ø"	$CØØØ-$CFFF
$9ØØØ-$9FFF	"1"	$DØØØ-$DFFF
$9ØØØ-$9FFF	"2"	$EØØØ-$EFFF
$9ØØØ-$9FFF	"3"	$FØØØ-$FFFF

ADDENDUM TO 16K ROM EMULATOR BOARD

The board provided for use as a FRODO developement system has been specially modified. Another toggle switch has been added to the upper right-hand corner which allows the Emulator to appear to the target system as either 16K bytes of ROM from $C000-$FFFF or two 8K byte ROMS from $A000-$BFFF and $E000-$FFFF. In the 16K mode, the Emulator is used to emulate the Operating System/Basic ROM (OSROM). In the two 8K mode, the Emulator is used to emulate 8K bytes of Operating System ROM (OSROM, from $E000-$FFFF) and 8K bytes of cartridge ROM (CROM, from $A000-$BFFF). When in the two 8K mode, the rotary switch positions "0" and "1" select the OSROM banks and positions "2" and "3" select the CROM banks for the host system. The "128K" dipswitch has no effect.

FRODO EXPANSION CONNECTOR

1	GND	A	GND
2	[redacted] +5	B	+5
3	[redacted] CROM	C	$\overline{IRQ}$
4	[redacted] $\overline{RESET}$	D	R/$\overline{W}$
5	[redacted] Ø2	E	$\overline{NMI}$
6	$\overline{I/O}$	F	A15
7	CB2	[redacted]	
8	CB1	H	A14
9	D7	J	A13
10	D6	K	A12
11	D5	L	A11
12	D4	M	A10
13	D3	N	A9
14	D2	P	A8
15	D1	R	A7
16	D0	S	A6
17	SYNC	T	A5
18	RDY	U	A4
19	6R/$\overline{W}$	V	A3
20	$\overline{RAM2}$	W	A2
21	$\overline{RAM3}$	X	A1
22	GND	Y	A0
		Z	GND

PROTOTYPE ONLY

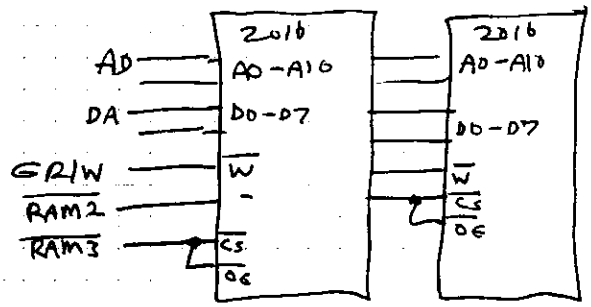
FRODO EXPANDO

1	GND		A	GND	
2	+5	150 ma MAX CURRENT	B	$\overline{\text{CROM}}$	(LS OUTPUT)
3	+5		C	$\overline{\text{RES}}$	(LS OUTPUT)
4	$\overline{\text{IRQ}}$	(O.C. 10K PULL-UP)	D	$\overline{\text{NMI}}$	(O.C. 10K PULL-UP)
5	R/$\overline{\text{W}}$	(MOS W/ 1 LS LOAD)	E	ϕ_2	(LS OUTPUT)
6	$\overline{\text{I/O}}$	(LS OUTPUT)	F	A15	(MOS W/ 1 LS LOAD)
7	$\overline{\text{RAM2}}$	(LS OUTPUT)	H	A14	
8	$\overline{\text{RAM3}}$	(LS OUTPUT)	J	A13	
9	CB2	(MOS)	K	A12	
10	CB1	(MOS)	L	A11	
11	SYNC	(MOS)	M	A10	
12	RDY	(10K PULL-UP)	N	A9	
13	GR/$\overline{\text{W}}$	(LS OUTPUT)	P	A8	
14	D7	(MOS)	R	A7	
15	D6		S	A6	
16	D5		T	A5	
17	D4		U	A4	
18	D3		V	A3	
19	D2		W	A2	
20	D1		X	A1	
21	D0		Y	A0	
22	GND		Z	GND	

HOW TO ADD A RAM CARTRIDGE TO FRODO:

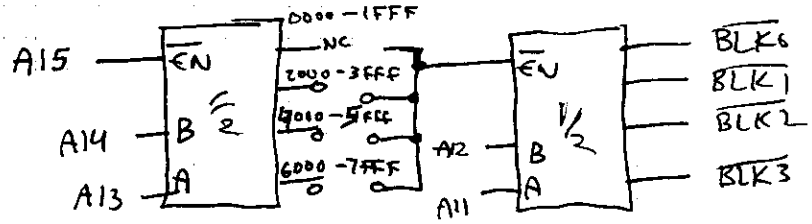
1st 4K:

(EXTENDS SYSTEM TO 8K RAM)



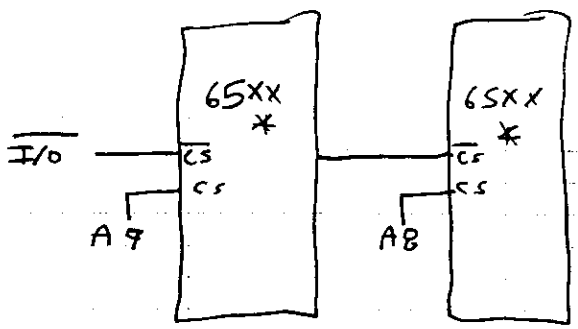
BEYOND 1ST 8K:

74LS139



THIS DECODES INTO A JUMPER SELECTABLE 8K BLOCK WHICH IS THEN DECODED DOWN TO 8K BLOCKS

HOW TO ADD AN I/O CARTRIDGE TO FRODO:

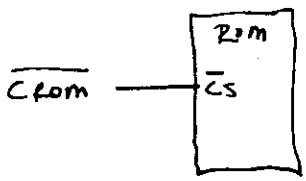


* MUST HAVE BOTH NEGATIVE AND POSITIVE CHIP SELECTS

. . . . ETC DOWN TO A4

CHIPS LIVE AT
9800-980F
9400-940F
9200-920F
9100-910F
9080-908F
9040-904F
9020-902F
9010-901F

HOW TO ADD A ROM CARTRIDGE TO FRODO:



LOADING:

VCS:

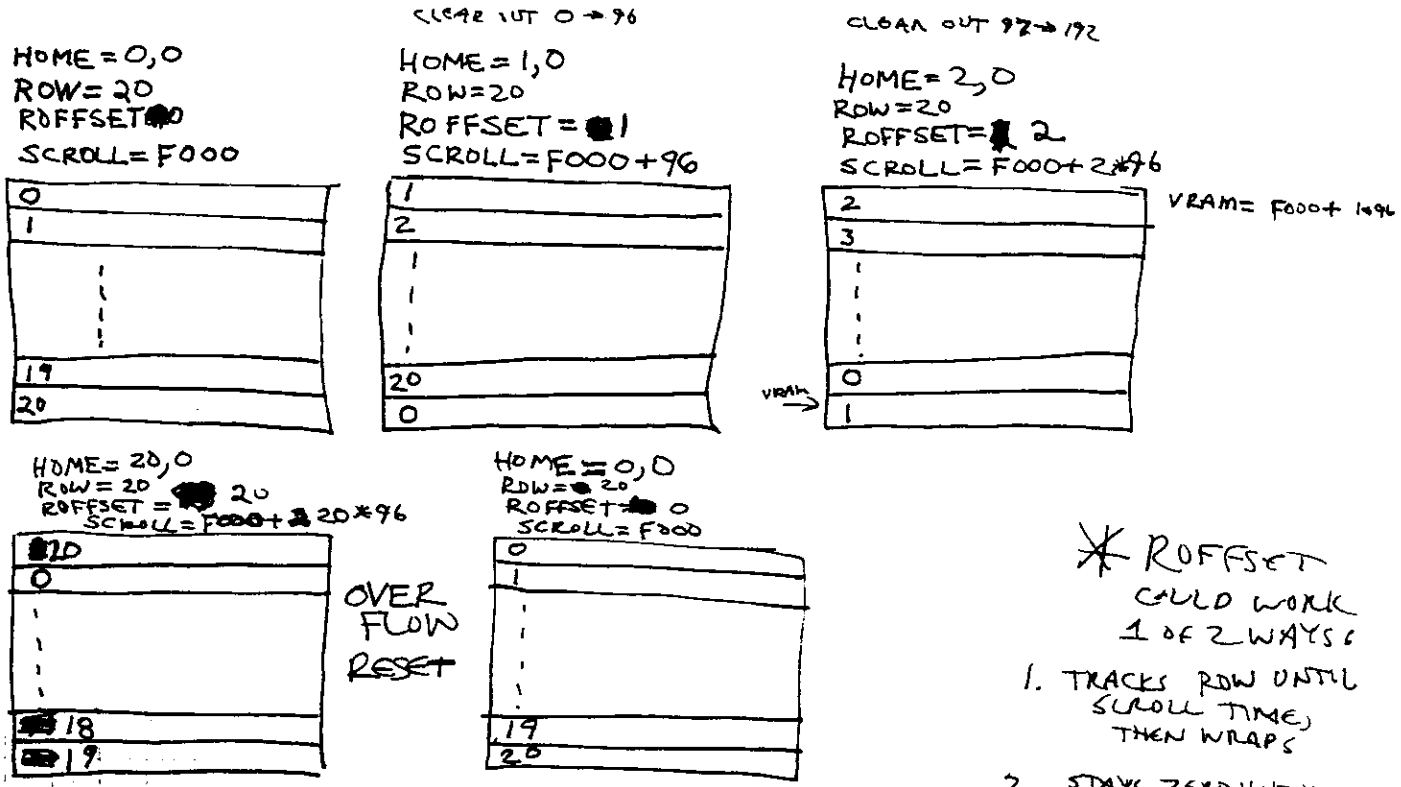
DATA BUS: 1 LS LOAD
ADDR BUS: 1 LS LOAD [redacted] EXCEPT:
A5: 2 LS
A7: 2 LS
A1-A3: 2LS
A12: 2LS, 10K-Ω PULL-UP

FRODO:

DATA BUS: EXPANSION CONNECTOR
ADDR BUS: ~~[redacted]~~ 1 LS LOAD AND EXPANSION CABLE
6522 CA2: 4 LS
R|W: 1 LS

CLEAR SHOULD SET ROW, COL, ROFFSET TO 0 AND SCROLL TO F000

HOME SHOULD SET TO ROFFSET, 0



* ROFFSET COULD WORK 1 OF 2 WAYS:

1. TRACKS ROW UNTIL SCROLL TIME, THEN WRAPS
2. STAYS ZERO UNTIL SCROLL THEN INCREMENTS ON EACH SCROLL AND WRAPS

ROFFSET SHOULD INCREMENT EVERY SCROLL TIME.

RESET OF SCROLL ON OVERFLOW SHOULD RESET ROFFSET, SO DON'T NEED TO KEEP TRACK

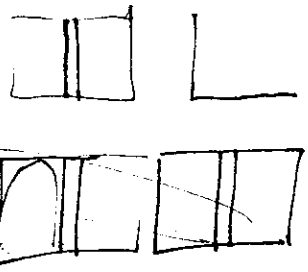
SCROLL

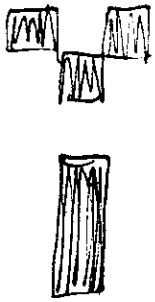
```
        CLC
        LDA SCRNPT
        ADC #96
        BCC NOADD
        INC SCRNPT+1
NOADD   LDA SCRNPT+1
        CMP #
        BNE NRST
        LDA SCRNPT
        CMP #
        BNE NRST
```

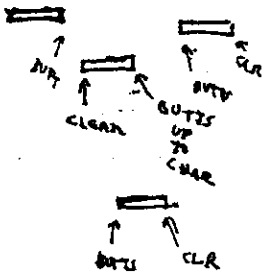
INC ROFFSET

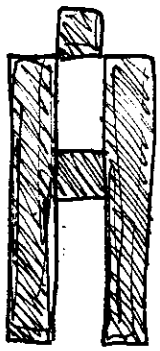
```
        CLC
        LDA SCRNPT
        ADC #96
        BCC NOADD
        INC SCRNPT+1
NOADD   LDA SCRNPT+1
        CMP #
        BNE NRST
```

```
        LDA #F0
        STA SCRNPT
        LDA #0
        STA SCRNPT
        STA ROFFSET
NRST    LDY #95
LINELP  STA (VRAM),Y
        DEY
        BPL LINELP
```

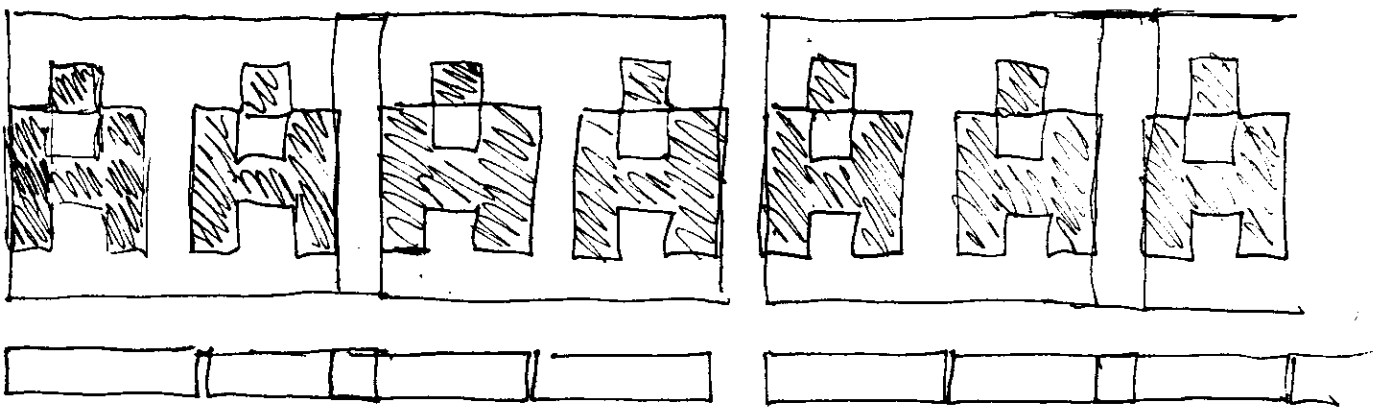


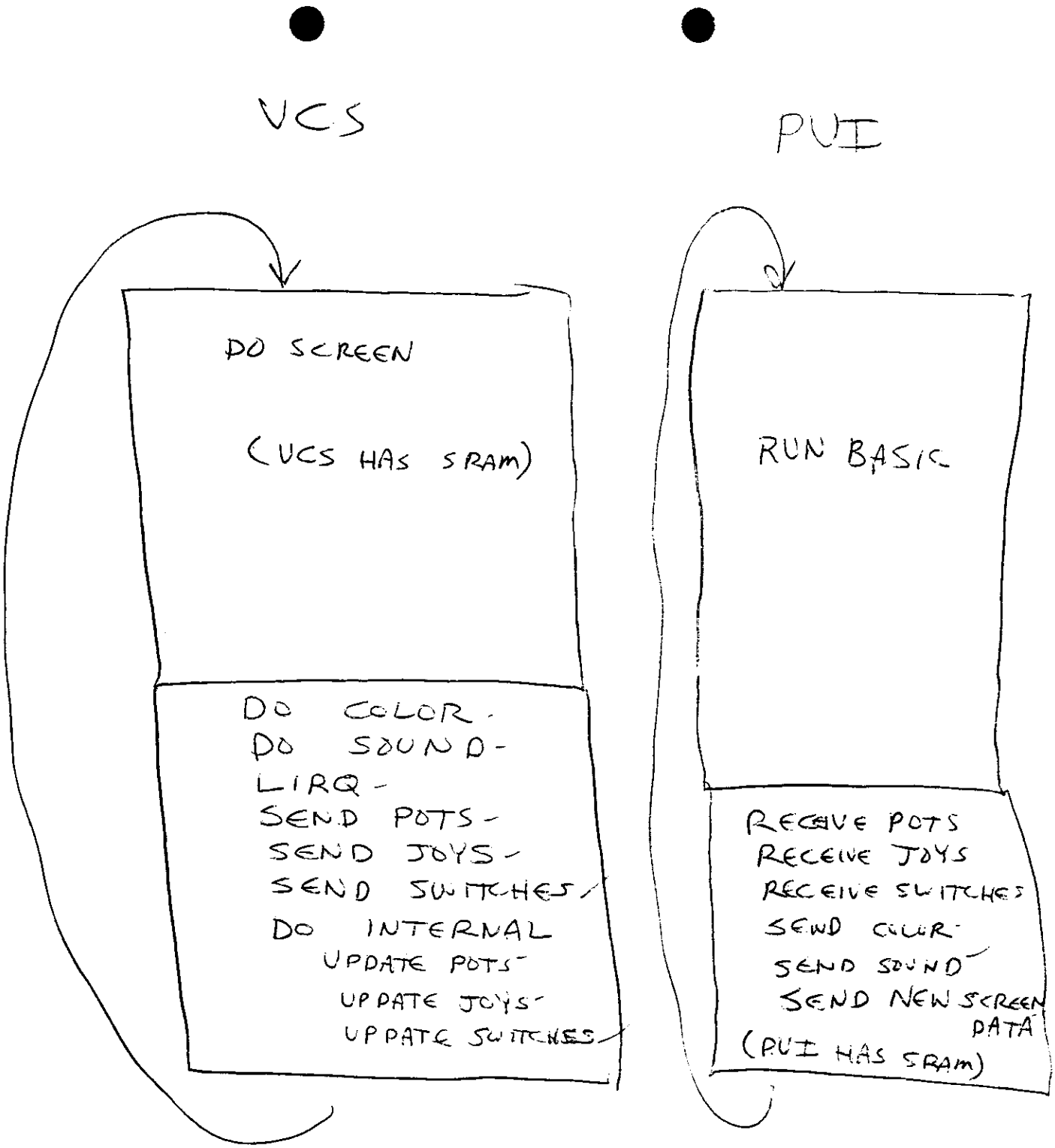


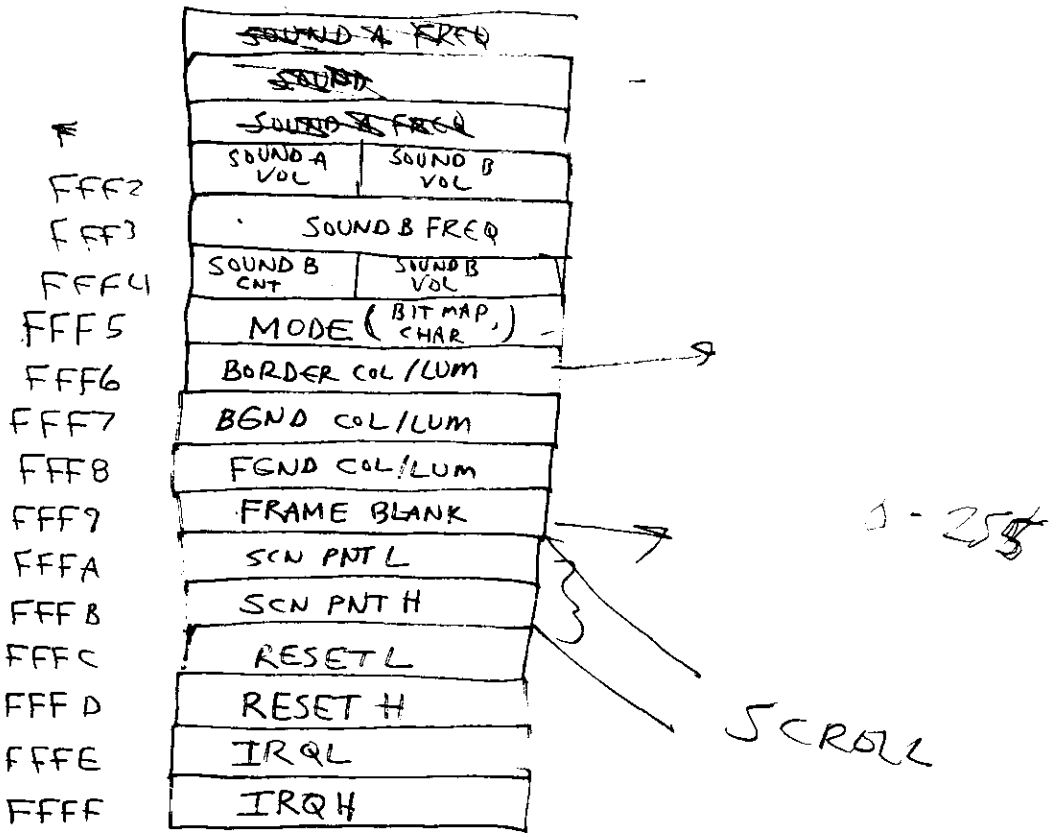




LDA ROW
CMP #20
BNE SKPCLR
LDA #0
SKPCLR CLR
ADC #ROWOFFSET




VCS
PUI
DO SCREEN
(VCS HAS SRAM)
DO COLOR.
DO SOUND-
LIRQ-
SEND POTS-
SEND JOYS-
SEND SWITCHES
DO INTERNAL
UPDATE POTS
UPDATE JOYS
UPDATE SWITCHES
RUN BASIC
RECEIVE POTS
RECEIVE JOYS
RECEIVE SWITCHES
SEND COLOR
SEND SOUND
SEND NEW SCREEN DATA
(PUI HAS SRAM)


~~SOUND A FREQ~~
~~SOUND~~
~~SOUND B FREQ~~
SOUND A VOL
SOUND B VOL
FFF2
FFF3
SOUND B FREQ
SOUND B CNT
SOUND B VOL
FFF4
FFF5
MODE (BIT MAP, CHAR)
FFF6
BORDER COL/LUM
FFF7
BGND COL/LUM
FFF8
FGND COL/LUM
FFF9
FRAME BLANK
FFFA
SCN PNT L
FFFB
SCN PNT H
FFFC
RESET L
FFFD
RESET H
FFFE
IRQL
FFFF
IRQH
SCROLL

1 - 25

IMPORTANT THINGS:

1.) BASIC SHOULD BE ABLE TO SET COLOR/LUM OF FOREGND AND BACKGND (AND BORDER WHEN IN BIT MAP MODE).

2.) There should be two GRAPHICS MODES;
TEXT (USING INTERLEAVED DISPLAY IN WHICH YOU CAN SET FOREGND AND BACKGROUND COLOR/LUM BUT BORDER IS ALWAYS BLACK AND NO PLOTTING IS AVAILABLE)

HIRES (USING FLASHING DISPLAY. FOREGND, BACKGND AND BORDER COLOR/LUM ARE SELECTABLE. PLOTTING IS AVAILABLE IN A 96H X 168V array. Characters can also be printed just as in text mode).

3.) ALL communication between our CPU and VCS should occur at VBLANK time it could go something like this:

		CODE	MEANING
VCS SENDS:	IRQ	ØØ	POT VALUE Ø
POLLED	(IRQ)	NN	(POT VALUE)
	(IRQ)	Ø1	POT VALUE 1
	(IRQ)	NN	(POT VALUE)
	(IRQ)	Ø2	POT VALUE 2
	(IRQ)	NN	(POT VALUE)
	(IRQ)	Ø3	POT VALUE 3
	(IRQ)	NN	(POT VALUE)
	(IRQ)	Ø4	JOYØ VALUE
			JOY1 VALUE
			~~SWITCH STATUS~~
			COLLISION REGS — ? NOT USEFUL IN OUR SYSTEM
			OK F'W DONE

VCS
UPDATE POTS, JOYS, ETC.

OURS
DOWN LOAD INFO INTO SRAM

4.) OUR CPU CAN TELL SOUND GENS WHAT TO DO

FRODO

BASIC

STANDARD MICROSOFT
- MATH PACKAGE
- STRINGS

PLUS GRAPHICS/SOUND ENHANCEMENTS

OR

ATARI SHEPARDSON BASIC

O.S.

SCREEN EDITOR
- AUTO CRSR RPT (RPT ALL KEYS?)
- INS/DEL
- TYPEOVER
- HOME/CLR AND CRSR POSITIONING

DEVICE DRIVERS
- AUDIO CASSETTE
- PRINTER
- HOOKS TO DOS/COMPUTER CONTROLLED MASS STORAGE
- MODEM → MAY BE PLUG-IN ROM OR MAY BE INTELLIGENT PERIPHERAL

,,,,, PERHAPS HP-IL DRIVER IN PLACE OF PRINTER/DOS

FRODO

BASIC ENHANCEMENTS:

1.) 2 GRAPHICS MODES:
   - A.) TEXT
   - B.) BIT MAP
     - 1.) ABILITY TO WRITE TEXT IN BIT MAP MODE
     - 2.) POSSIBLE SPLIT SCREEN?

2.) COLOR - SETCOLOR COMMAND SPECIFY:
   FOREGROUND/BACKGROUND COLOR/LUM
   BORDER

3.) SOUND - SOUND COMMAND SPECIFY:
   - A) WHICH SOUND REG
   - B) PITCH/VOLUME
   - C) AUDIO MODE (1 OF THE VCS MODES)

4.) READ PADDLES - COULD BE REALLY DIFFICULT. MUST BE DIGITIZED BY VCS IN REAL-TIME

5.) READ JOYSTICKS

6.) READ CONSOLE SWITCHES

7.) PLOT, DRAW COMMANDS (WHATEVER CAN BE FIT. IE: PLOT [Ø,1], X,Y TO A,B TO...
   - LOCATE X,Y
   - PAINT [Ø,1] X,Y
   - CIRCLE
   - BOX
   - READ COLORS, GRAPHICSMODE, CRSR POSITION
   - ETC

OTHER FEATURES OF ATARI BASIC OR MICROSOFT COLOR BASIC?

[screen mode] 0 – 24×24 char
1 – bit map

[register to read]

[foreground color/lum]

[background color/lum]

2X [frequency 5 bits
volume 4 bit
modifiers 4 bit]

[border color/lum]

[blank frames]

[scroll/ext scroll]

CSAVE

CLOAD

{BLOAD

~~CLS n,n,n,n mode, foreground, background, border~~

CLS mode

~~COLOR foreground, background, border~~

~~COLOR 1-3, color, luminosity~~

{ PRINT #1, } {LLIST}
{ INPUT #1, } {TERM}
{ OPEN DEV }
{ CLOSE }

Reset	KEY	PAD0 (5)	G5
B/W	BACK	PAD1 (5)	COLOR=1
L	FORE	JOY1 (5)	{SIZE
R	BORDER	JOY2 (5)	{ROT=

SOUND ~~duration~~ freq, mode, volume

CHAR #, "_____"

PLOT 2,2

LINE 1,1,10,10

PRINT @X,Y,~~_____~~

~~DRAW~~ X,Y, "UUU4LLLDDD" B F R

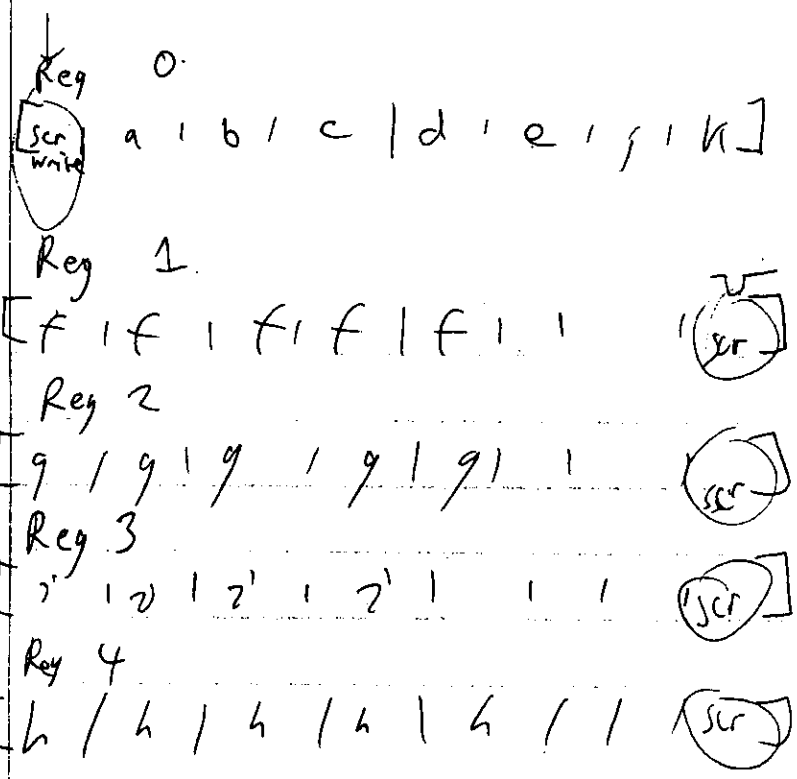
PAINT

GET

PUT

!

a	"Reset"		1
b	B/W /Color"		1
c	Left difficulty		1
d	Right difficulty		1
e	game select		1
~~f~~			
f	Joysticks	1	5
g	Joysticks	2	5
h	Paddle	1	8?
i	Paddle	1	8?
j	Paddle fire		1
k	Paddle fire		1



CSAVE

CLOAD

{BLOAD

~~CLS n,n,n,n mode, foreground, background, border~~

CLS mode

~~COLOR foreground, background, border~~

~~COLOR 1-3, color, luminosity~~

{ ? PRINT #1 } { LLIST }
{ ? INPUT #1 } { TERM }
{ OPEN DEV }
{ CLOSE }

Reset	KEY	PAD0	G5
B/W	BACK	PAD1	COLOR=1
L	FORE	JOY1(5)	{SIZE
R	BORDER	JOY2(5)	ROT=

SOUND ~~duty~~ freq, mode, volume

!line number

CHAR #, "_____"

PLOT 2,2

LINE 1,1,10,10

PRINT @x,y,~~_____~~

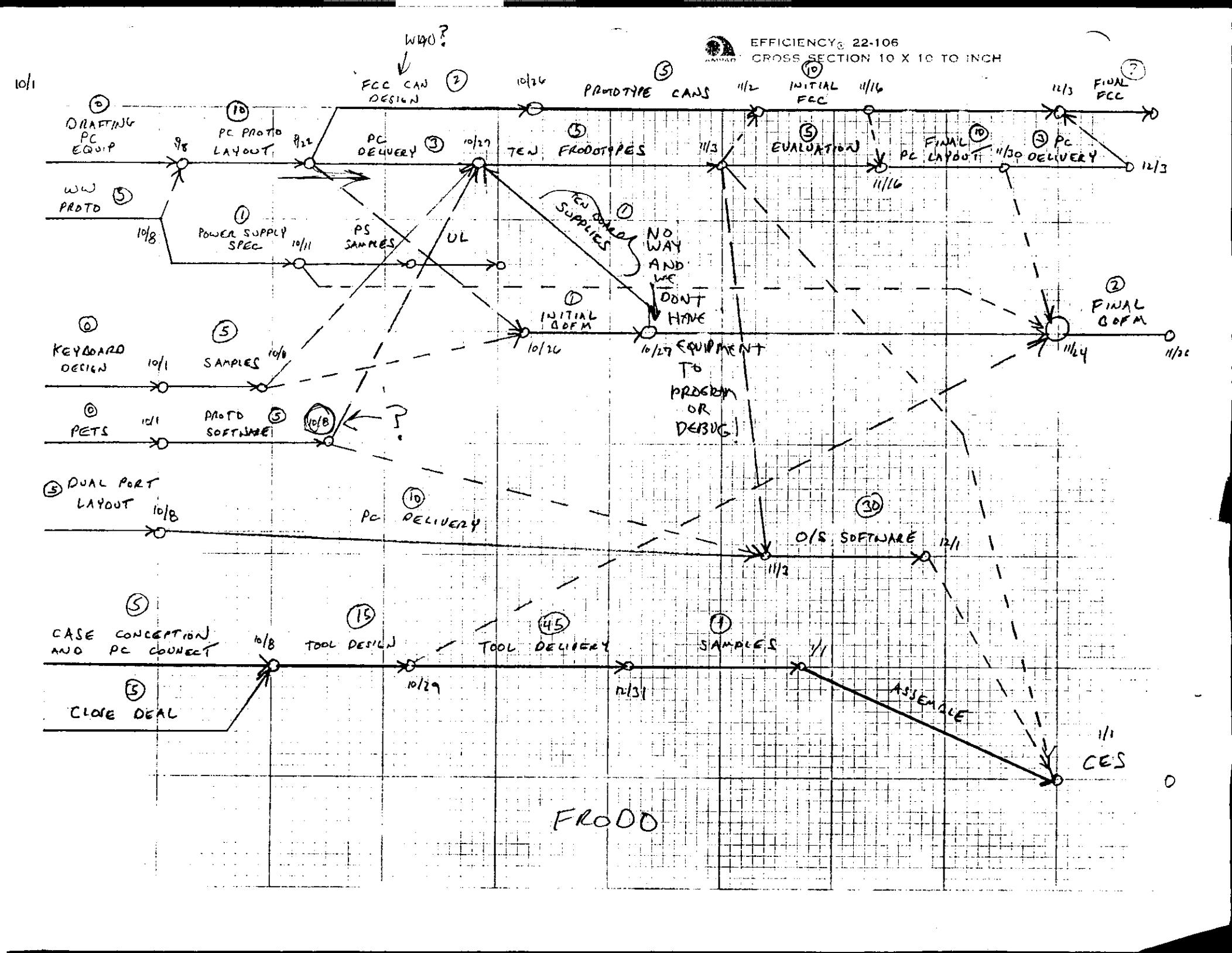
DRAW X,Y, "UUUULLLDDD" B F R

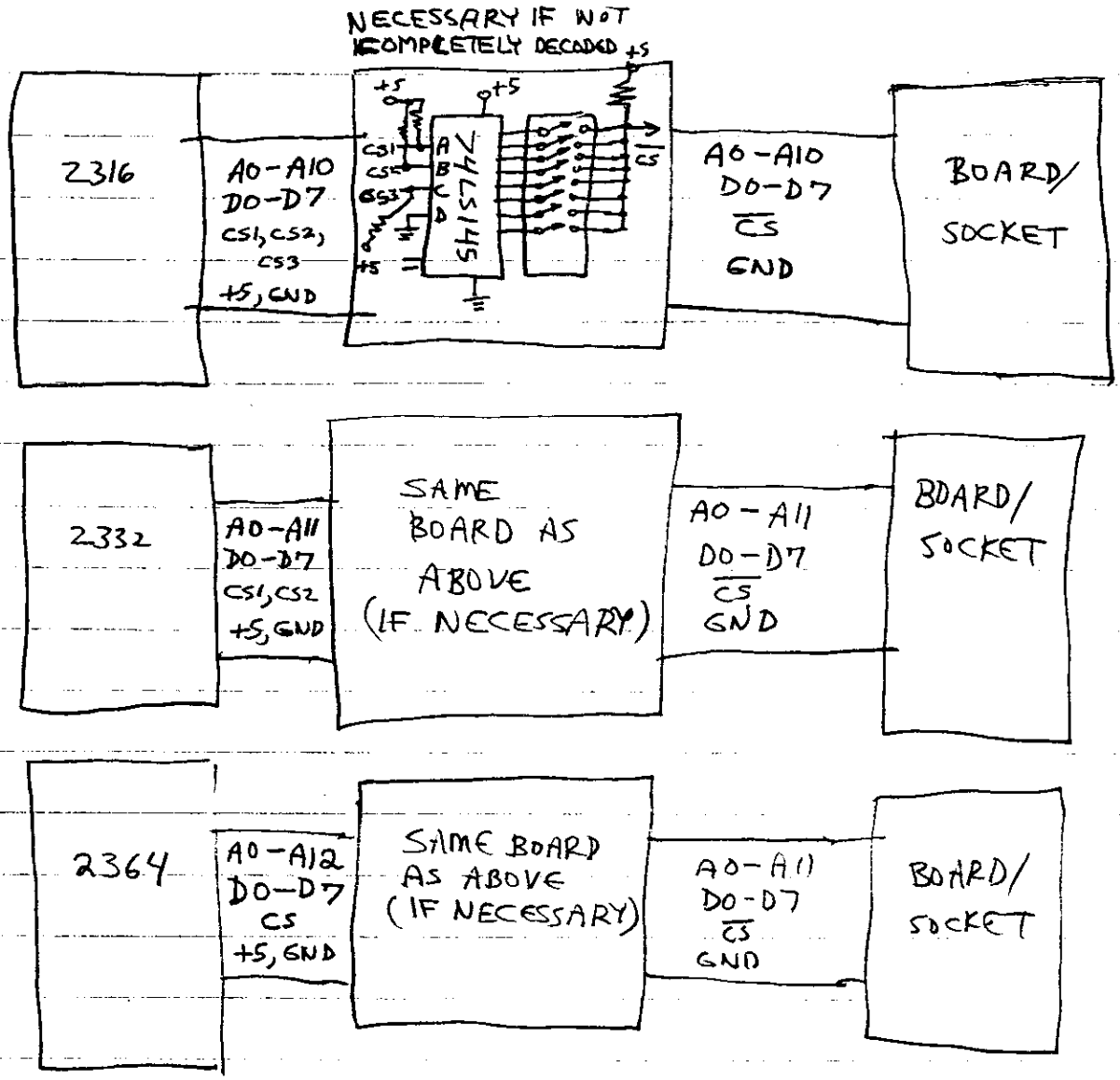
PAINT

GET

PUT

1. VCS *
2. Frodo *
3. Dual port ram board.
4. Development that can assemble Microsoft BASIC.


EFFICIENCY 22-106
CROSS SECTION 10 X 10 TO INCH
10/1
WHO?
FCC CAN DESIGN (2)
10/26
PROTOTYPE CANS (5)
11/2
INITIAL FCC (10)
11/16
FINAL FCC (7)
12/3
(0) DRAFTING PC EQUIP
9/8
(10) PC PROTO LAYOUT
9/22
PC DELIVERY (3)
10/29
TEN PROTOTYPES (5)
11/3
EVALUATION (5)
11/16
FINAL PC LAYOUT (10)
11/30
PC DELIVERY (3)
12/3
WW PROTO (5)
10/8
(1) POWER SUPPLY SPEC
10/11
PS SAMPLES
UL
FCC BOARD SUPPLIES (1)
NO WAY AND WE DONT HAVE
(1) INITIAL DOFM
10/26
10/29 EQUIPMENT TO PROGRAM OR DEBUG
(2) FINAL DOFM
11/24
11/26
(0) KEYBOARD DESIGN
10/1
(5) SAMPLES
10/8
(0) PETS
10/1
PROTO SOFTWARE (5)
10/8
?
(5) DUAL PORT LAYOUT
10/8
PC DELIVERY (10)
(30) O/S SOFTWARE
12/1
11/2
(5) CASE CONCEPTION AND PC CONNECT
10/8
(15) TOOL DESIGN
(45) TOOL DELIVERY
10/29
11/31
(1) SAMPLES
1/1
(5) CLOSE DEAL
ASSEMBLE
1/1
CES
FRODO

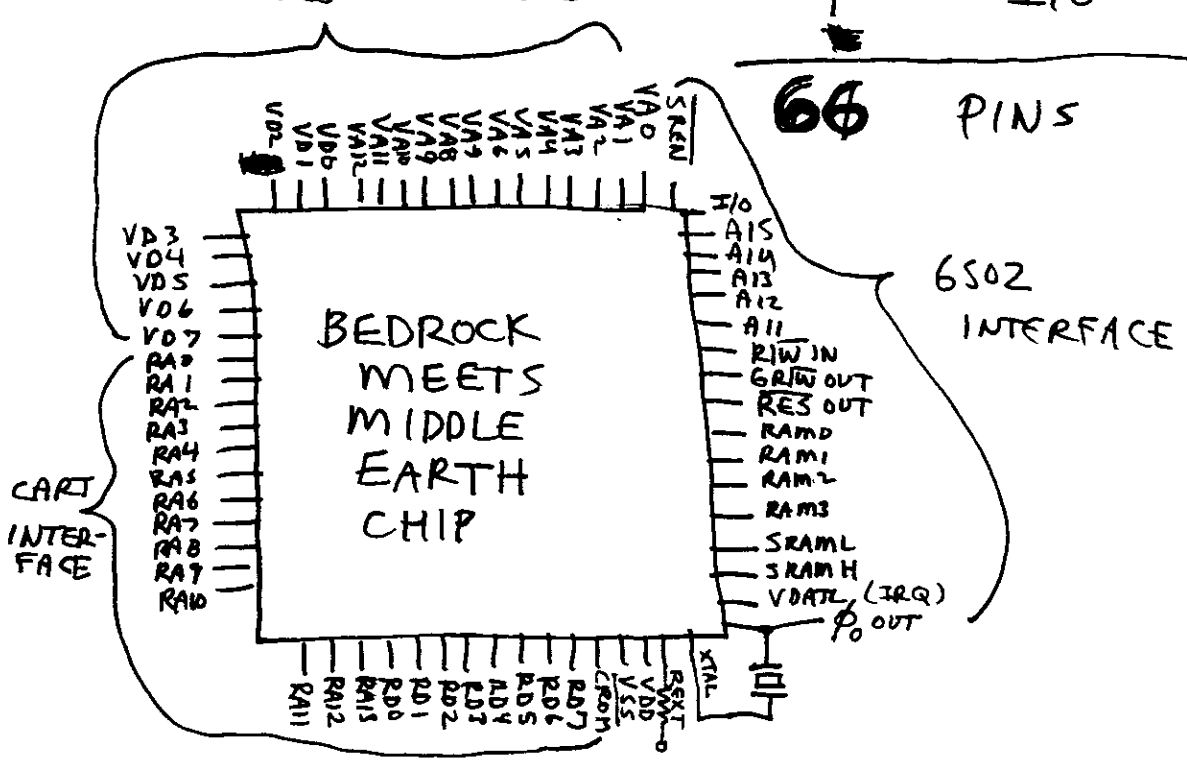

NECESSARY IF NOT COMPLETELY DECODED
2316
A0-A10
D0-D7
CS1, CS2, CS3
+5, GND
+5
CS1
CS2
CS3
A
B
C
D
74LS145
0
1
2
3
4
5
6
7
CS
A0-A10
D0-D7
CS
GND
BOARD/ SOCKET
2332
A0-A11
D0-D7
CS1, CS2
+5, GND
SAME BOARD AS ABOVE (IF NECESSARY)
A0-A11
D0-D7
CS
GND
BOARD/ SOCKET
2364
A0-A12
D0-D7
CS
+5, GND
SAME BOARD AS ABOVE (IF NECESSARY)
A0-A11
D0-D7
CS
GND
BOARD/ SOCKET

FRED/WILMA COMBO

13	VA0 - VA12
14	RA0 - RA13
8	RD0 - RD7
8	VD0 - VD7
1	ϕ_0
1	$\overline{SREN}$
1	Vss
1	VDD
1	REXT
1	VDATL (IRQ)
1	XTAL IN
1	R/$\overline{W}$ IN
1	GR/$\overline{W}$ OUT
1	LINK CS
[redacted]	
1	RAM CS
1	ROM CS
55	PINS

FRED/WILMA/FRODO COMBO

13	VA0-VA12	(FOR VCS ADDR DECODING + MULTIPLEXING
14	RA0-RA13	(BUBBLE ADDR OUTPUT)
8	RD0-RD7	(BUBBLES DATA)
8	VD0-VD7	(VCS DATA)
1	ϕ_0	(USED FOR TIMING, OSC, GR/$\overline{W}$
1	$\overline{SREN}$	(CONTROLS MULTIPLEXING, DECODING AND BUBBLES TRI-STATE)
1	Vss	
1	VDD	
1	REXT	(SETS WRITE STROBE FOR LINK AND REGISTERS)
1	VDATL (IRQ)	(USED TO ALLOW VCS TO INTERRUPT 6502)
1	XTAL IN (osc)	
1	R/$\overline{W}$ IN	
1	GR/$\overline{W}$ OUT	
1	RESET OUT	
5	A11-A15	
1	CROM	
1	RAM0	
1	RAM1	
1	RAM2	
1	RAM3	
1	SRAML	
1	SRAM H	
1	I/O	
66	PINS	



3. STORE IMMEDIATE (command mode 3)
(AUTOMATIC STA GENERATION)

BIT 7 = 0
BIT 6 = INSTRUCTION CHAIN
5-0 = TIA REGISTER

2ND BYTE 8 BITS OF DATA

DOZE → WOF RESERVED

2D - SOFT RESET
2E -
2F -

30-3F → ASSUMES WRITE TO POINTER REGISTERS

BREAKTHRU!!

Berkshire Hotel

(212) 753-5800

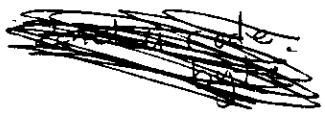
(212) 691-1459

FULL - BUBBLES

COMMAND BYTES

1. GENERATE OP-CODE (command mode 1) BIT 7,6 1st Mcode = 10

5,4 00 = GIVE DATA
01 = RETURN STATUS
10 RESERVED
11 "



3,2,1,0 → OP CODE LIST

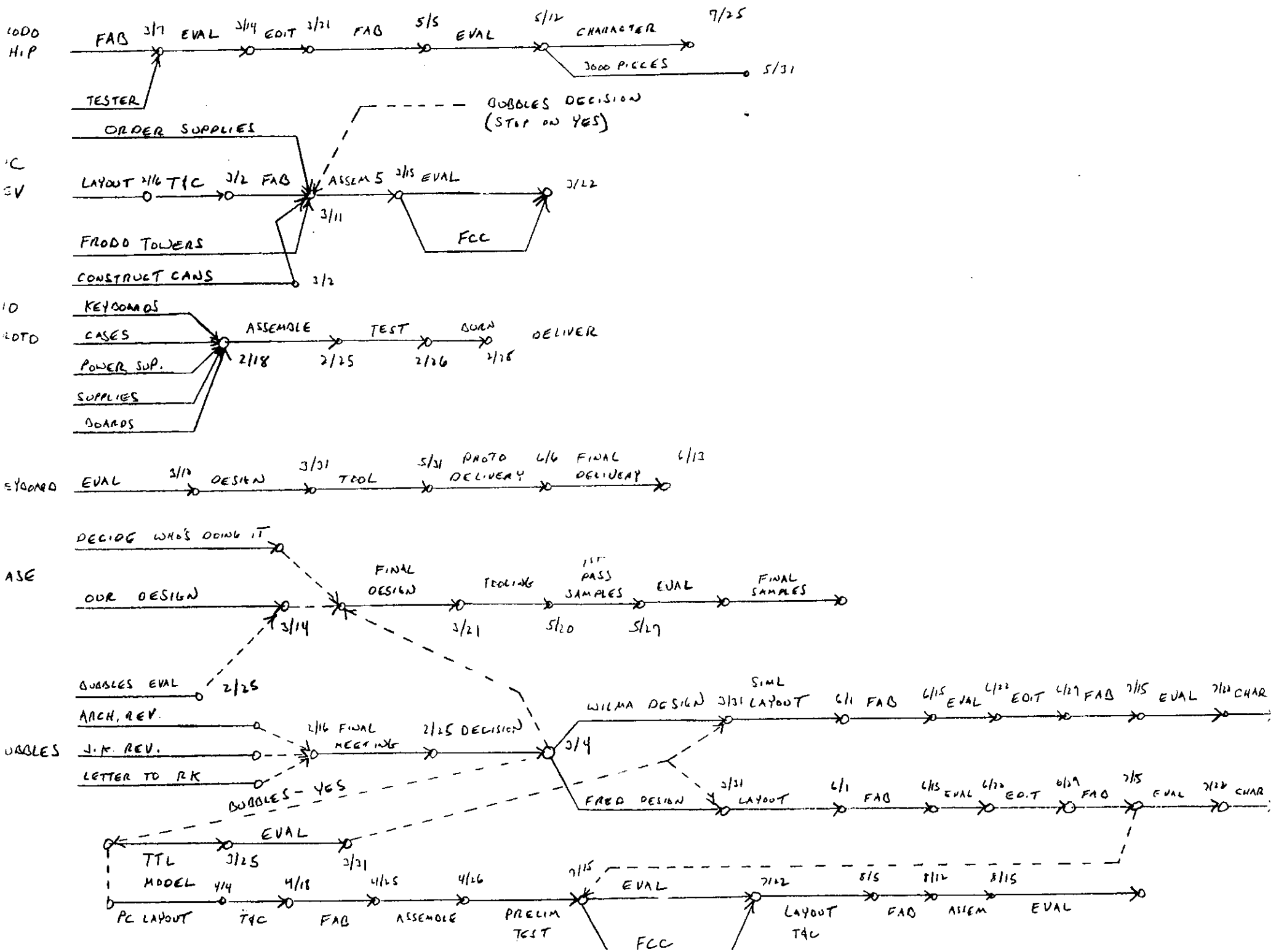
0	LDA#	5	EOR#
1	LDX#	6	ADC #
2	LDY#	7	CMP#
3	ORA #	8	CPX #
4	AND #	9	CPY #
A	SBC#	B-F	UNUSED

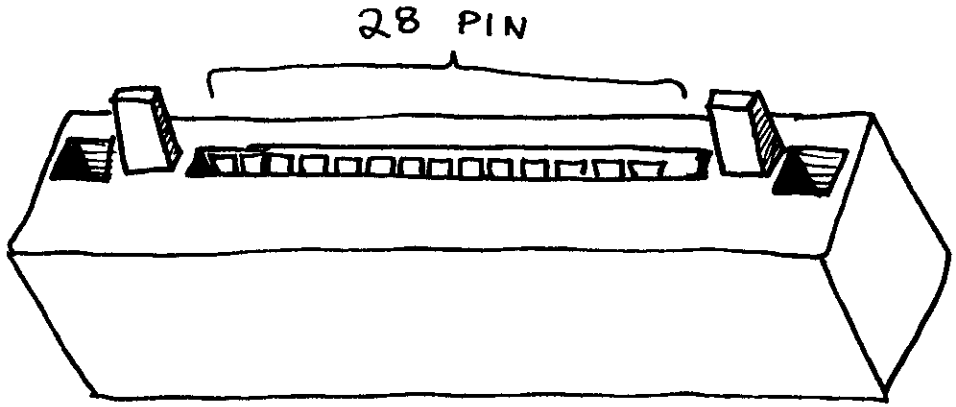
2ND Mcode byte

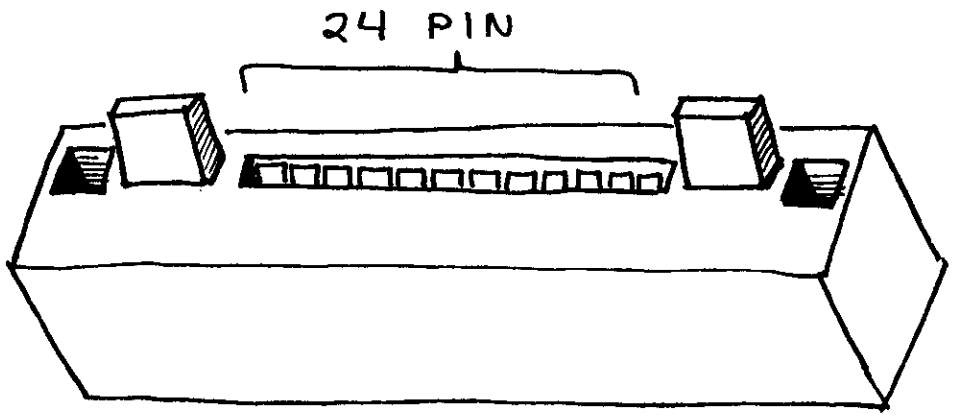
BIT 7 – INSTRUCTION CHAIN (following data is Mcode)
BIT 6 – REVERSE BYTE
BIT 5 – nybble swap
BIT 4 – 0 = bubble 1 = POINTER
BIT 3,2,1,0 = POINTER SELECT
0 POINTER OR DIRECT

2. BUS STUFF (command mode 2) (STA ZERO PAGE AUTO GENERATE)
7,6 1 Mcode = 11
5-0 TIA ADDRESS

2ND Mcode byte same as above


FAB 3/7 EVAL 3/14 EDIT 3/21 FAB 5/5 EVAL 5/12 CHARACTER 7/25
TESTER
3000 PIECES 5/31
BUBBLES DECISION (STOP ON YES)
ORDER SUPPLIES
LAYOUT 2/16 T&C 3/2 FAB
ASSEM 5 3/15 EVAL 3/22
3/11
FCC
FRODO TOWERS
CONSTRUCT CANS 3/2
KEYBOARDS
CASES
POWER SUP.
SUPPLIES
BOARDS
ASSEMBLE 2/18
TEST 2/25
BURN 2/26
DELIVER 2/28
EVAL 3/10
DESIGN 3/31
TOOL 5/31
PROTO DELIVERY 6/6
FINAL DELIVERY 6/13
DECIDE WHO'S DOING IT
OUR DESIGN 3/14
FINAL DESIGN
TOOLING
1ST PASS SAMPLES 5/20
EVAL 5/29
FINAL SAMPLES
BUBBLES EVAL 2/25
ARCH. REV.
J.K. REV.
LETTER TO RK
2/16 FINAL MEETING
2/25 DECISION
3/4
WILMA DESIGN 3/31 LAYOUT 6/1 FAB 6/15 EVAL 6/22 EDIT 6/29 FAB 7/15 EVAL 7/22 CHAR
FRED DESIGN 3/31 LAYOUT 6/1 FAB 6/15 EVAL 6/22 EDIT 6/29 FAB 7/15 EVAL 7/22 CHAR
BUBBLES - YES
TTL MODEL 3/25 EVAL 3/31
PC LAYOUT 4/4 T&C 4/18 FAB 4/25 ASSEMBLE 4/26 PRELIM TEST
7/15 EVAL 7/22 LAYOUT T&C 8/5 FAB 8/12 ASSEM 8/15 EVAL
FCC


28 PIN


24 PIN

PLA

$\overline{LINK} = A15 \cdot \overline{A14} \cdot \overline{A13} \cdot A12 \cdot \overline{A11}$ (9000-9FFF)

$\overline{CROM} = A15 \cdot \overline{A14} \cdot A13$ (A000-BFFF)

$\overline{RAM2} = \overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot A12 \cdot \overline{A11}$ (1000-17FF)

$\overline{RAM3} = \overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot A12 \cdot A11$ (1800-1FFF)

$\overline{I/O} = A15 \cdot \overline{A14} \cdot \overline{A13} \cdot A12 \cdot A11$ (9800-9FFF)

$\overline{RAM1} = \overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot \overline{A12} \cdot \overline{A11}$ (0800-0FFF)

$\overline{RAM\phi} = \overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot \overline{A12} \cdot \overline{A11}$ (0000-07FF)

$\overline{SRAML} = A15 \cdot \overline{A14} \cdot \overline{A13} \cdot \overline{A12} \cdot \overline{A11} \cdot SREN + VA12 \cdot \overline{VA11} \cdot \overline{SREN}$ (8000-87FF +)

$\overline{SRAMH} = A15 \cdot \overline{A14} \cdot \overline{A13} \cdot \overline{A12} \cdot A11 \cdot SREN + VA12 \cdot VA11 \cdot \overline{SREN}$ (8800-8FFF +)

$VCSEL = \overline{VA12} \cdot \overline{VA7} \cdot VA5 \cdot VA3 \cdot VA2 \cdot VA1$

	1	A11	23	REXT	✓
	2	A12	24	RESET	✓
✓	3	A13	25	VDATL	✓
	4	A14	26	ϕ_2 IN	✓
	5	A15	27	VSS	✓
			28	V_{DD}	✓
	6	VA12			
	7	VA11			
✓	8	VA7			
	9	VA5			
	10	VA3			
	11	VA2			
	12	VA1			
✓	13	SREN			
OUT1	14	LINK			✓
OUT2	15	CROM			✓
OUT3	16	RAM2			✓
OUT4	17	RAM3			✓
OUT5	18	I/O			✓
OUT6	19	RAM1			✓
OUT7	20	RAM0			✓
OUT8	21	SRAML			✓
OUT9	22	SRAMH			✓

FRODO CHIP (INTERNAL MATRIX)

$\overline{LINK} = \overline{A15} + A14 + A13 + \overline{A12} + A11$

$\overline{CROM} = \overline{A15} + A14 + \overline{A13}$

$\overline{RAM2} = A15 + A14 + A13 + \overline{A12} + \overline{A11}$

$\overline{RAM3} = A15 + A14 + A13 + \overline{A12} + \overline{A11}$

$\overline{I/O} = \overline{A15} + A14 + A13 + \overline{A12} + \overline{A11}$

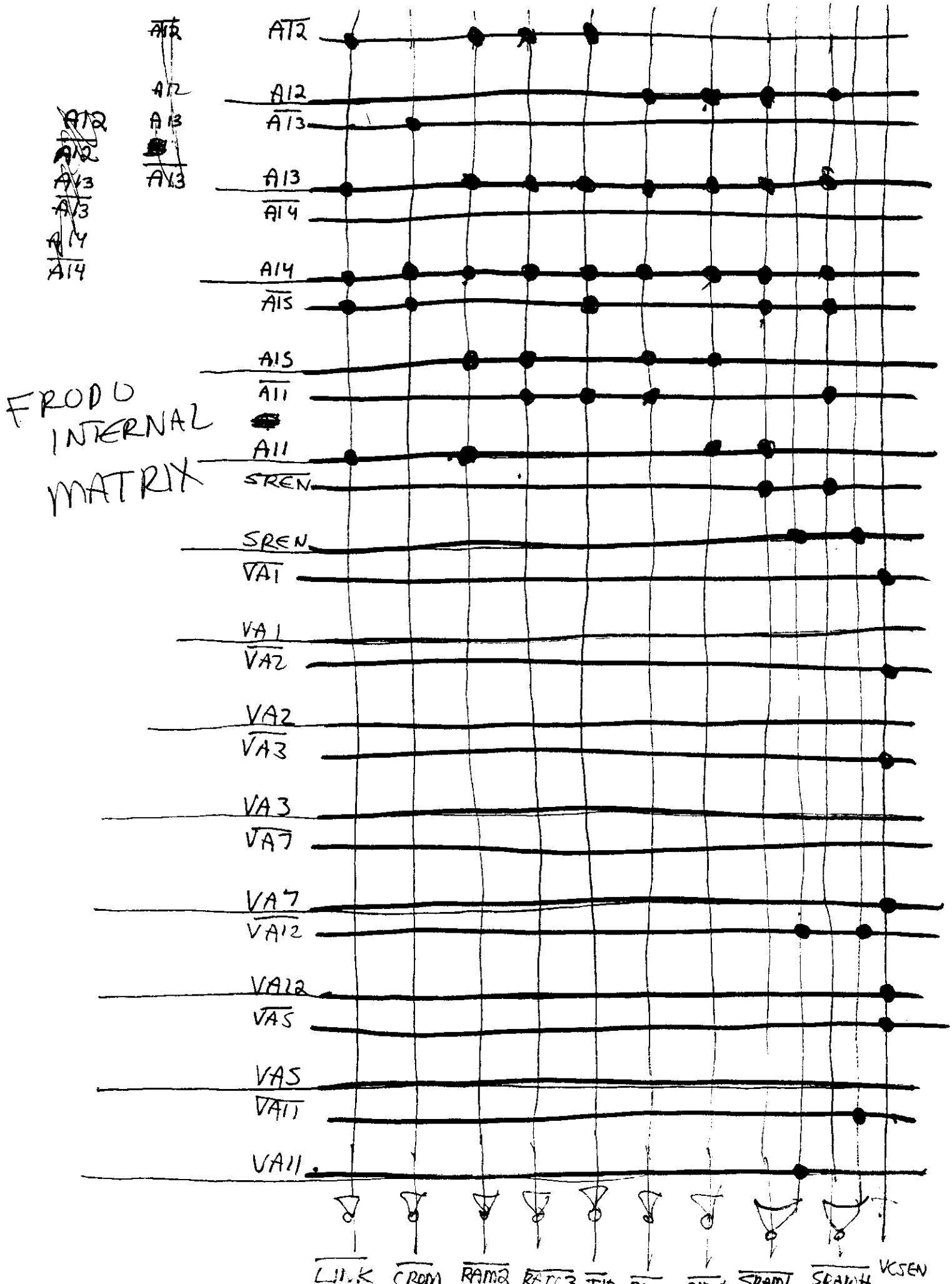
$\overline{RAM1} = A15 + A14 + A13 + A12 + \overline{A11}$

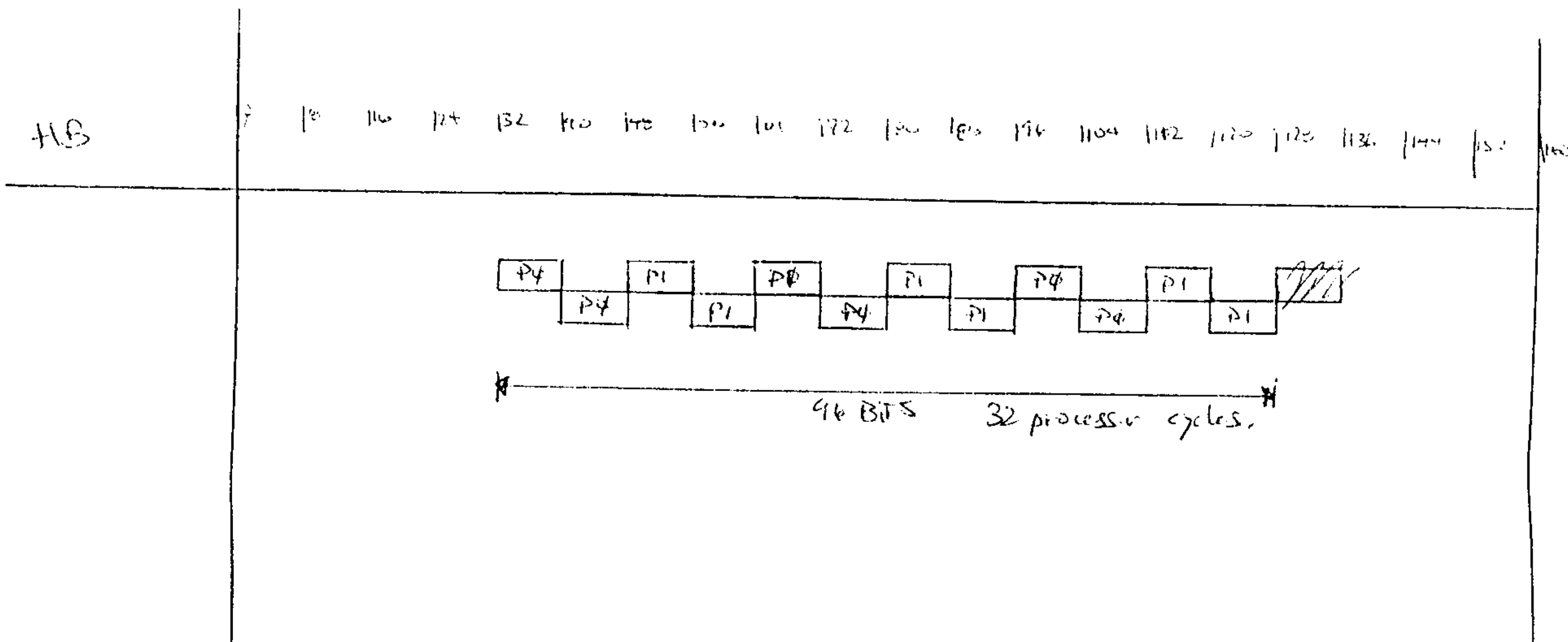
$\overline{RAM\phi} = A15 + A14 + A13 + A12 + A11$

$\overline{SRAML} = \overline{A15} + A14 + A13 + A12 + A11 + \overline{SREN} \cdot \overline{VA12} + VA11 + SREN$

$\overline{SRAMH} = \overline{A15} + A14 + A13 + A12 + \overline{A11} + \overline{SREN} \cdot \overline{VA12} + \overline{VA11} + SREN$

$VCSEL = VA12 + VA7 + \overline{VA5} + \overline{VA3} + \overline{VA2} + \overline{VA1}$


FRODO
INTERNAL
MATRIX
A12
A13
A14
A15
A11
SREN
VA1
VA2
VA3
VA7
VA12
VA5
VA11
VCSEN


HB
96 BITS
32 processor cycles.

AUDIO:

CHANNEL # 04 PIN 13

TOP CLOCK (MHz) B2 2XHSYNC

Φ	NOTHING
1	4BIT POLY CTR 400 μsec
2	SLOWER CLOCK TO 4 BIT POLY ~~7.5~~ 7.4usec period ~ ÷15 SOUNDS RIGHT
3	BIZARRE ~~RES~~ NO SLNGLE BITS. (POLY CLOCKING POLY?)
4	÷2
5	÷2
6	~~÷31 (15.5 X2)~~ ÷15.5
7	POLY COUNTER PERIOD 31 HSYNCS 5BIT POLY ÷2
8	LONG POLY (9 BIT) PERIOD OF 511 BMS (511 × 63μsec = 30msec?)
9	5 BIT POLY COUNTER
A	~~LIKE E DIFFERENT DUTY CYCLE~~ ÷15.5
B	ALL 1's SET
C	DIVID BY 3 CLEARS TOGGLES IN HALF CYCLES
D	SAME AS C
E	÷ 45.5
F	5 BIT POLY PATTERN, ~~SPARES~~ ÷3

SET

$\phi 9 = 0$
$\phi 8 = 2$
$\phi 7 = 4$
$\phi 6 = 8$

L2 = PIN 7
L1 = PIN 5
Lϕ = PIN 3

CS1B	OK	Pϕ
CS1C	OK	P1
CS1D	OK	Mϕ
CS1E	OK	M1
CS1F	OK	BL
CSϕD	OK	PF2
CS0E	OK	PF1
CS0F	OK	PFϕ

Pϕ P1 Mϕ M1 BL
PF

COLLISION MATRIX

X0	M0·P1	M1·Pϕ
X1	M1·Pϕ	Mϕ·P1
X2	Pϕ·PF	Pϕ·BL
X3	P1·PF	P1·BL
X4	Mϕ·PF	Mϕ·BL
X5	M1·PF	M1·BL
X6	BL·PF	X
X7	Pϕ·P1	Mϕ·M1

LOOKS RIGHT

VDELAY

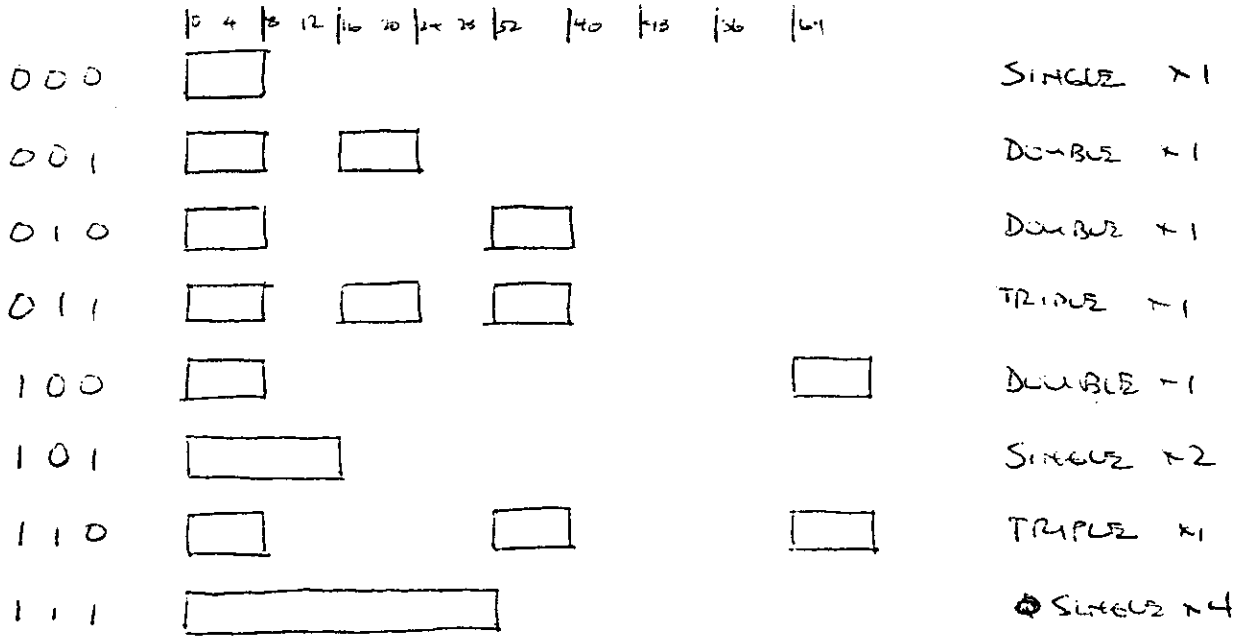
Pϕ STROBED BY P1
P1 STROBED BY Pϕ
BL STROBED BY P1

MSB OF VBLANK COUNTS PAT IMAGES

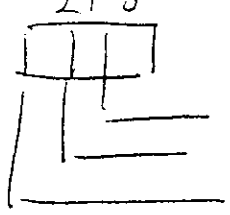
BITS [5,4] OF $04, $05, $0A SET SIZE OF 1 BIT OBJECT

00	1 clock
01	2 clocks
10	4 clocks
11	8 clocks

BITS [2,1,0] SET NUMBER/SIZE OF PLAYER



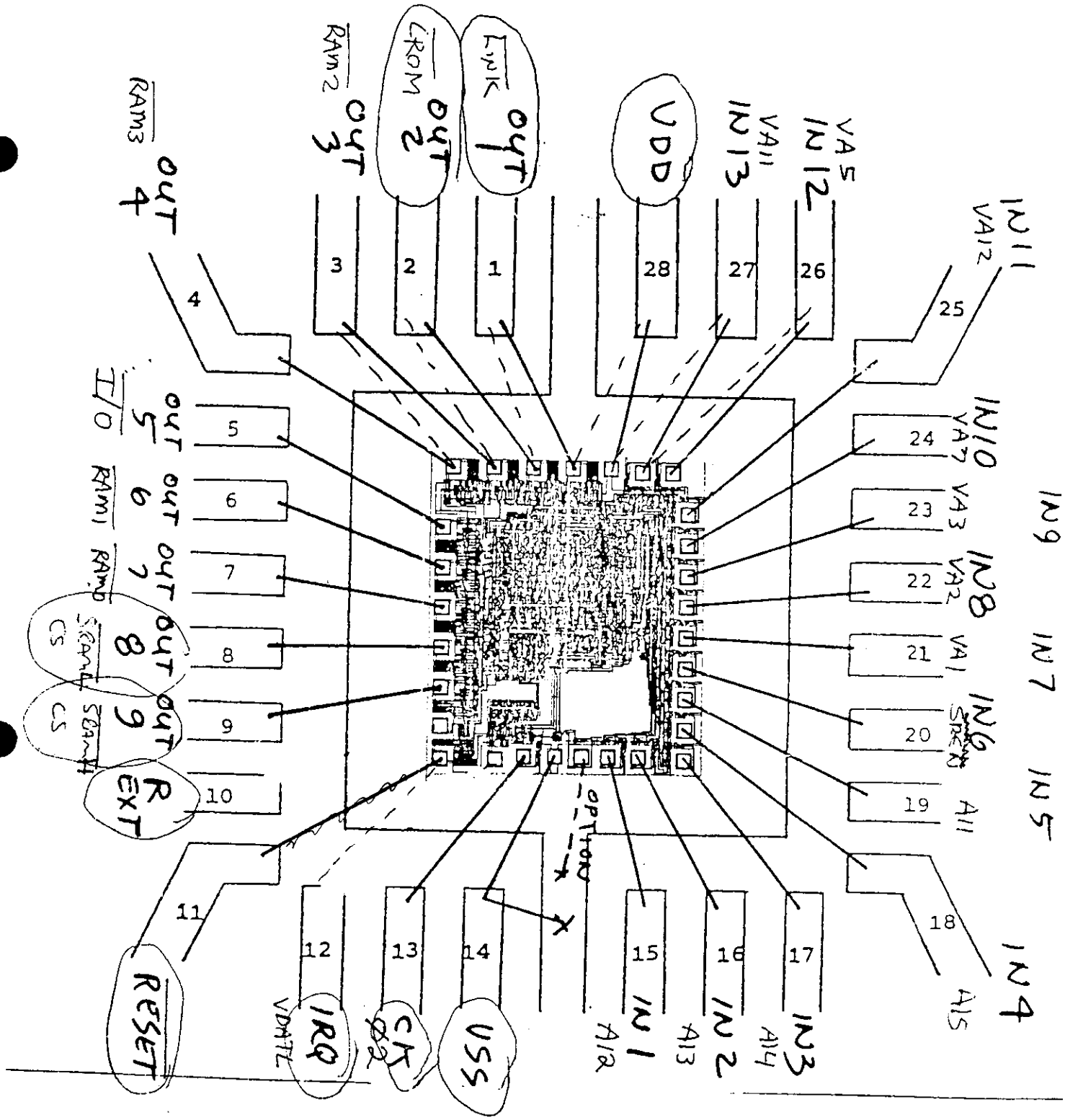
~~CTRL~~ REFP CTRL



REFLECT (=1) NORMAL (=0)
SCORE (=1)
PRIORITY (=1) OVER PLAYERS

WRITE ADDRESS SUMMARY.

ADDRESS	7 6 5 4 3 2 1 0	NAME	SIMPLE DESCRIPTION
00		VSYNC	VERTICAL SYNC
01		VBLANK	VERTICAL BLANK, DISCHARGES CAPS.
02	— STROBE —	WSYNC	HALT PROCESSOR UNTIL HSYNC
03	— STROBE —	RESET	RESET HSYNC COUNTER
04		NUSIZ0	SIZE & MISSILES / NUMBER & SIZE OF PLAYER 0
05		NUSIZ1	" " " " " " 1
06		COLUP0	COLOR / LUMINANCE PLAYER 0
07		" P1	PLAYER 1
08		" PF	PF
09		" BK	BACKGROUND.
0A		CTRLPF	BALL SIZE / PF: PRIORITY, COLOR, REFLECT
0B		REFP0	REFLECT P0
0C		REFP1	REFLECT P1
0D	7 6 5 4	PF2	PLAYFIELD 2
0E	7 6 5 4 3 2 1 0	PF1	1
0F	7 6 5 4 3 2 1 0	PF2	0
10	— Strobe —	RESP0	RESET HORIZONTAL POSITION P0
11	— strobe —	P1	RESET HORIZONTAL POSITION P1
12	— strobe —	M0	M0
13	— strobe —	M1	M1
14	— strobe —	BL	BL
15		AUDC0	AUDIO CONTROL 0
16		" 1	" " 1
17		AUDF0	AUDIO FREQUENCY 0
18		" 1	" " 1
19		AUDV0	AUDIO VOLUME 0
1A		" 1	" " 1
1B		GRP0	GRAPHICS P0
1C		GRP1	P1
1D		GRM0	M0
1E		GRM1	M1
1F		GRBL	BL
20		HMP0	HORIZONTAL MOTION P0
21		HMP1	P1
22		HMM0	M0
23		HMM1	M1
24		HMBL	BL
25		VDELP0	Varied Delay P0
26		VDELP1	" " P1
27		VDELBL	" " BL
28		RMP0	Reset missle to player 0
29		RMP1	" " " 1
2A	— Strobe —	HMOVE	HORIZONTAL MOVE
2B	— STROBE —	HMCLR	HORIZONTAL MOTION CLEAR
2C	— STROBE —	CXCLR	CLEAR COLLISIONS.



SCALE: 20X

THIS [illegible] BONDING DIAGRAM

NO. _____ FORMS A PART OF

[illegible] NO. _____ AND WILL BE USED

IN PLACE OF CUSTOMER'S P/O NO. _____

ORIGINATOR: ICS

CUSTOMER: PVI

DEVICE TYPE: _____

PACKAGE TYPE: 28 Leads Plastic

DIE SIZE: 118 X 101 ~

PAD SIZE: 150 X 150

APPROVAL:

ENG: _____

OP : _____

QA : _____

EFF DATE: 1/5/

IEI FORM 0220-1331

OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	4.75	5.00	5.25	V
I_{OH}	High Level Output Current			400.0	μA
I_{OL}	Low Level Output Current			-1.60	mA
V_{IH}	High Level Input Voltage	2.00			V
V_{IL}	Low Level Input Voltage			.80	V
I_{CC}	Supply Current			40.00	mA
T_A	Operating Free Air Temp.	0		70°	C

DC ELECTRICAL CHARACTERISTICS - INPUTS
SA_X, VA_X, SREN, ϕ_2, I/O

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High Level Input Voltage		2.0		V
V_{IL}	Low Level Input Voltage			.8	V
I_{IH}	High Level Input Current	V_{CC} = MAX V_I = 2.4V		400.0	μA
I_{IL}	Low Level Input Current	V_{CC} = MAX V_I = .4V		-1.6	mA

DC ELECTRICAL CHARACTERISTICS - OUTPUTS

T_{SC}, FA12, ROM CS, SA_X (1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High Level Output Voltage	I_{OH} = 400.0μA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		.4	V
I_{OH}	High Level Output Current	V_{OH} = 2.4 V		400.0	μA
I_{OL}	Low Level Output Current	V_{OL} = .4 V		-1.6	mA

VD_X (2), (3)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High Level Output Voltage	I_{OH} = -25 mA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 25 mA		.8	V
I_{OH}	High Level Output Current	V_{OH} = 2.4V	25.00		mA
I_{OL}	Low Level Output Current	V_{OL} = .6V		-25.00	mA
I_{OZ}	Tri State Leakage Current			1.00	μA

NOTES

1. CL = 10pf (Load Capacitance)
2. CL = 25pf (Load Capacitance)
3. 10K - 25K Internal Pullup

6502

```
1000   SEI
       CLD
       LDX #FF
       TXS
       STX [redacted] 9E02
       INX
       STX [redacted] 9E00
       LDA #4
       STA [redacted] 9E03
       LDA #FE
       STA [redacted] 9E01
LP1    LDA 1800,X
       STA 8000,X
       INX
       BNE LP1
       LDA #0
       STA 8FFC
       LDA #F0
       STA 8FFD
       LDA #F6
       STA [redacted] 9E01
LP2    BIT [redacted] 9E01
       BPL LP2
       LDA 9E00
       LDA 9000
       CMP #AA
       BNE LP2
       [redacted]
LP3    BIT 9E01
       BPL LP3
       LDA 9E00
       [redacted]
       [redacted]
       [redacted]
       CPX 9000
       BEQ SKP1
       LDA #FF
SKP1   STA
```

```
       LDA 9000
       CMP #AA
       BNE LP2
LP4    BIT 9E01
       BPL [redacted] LP4
       LDA 9E00
       LDA #0
       CPX 9000
       BEQ SKP1
       LDA #FF
SKP1   STA 9E02
       [redacted]
       LDA 9000
       STA 1900,X
       INX
       BNE LP4
       BEQ LP2
```

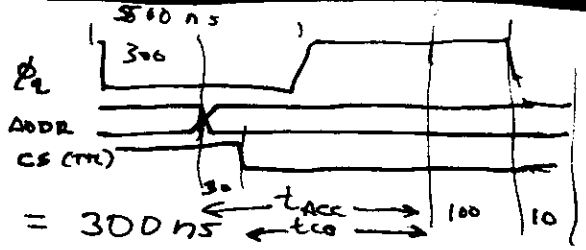
6507

```
1800   SEI
       CLD
       LDX #FF
       TXS
       STX 0281
       [redacted]
       INX
       STX 90
LP1    LDA #AA
       STA 3F
       JSR DELAY
       LDA #AA
       STA 3F
       JSR DELAY
LP2    LDA 90
       STA 3F
       [redacted]
       JSR DELAY
```

```
DELAY  LDX #35
       LDY #0
LP3    DEY
       BNE LP3
       DEX
       BNE LP3
       RTS
```

INC 90
BNE LP1
BEQ LP

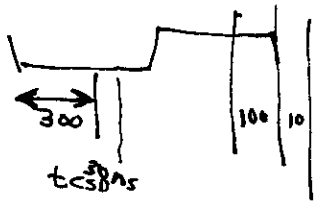
ϕ_2 = 1000 ns



6502 ADDR WORST CASE SET UP = 300 ns
6502 DATA STABLE BEFORE FALL OF ϕ_2 = 100 ns
DATA HOLD AFTER ϕ_2 = 10 ns

ROM

∴ ROM ACCESS TIME < 600 ns
20% ROM ACCESS < 480 ns



(*) TEST FOR ROM ACCESS ≤ 480

(*) IF 23128 USED, TEST FOR TCO ≤ 480 (TOE)

(*) IF 2364's USED TEST FOR TCO ≤ 450

(*) ELECTRICAL LEVELS: TTL, 5V SUPPLY

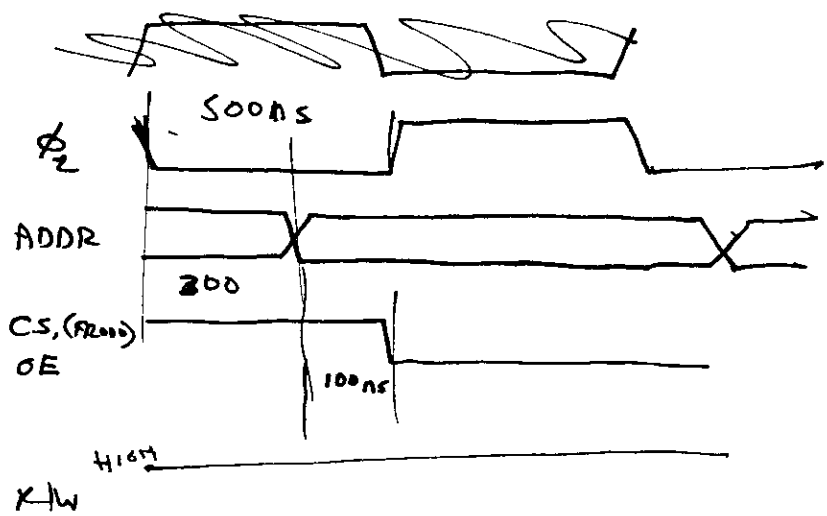
(*) I_{IC} MAX 250 for 23128
125 for 2364

(*) TEST FOR 10 ns HOLD from ADDR CHANGE

(*) CYCLE TIME = 1000 ns

SYSTEM RAM

READ ACCESS



(*) CYCLE TIME ≤ 1000 ns

(*) TACC ≤ 480

(*) TCO ≤ 400
(TOE ≤ 400)

(*) TOH ≥ 10 ns (from ADDR CHANGE)

WRITE

(*) T_{WP} = 480 ns min
500 ns max

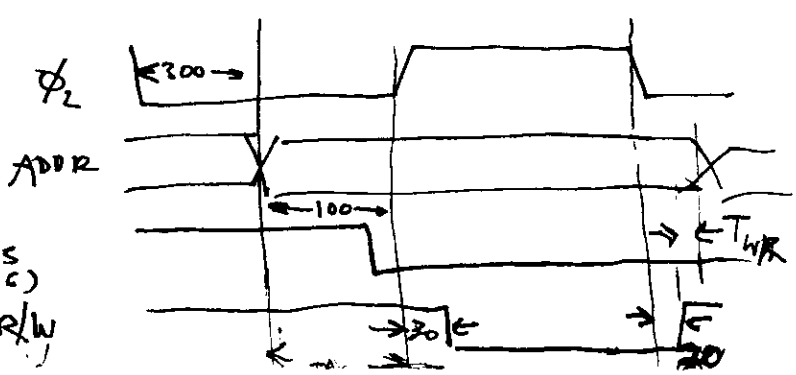
(*) T_{AS} min 160

(*) T_{CW} min = 480

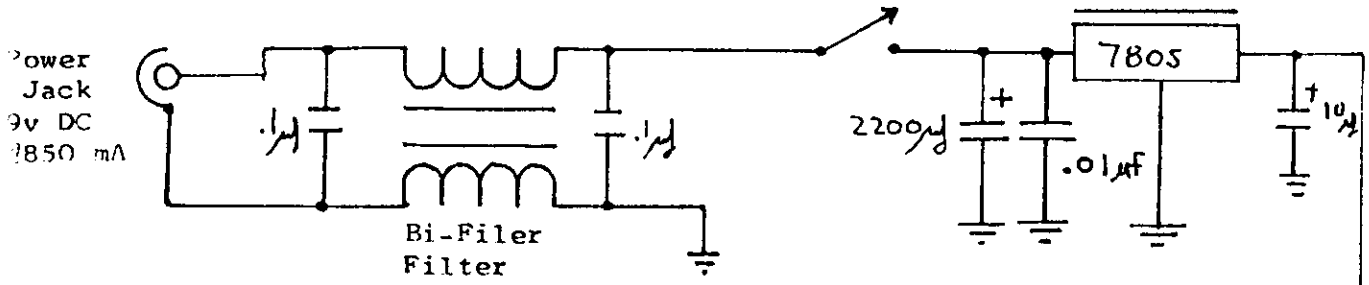
(*) T_{WR} min = 10 ns

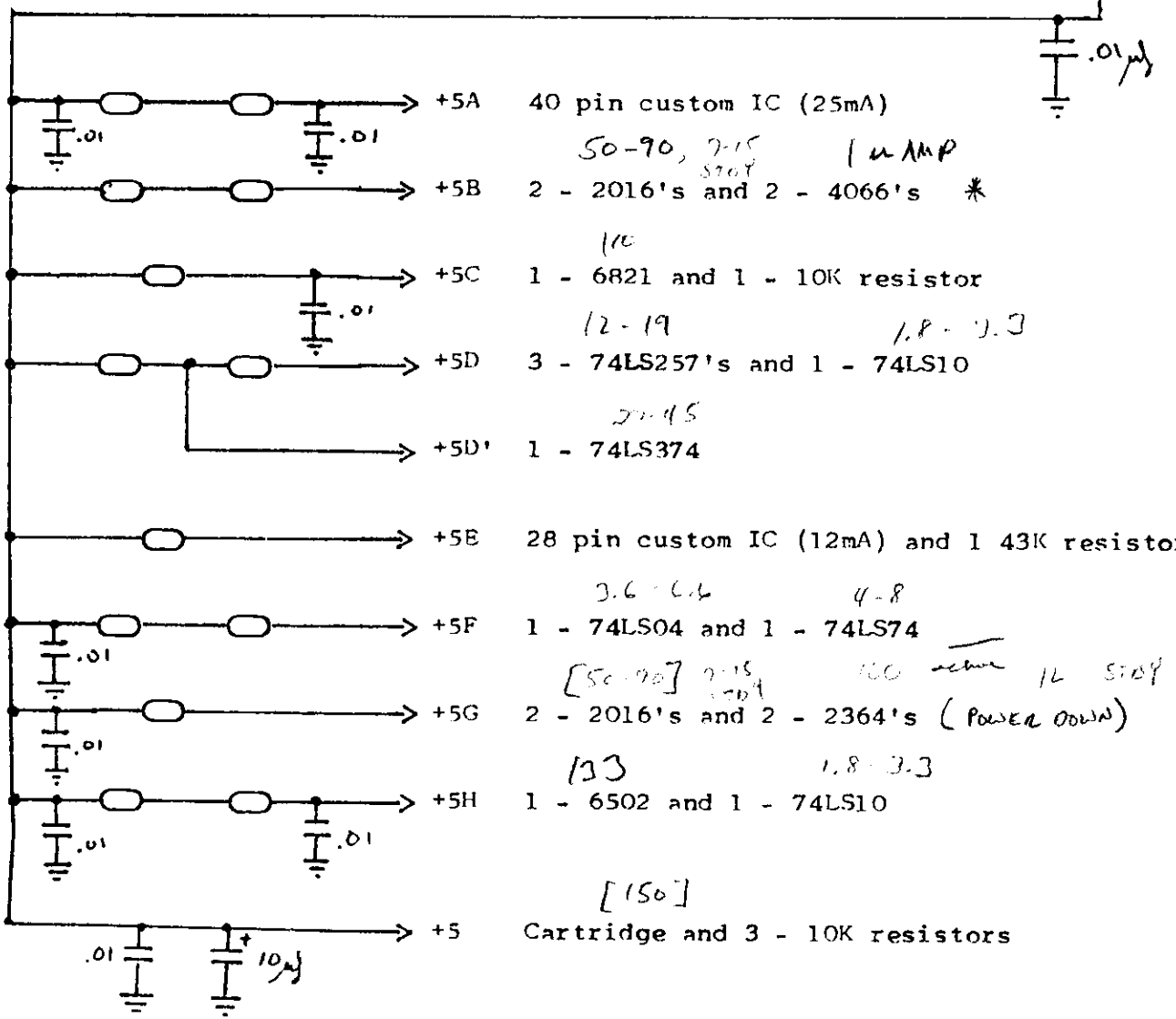
(*) VALID DATA ≤ 200 ns min

(*) CS (OE) R/W 60 ns min



POWER DISTRIBUTION





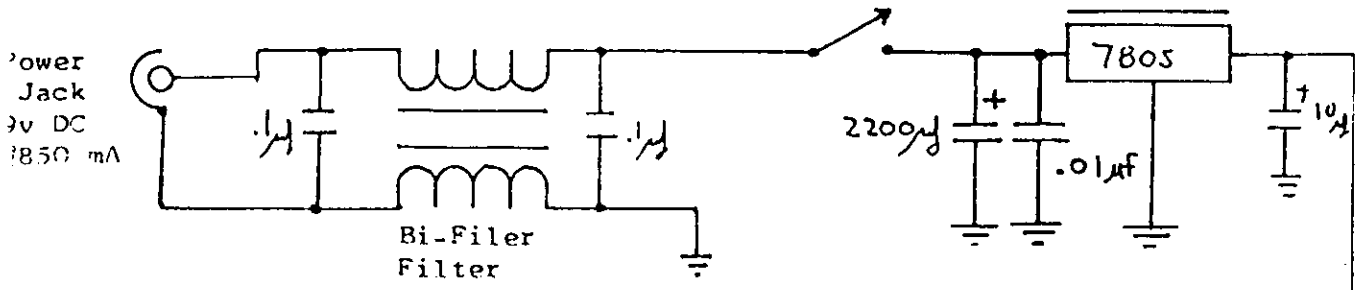
⬭ = Ferrite Bead

* WORST CASE

1 2016 ACTIVE
3 2016 STANDBY
1 2364 ACTIVE
1 2364 STANDBY
1 150 MA CARTRIDGE

Rev Ø

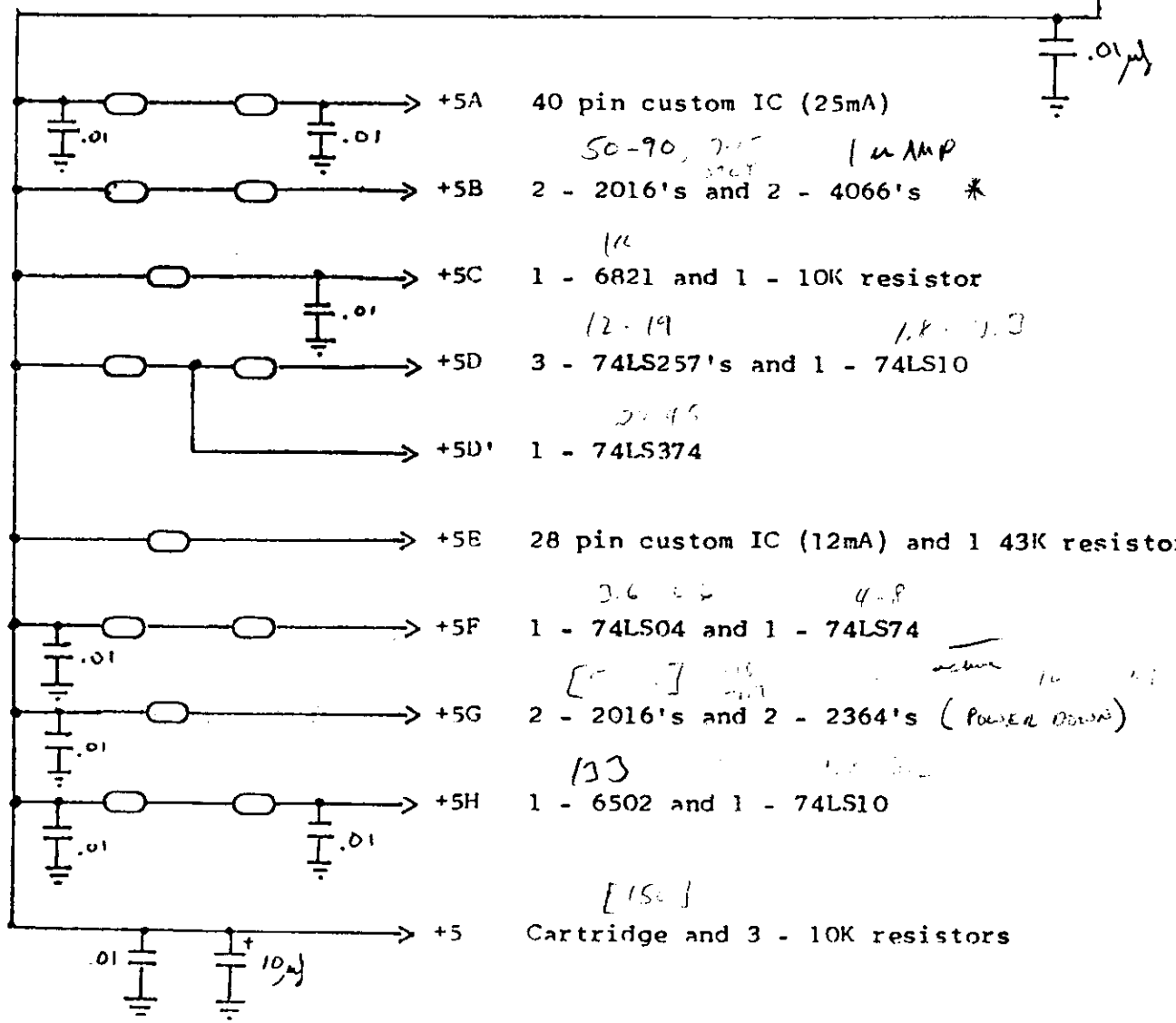
DAZ



⬭ = Ferrite Bead

* WORST CASE

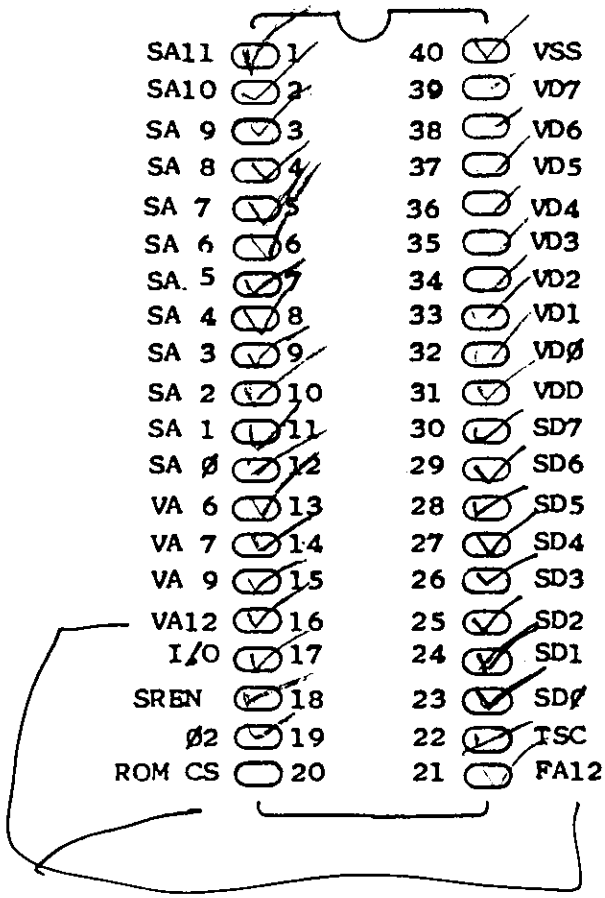
1 2016 ACTIVE
3 2016 (STANDBY
1 2364 ACTIVE
1 2364 STANDBY
1 150 MA CARTRIDGE



Rev Ø

DAZ

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED



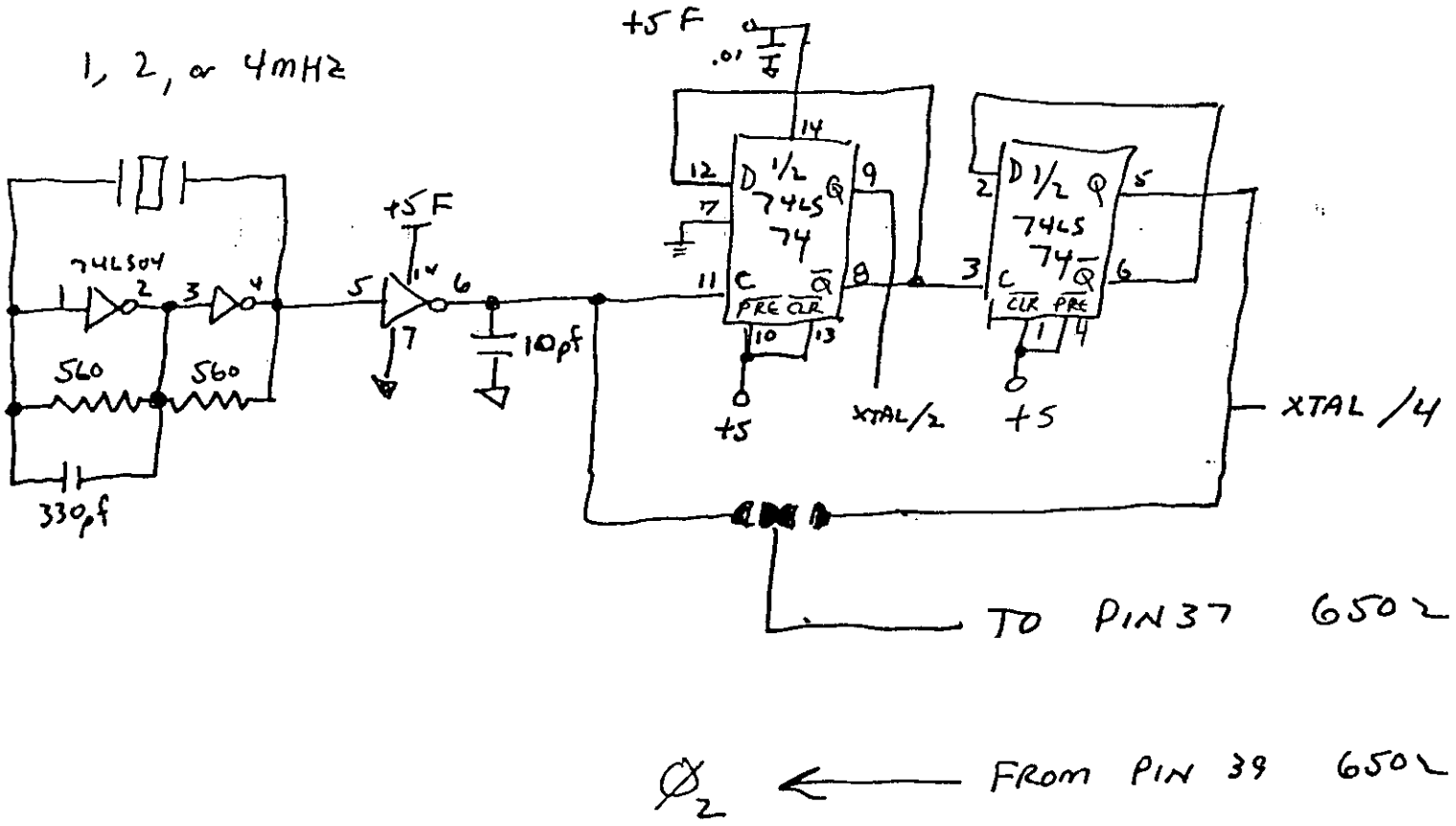
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	PERIPHERAL VISIONS, INCORPORATED	
	APPROVALS / DATE	C5502 PIN-OUT	
MATERIAL	DRAWN DA2 12 Apr 83		
FINISH	CHECKED	SIZE A / FSCM NO. / DWG. NO. 5502000101 / REV.	
DO NOT SCALE DRAWING	ISSUED	SCALE / SHEET	

EXPANSION CONNECTOR (44 PIN FEMALE)

PIN	SIGNAL	FUNCTION
W	GR/$\overline{W}$	Gated R/W output (for RAMs)--LSTTL
13	Ø2	Phase two output--MOS
19	CR/$\overline{W}$	Buffered R/W (for I/O devices)--LSTTL
17	$\overline{Res}$	Reset output--LSTTL
16	$\overline{IRQ}$	Interrupt request input--MOS, 1ØK pull-up
15	$\overline{NMI}$	Non-maskable interrupt input--MOS, 1ØK pull-up
18	RDY	Ready input--MOS, 1ØK pull-up
14	SYNC	Op-code sync output--MOS
C	A15	Address line 15--MOS (all)
D	A14	" " 14
E	A13	" " 13
F	A12	" " 12
H	A11	" " 11
J	A1Ø	" " 1Ø
K	A9	" " 9
L	A8	" " 8
M	A7	" " 7
N	A6	" " 6
P	A5	" " 5
R	A4	" " 4
S	A3	" " 3
T	A2	" " 2
U	A1	" " 1
V	AØ	" " Ø
2Ø	$\overline{I/O}$	Low-active I/O select ($9CØØ-$9FFF)--MOS
3	CB2	PIA I/O or cassette output--MOS
4	CB1	PIA input or cassette input--MOS
21	$\overline{RAM2}$	Low-active RAM select ($1ØØØ-$17FF)--MOS
Y	$\overline{RAM3}$	Low-active RAM select ($18ØØ-$1FFF)--MOS
X	$\overline{CROM}$	Low-active ROM select ($AØØØ-$BFFF)--MOS
5	D7	Data Line 7--MOS (all)
6	D6	" " 6
7	D5	" " 5
8	D4	" " 4
9	D3	" " 3
1Ø	D2	" " 2
11	D1	" " 1
12	DØ	" " Ø
2	+5V	(Total pins 2 and B: 15Ø mA MAX)
B	+5V	
1	GND	
22	GND	
A	GND	
Z	GND	

SHEET 2

CLOCK



OUT

PIN → 9 10 12 13 14 15 16 11

	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7		PIN
CL.	7	8	9	0	INS/DEL	←	CLR ↕		PA0	1
	6	5	4	3	2	1	ESC		PA1	2
	U	I	O	-	+	-	RET		PA2	3
	Y	T	<	E	W	Q	TAB		PA3	4
CTRL		K	L	.	;	=	J		PA4	5
		G	F	D	S	A	H		PA5	6
	N		M	,	•	/	SPACE		PA6	7
SHIFT		B	V	C	X	Z	FUNC		PA7	9

IN

MATRIX 9 × 8

PVI KEYBOARD

KEY		VAL	SHKEY	VAL
0	HOME	40	CLR	41
1	⊗	FF	⊗	FF
2	⊗	FF	⊗	FF
3	⊗	FF	⊗	FF
4	CTL	FF	CTL	FF
5	⊗	FF	⊗	FF
6	⊗	FF	⊗	FF
7	LSHIFT RSHIFT	FF	⊗	FF
8	7	17	'	07
9	6	16	&	06
10	U	35	U	35
11	Y	39	Y	39
12	⊗	FF	⊗	FF
13	⊗	FF	⊗	FF
14	N	2E	N	2E
15	⊗	FF	⊗	FF
16	⇩	46	⇧	45
17	ESC	FF	←	3F *
18	RET	4D	RET	4D
19	SELECT	FF	SELECT	FF
20	J	2A	J	2A
21	H	28	H	28
22	SP	00	SP	00
23	⊗	FF	⊗	FF
24	8	18	(	08
25	5	15	%	05
26	I	29	I	29
27	T	34	T	34
28	K	2B	K	2B
29	G	27	G	27
30 *	⊗	FF	⊗	FF
31	B	22	B	22
32	9	19	)	09
33	4	14	$	04
34	O	2F	O	2F
35	R	32	R	32
36	L	2C	L	2C
37	F	26	F	26
38	M	2D	M	2D
39	V	36	V	36

KEY		VAL	SHKEY	VAL
40	Ø	10	*	0A
41	3	13	#	03
42	P	30	P	30
43	E	25	E	25
44	:	1A	[	3B
45	D	24	D	24
46	;	0C	<	1C
47	C	23	C	23
48	DEL	FF	INS	FF
49	2	12	"	02
50	+	0B	@	20
51	W	37	W	37
52	,	1B	]	3D
53	S	33	S	33
54	.	0E	>	1E
55	X	38	X	38
56	⇨	44	⇦	43
57	1	11	!	01
58	—	0D	/	3C *
59	Q	31	Q	31
60	=	1D	↑	3E *
61	A	21	A	21
62	/	0F	?	1F
63	Z	3A	Z	3A

PVI

ATARI KYBD

PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 ← INPUT PORT

	1	2	3	4	5	6	7	8
PB0	9	BRK	⊗	⊗	⊗	CTL	⊗	⊗	L SHFT R SHFT
PB1	10	7	6	U	Y	⊗	⊗	N	⊗
PB2	11	BK SP	ESC	RET	TAB	J	H (n/c)	SP	⊗
PB3	12	8	5	I	T	K	G	M	B
PB4	13	9	4	O	R	L	F	,	V
PB5	14	0	3	P	E	;	D	.	C
PB6	15	<	2	-	W	+	S	/	X
PB7	16	>	1	=	Q	*	A	↑	Z

OUTPUT PORT

	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7	
	BRK	7	BK SP	8	9	0	<	>	PA0
	⊗	6	ESC	5	4	3	2	1	PA1
	⊗	U	RET	I	O	P	-	=	PA2
	⊗	Y	TAB	T	R	E	W	Q	PA3
	CTL	⊗	J	K	L	;	+	*	PA4
	⊗	⊗	(n/c) H	G	F	D	S	A	PA5
	⊗	N	SP	M	,	.	/	↑	PA6
	L SHFT R SHFT	⊗	⊗	B	V	C	X	Z	PA7

ATARI KEYBOARD

← , BACKSLASH, ↑ NOT USED

KEY		VAL	SKEY	VAL
0	BRK	40	HOME	40
1		FF		FF
2		FF		FF
3		FF		FF
4	CTL	FF	CTL	FF
5		FF		FF
6		FF		FF
7	LSHIFT RSHIFT	FF		FF
8	7	17	'	07
9	6	16	&	06
10	U	35	U	35
11	Y	39	Y	39
12		FF		FF
13		FF		FF
14	N	2E	N	2E
15		FF		FF
16	BKSP	FF	BKSP	FF
17	ESC	FF	ESC	FF
18	RET	0D	RET	0D
19	TAB	FF	TAB	FF
20	J	2A	J	2A
21	H	28	H	28
22	SP	00	SP	00
23		FF		FF
24	8	18	@	20
25	5	15	%	05
26	I	29	I	29
27	T	34	T	34
28	K	2B	K	2B
29	G	27	G	27
30	M	2D	M	2D
31	B	22	B	22
32	9	19	(	08
33	4	14	$	04
34		00	0	00
35	R	32	R	32
36	L	2C	L	2C
37	F	26	F	26
38	,	0C	[	3B
39	V	36	V	36

KEY		VAL	SKEY	VAL
40	@	10	)	09
41		13	#	03
42		30	P	30
43	E	25	E	25
44	;	2B	:	1A
45	D	24	D	24
46	.	0E	]	3D
47	C	23	C	23
48	<	1C	CLR	41
49	2	12	"	02
50		0D		45
51	W	37	W	37
52	+	0B		43
53	S	33	S	33
54	/	0F	?	1F
55	X	38	X	38
56	>	1E	>	1E
57	1	11	!	01
58		1D		46
59	Q	31	Q	31
60	*	0A		44
61	A	21	A	21
62		FF		FF
63	Z	3A	Z	3A

3C, 3E, 3F MISSING

CHECK

LSHCOL = FE (F7)
RSHCOL = FE (EF)
LSH ROW = 80 (02)
RSH ROW = 80 (40)
LSH = 8 (1A)
RSH = 8 (27)

DIFF. FROM ATARI KYBD:

SHIFT (NOT CTL) ACCESSES CURSOR KEYS.
"BREAK" IS "HOME"
←, /, ↑ DONT PRINT

ESC, INSERT, DEL/BKSP, CLR/SET/TAB, CTRL, JIL
DO NOTHING

CAP/LOWER IS SAME AS "H"

SE 1800-4FFC 1000-17FC 7900
7DFE 1552

11	13	15	17	19	0B	00	41
3F	37	32	39	29	30	0A	4D
00	21	24	27	2A	2C	1B	44
00	00	38	36	2E	0C	0F	46
00	3A	23	22	2D	0E	00	43
00	33	26	28	2B	1A	1D	45
31	25	34	35	2F	20	3E	00
12	14	16	18	10	0D	40	00

LSH KEY SHOULD BE 19

RSH SHOULD BE KEY 26

CHECK FOR 1A AND 2B

KEY	LSH	RSH
2	SP	SP
4	SP	SP
6	SP	SP
8	SP	SP
Ø	SP	SP
—	SP	SP
HM	SP	SP
↑	$	$
E	£	£
T	(	(
U	Ø	Ø
@	HM	HM
↑	SP	SP
S	T	T
F	U	U
H	O	O
K	@	@
.	↑	↑
=	SP	SP
CR	E	E
Z	F	Z
C	H	C
B	K	B
M	L	M
.	=	>
SP	S	SP
f1	Ø	SP

f3 SP

	R 7	R 6	R 5	R 4	R 3	R 2	R 1	ROW 0
PB0	1 !	3 #	5 %	7 '	9)	+	£	INS DEL
PB1	←	W	R	Y	I	P	*	CR
PB2	CTRL	A	D	G	J	L	;	COL 2
PB3	RUN STOP	LSH	X	V	N	, <	? /	COL 3
PB4	SP	Z	C	B	M	. >	RSH	F1 COL 4
PB5	CBM	S	F	H	K	: [	=	F3 COL 5
PB6	Ø	E	T	U	O	@	↑	F5 COL 6
PB7	2 "	4 $	6 &	8 (	0	-	CLR HM	F7 COL 7
	PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
	0	1	2	3	4	5	6	7 ROW

LSH = $1A

RSH = $27

RSHROW = 02 = 1000 0010 = FD

RSHCOL = 10 = 0001 0000 = EF

LSHROW = 40 = 0100 0000 = BF

LSHCOL = 08 = 0000 1000 = F7

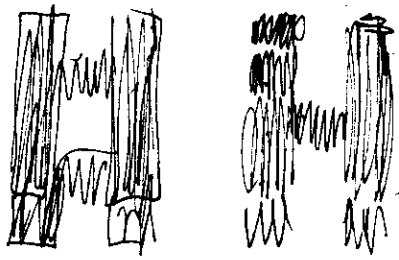
LS = 1E

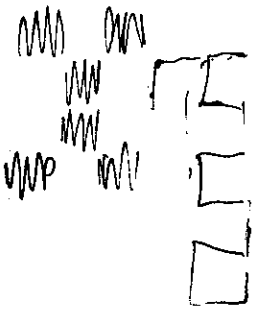
RS = 21

PROTOTYPE ONLY

```
! # %  ' '
1 3 5 7 9 + £ INST DEL
← W R Y I P * CR
CNTL A D G J L [redacted] ; ⇔

RVS L SHFT X V N , ? / ↕
SP Z C B M . R SHFT F1
C= S F H K : = F2
Q E T U O @ ↑ F3
2" 4$ 6& 8( Ø - HM F4
```





FRMBLNK MUST = 2

CHANGE N

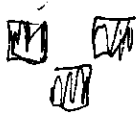
COLS → PB
ROWS → PA

COLØ = PBØ
RowØ = PAØ

COLØ = PIN12
RowØ = PIN20

KEY = [redacted] PIN2

1	NC	(GND)
2	KEY	
3	NC	(+5)
4	NC	(UNREGULATED)
5	PB7	
6	PB6	
7	PB5	
8	PB4	
9	PB3	
10	PB2	
11	[redacted] PB1	
12	[redacted] PB0	
13	PA7	
14	PA6	
15	PA5	
16	PA4	
17	PA3	
18	PA2	
19	PA1	
20	PA0	



```
SP Z C B M . RS F1
↓  ↓ ↓ ↓ ↓ ↓  ↓  ↓
5  F H K [ = SP Q

C= S F H K : = F2
E T U O @ ↑ SP 11
```

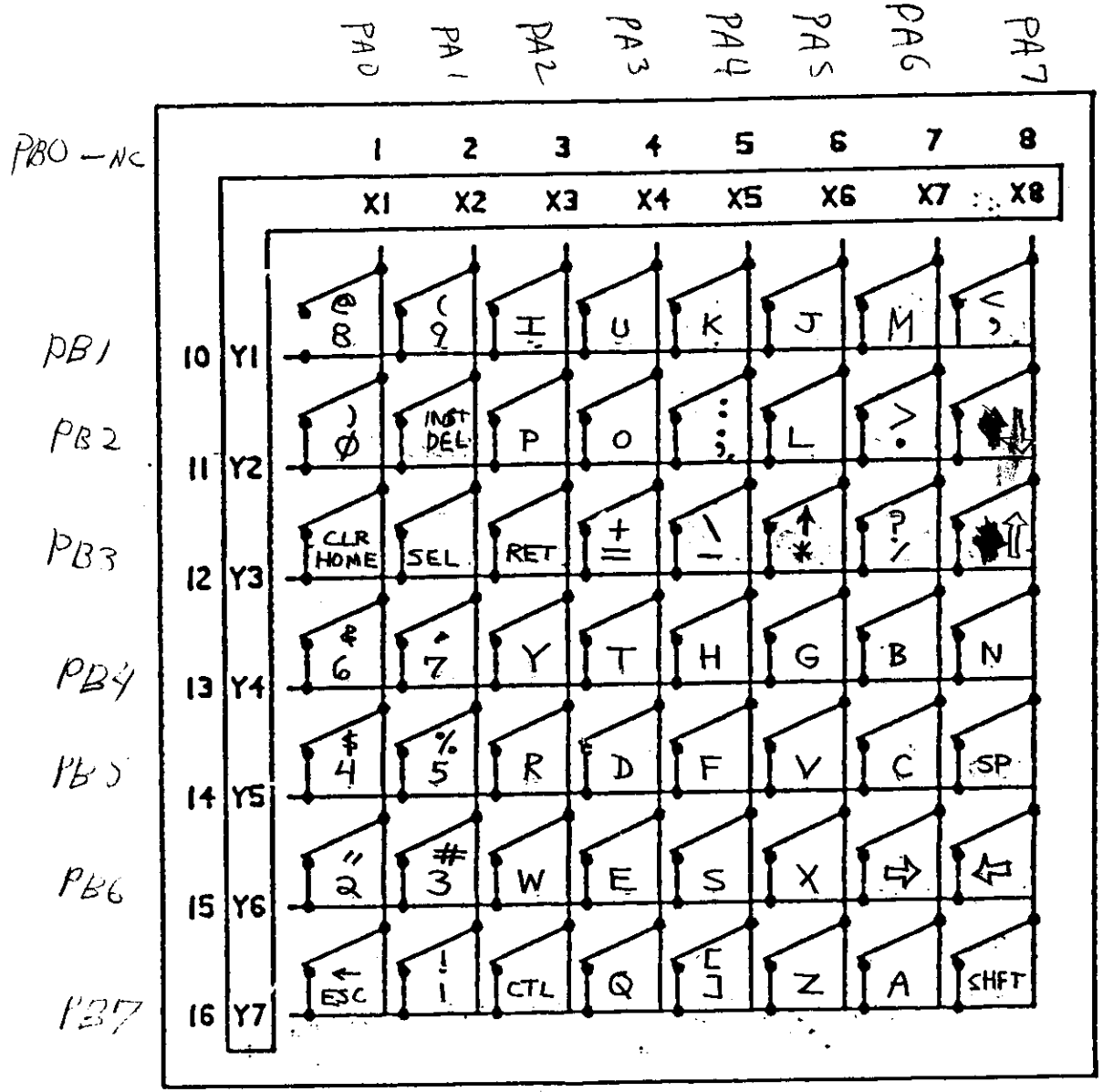
CES KEYBOARD 6/3/83 CFF = NON-PRINT

KEY#	NORMAL	KTBL	SHIFTED	SHFTBL
0	XX	FF	XX	FF
1	XX	FF	XX	FF
2	XX	FF	XX	FF
3	XX	FF	XX	FF
4	XX	FF	XX	FF
5	XX	FF	XX	FF
6	XX	FF	XX	FF
7	XX	FF	XX	FF
8	8	18	@	20
9	9	19	(	08
10	I	29	I	29
11	U	35	U	35
12	K	2B	K	2B
13	J	2A	J	2A
14	M	2D	M	2D
15	,	0C	<	1C
16	Ø	10	)	09
17	DEL	[redacted] 4E	INST	FF
18	P	30	P	30
19	O	2F	O	2F
20	;	1B	:	1A
21	L	2C	L	2C
22	.	0E	>	1E
23	⇩	4A	⇩	4A
24	HOME	5E	CLR	5A
25	SEL	FF	SEL	FF
26	RET	4D	RET	4D
27	=	1D	+	0B
28	-	0D	/	3C
29	*	0A	↑	3E
30	/	0F	?	1F
31	⇧	4B	⇧	4B

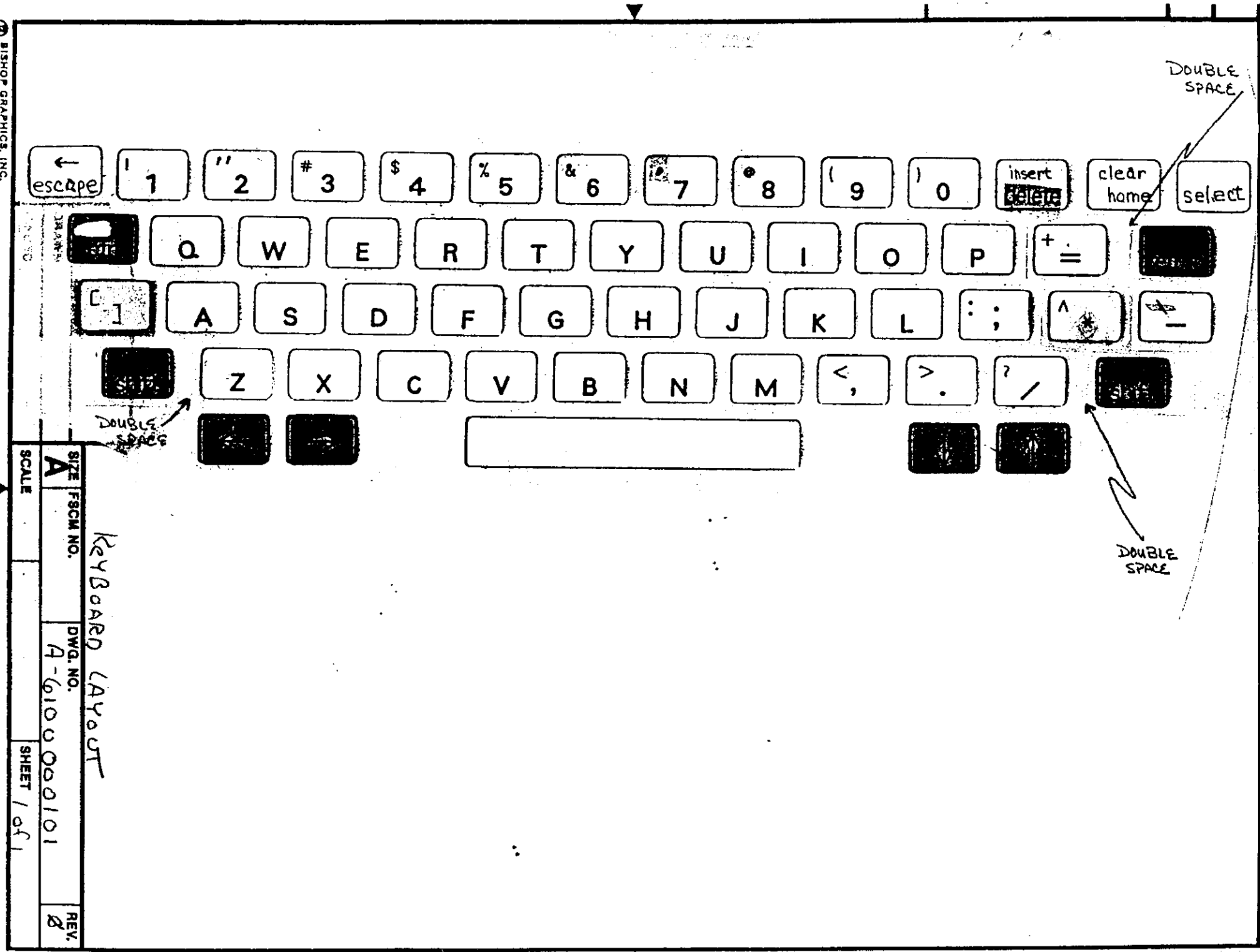
*

KEY #	NORMAL	KTBL	SHIFTED	SHFTBL
32	6	16	&	06
33	7	17	'	07
34	Y	39	Y	39
35	T	34	T	34
36	H	28	H	28
37	G	27	G	27
38	B	22	B	22
39	N	2E	N	2E
40	4	14	$	04
41	5	15	%	05
42	R	32	R	32
43	D	24	D	24
44	F	26	F	26
45	V	36	V	36
46	C	23	C	23
47	SP	00	SP	06
48	2	12	"	02
49	3	13	#	03
50	W	37	W	37
51	E	25	E	25
52	S	33	S	33
53	X	38	X	38
54	⇨	4C	⇨	4C
55	⇦	48	⇦	48
56	ESC	FF	←	3F
57	1	11	!	01
58	CTL	FF	CTL	FF
59	Q	31	Q	31
60	J	3D	E	3B
61				
62	Z	3A	Z	3A
63	A	21	A	21
	SHIFT (L,R)	FF	SHIFT (L,R)	FF

LSHCOL=$7F
RSHCOL=$7F
LSHROW=$80
RSHROW=$80
LSH=64_{10}
RSH=64_{10}



NOTE: PIN 9 NOT USED



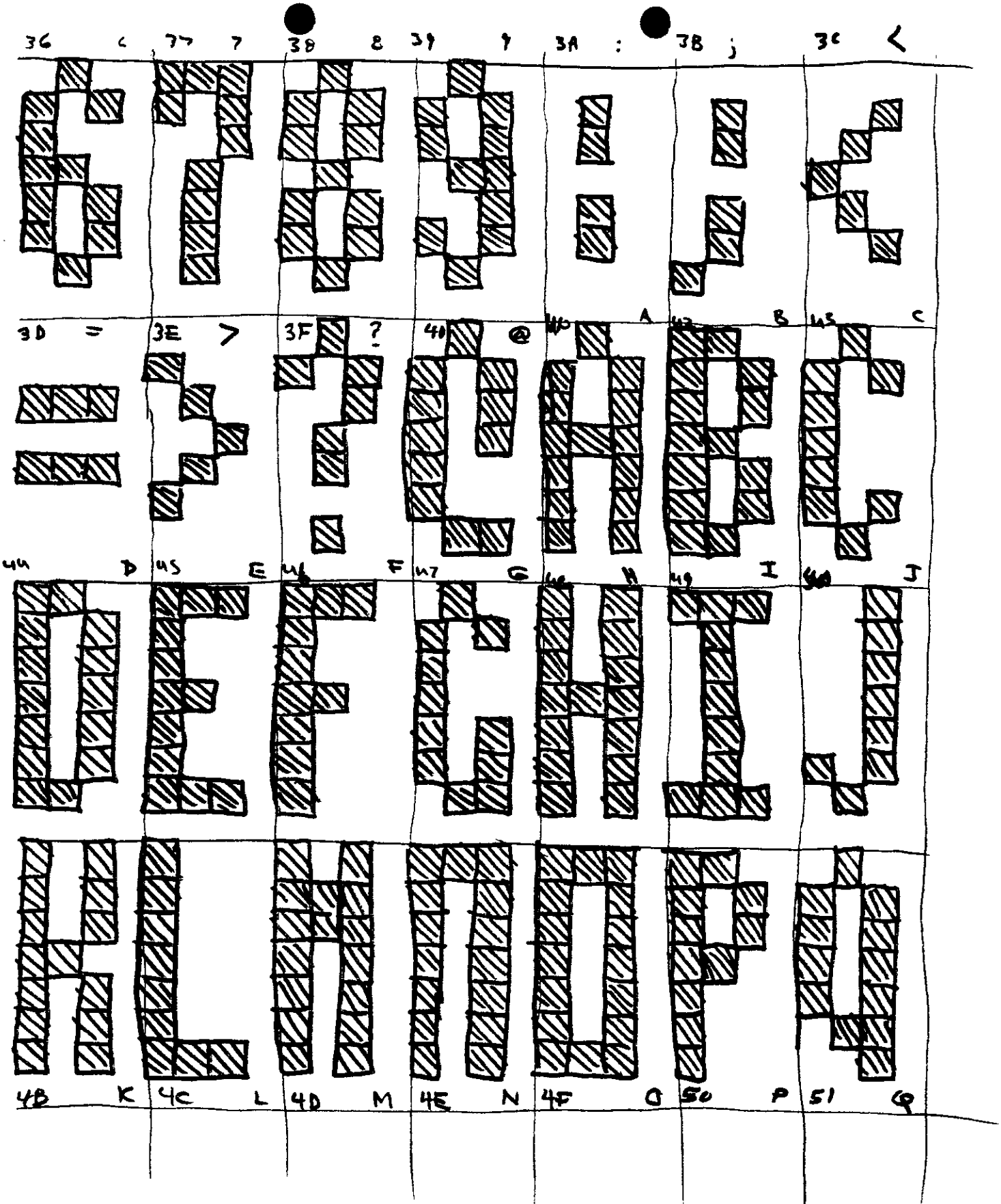
BISHOP GRAPHICS, INC.
REORDER NO. 20508

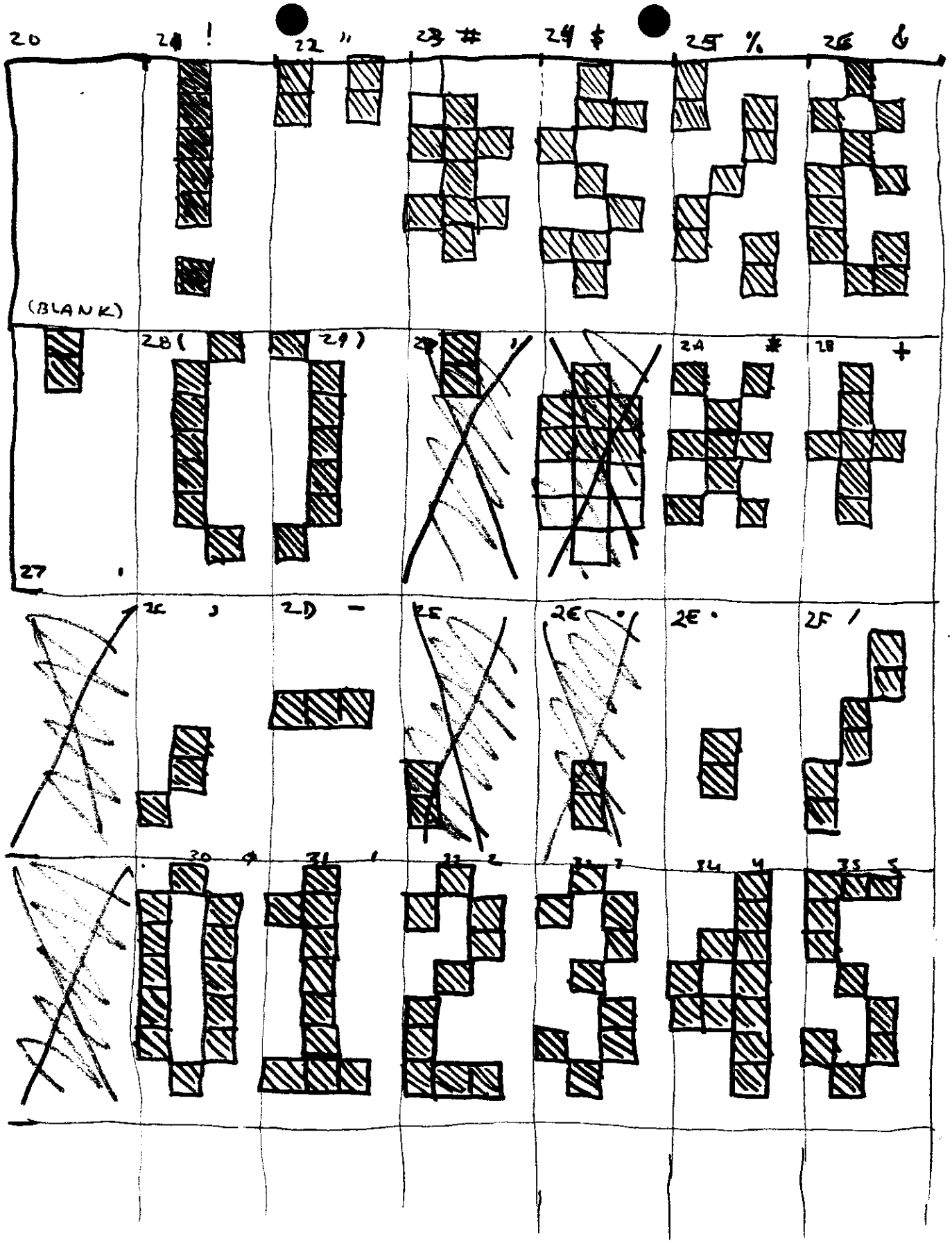
SIZE	FSCM NO.	DWG. NO.	REV.
A		A-6100000101	B

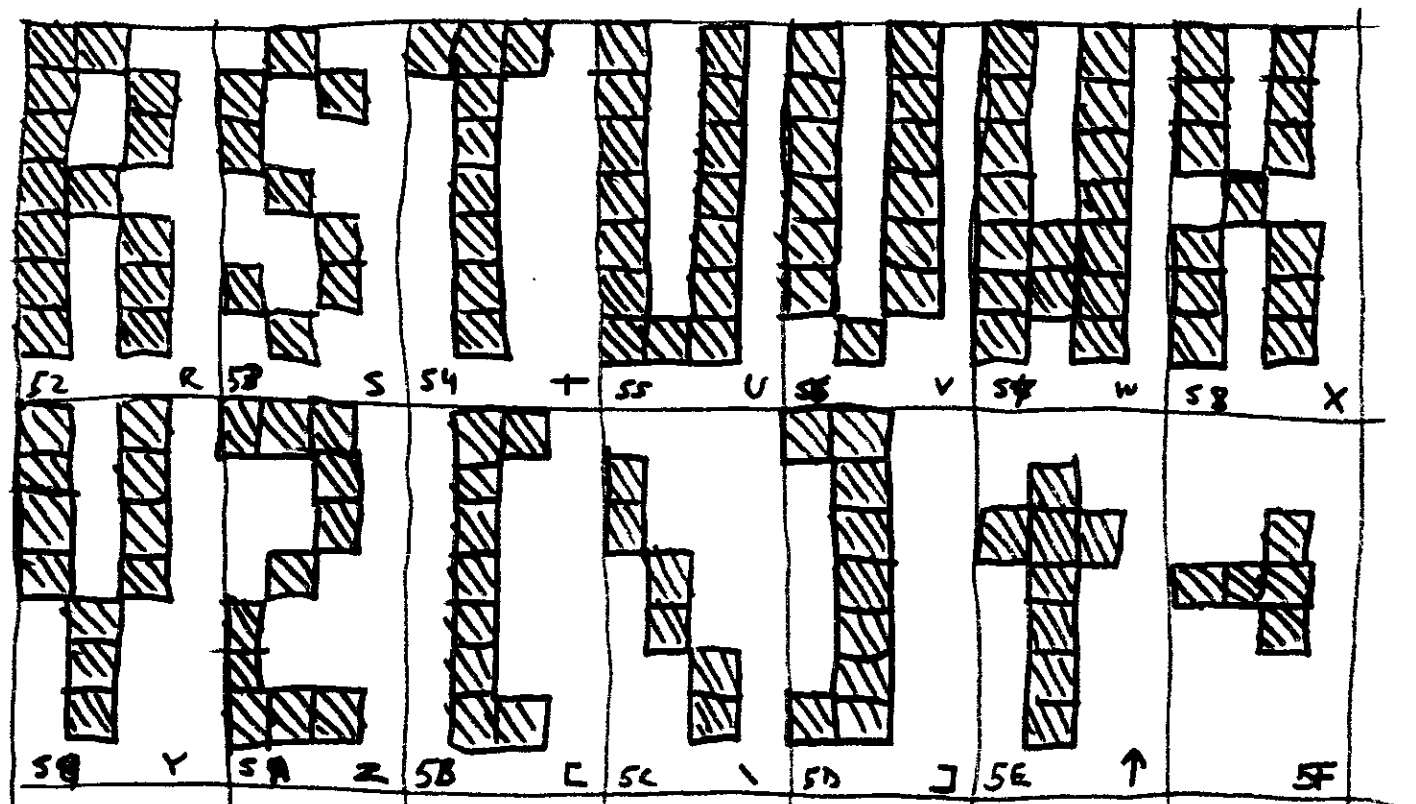
SCALE

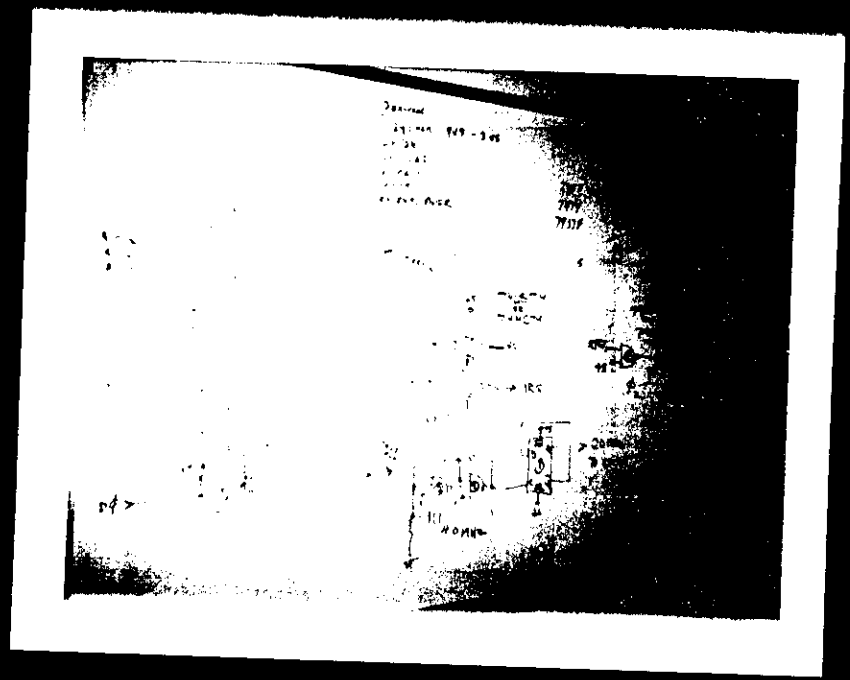
SHEET 1 of 1

KEYBOARD LAYOUT


36 6
37 7
38 8
39 9
3A :
3B ;
3C <
3D =
3E >
3F ?
40 @
41 A
42 B
43 C
44 D
45 E
46 F
47 G
48 H
49 I
4A J
4B K
4C L
4D M
4E N
4F O
50 P
51 Q

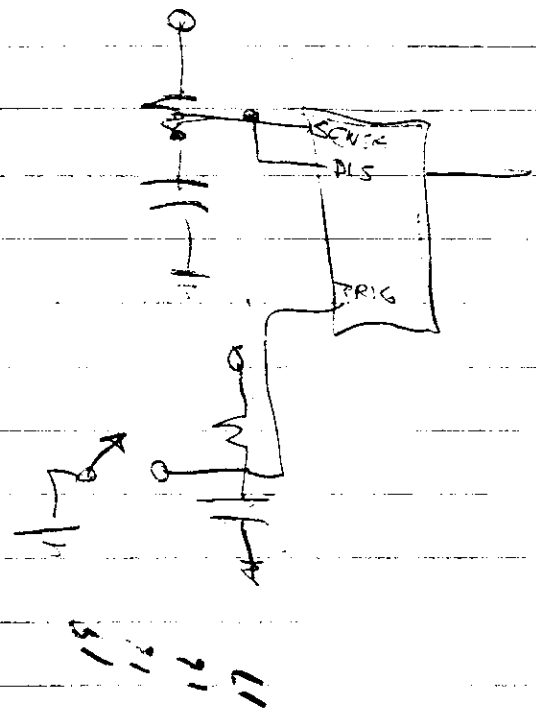

20
21 !
22 "
23 #
24 $
25 %
26 &
(BLANK)
28 (
29)
2A *
2B +
27 ,
2C ;
2D -
2E .
2E .
2F /
30 0
31 1
32 2
33 3
34 4
35 5


52 R
53 S
54 T
55 U
56 V
57 W
58 X
59 Y
5A Z
5B L
5C \
5D]
5E ↑
5F

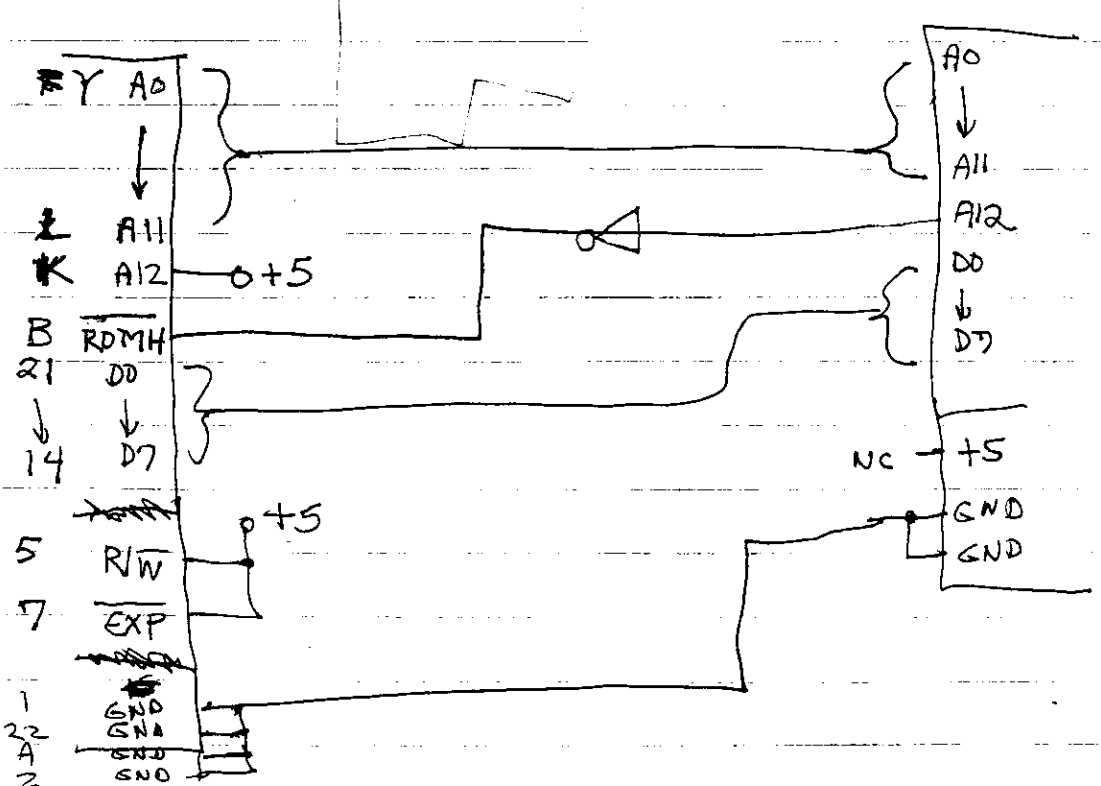


VCS CART PINOUT

1 - GND		A - A7	
2 - +5		B - A6	
3 - A8		C - A5	
4 - A9		D - A4	
5 - [redacted] A11		E - A3	
6 - A10		F - A2	
(D4) 7 - [redacted] ~~A12~~	CS (A12)	H - A1	
8 - D7		J - A0	
9 - D6		K - D0	
10 - D5		L - D1	
(A12) 11 - D4		M - D2	
12 - D3		N - GND	



PADDLE BOARD



VCS CART

BILL OF MATERIAL

ITEM #	DESC	QUANTITY	PART #	REV #	
1	SCHEMATIC	1	D-4010000501	Ø	
2	PC BOARD	1	A-4090000501	Ø	
3	VCS CON BOARD	1	A-4090000201	3	
4	CUSTOM CHIP	1	A-5501000101	Ø	IC-1
5	6502	1	A-1320650201	Ø	IC-17
6	6821	1	A-1320682101	Ø	IC 18
7	~~128K ROM~~ → 64K ROM	1	A-1350400101	Ø	IC-16
8	~~2016 RAM~~ → 2 ← (4)	(4)	A-1340201601	Ø	IC-3,4,1
9	7805 REG	1	A-1245780501	Ø	IC-11
10	74LS157 A00 16K ROM	3	A-1305015701	Ø	IC-5,6,7
11	74LS374 .95	1	A-1305037401	Ø	IC-10
12	74LS00	1	A-1305000001	Ø	IC-20
13	4066	4	A-1315406601	Ø	IC-1,2,8
14	R 1K .25W	1	A-1001010201	Ø	R-6
15	R 10K .25W	4	A-1001010301	Ø	R-1 to 4
16	R 20K .25W	1	A-1001020301	Ø	R-7
17	R 330K .25W	1	A-1001033401	Ø	R-5
18	R- CAL	1	T B D	Ø	R-8
19	CAP 2200uF	1	A-1150222201	Ø	C-19
20	CAP 10uF	3	A-1140110001	Ø	C-16,29,
21	CAP 10pF	2	A-1120310001	Ø	C-23,24
22	CAP .002uf	1	A-1120320201	Ø	C-30
23	CAP .22uF	4	A-1101322401	Ø	C-12,13,
24	CAP .1uF	7	A-1120310401	Ø	C-5,14,1 C-27
25	CAP .01uF	19	A-1120310301	Ø	C-1-4,6- C-21,25,
26	DIODE 1N914	3	A-1202091401	Ø	CR1-3
27	~~PWR & CAS. JACK~~	3	A-0430000101	Ø	J1-3
28	~~44 PIN CONN~~	1	A-0400004401	Ø	C-1
29	KEYBOARD CONN	1	A-0440000101	Ø	C-2
30	~~SHIELD BOX~~	1	D-3000000301	1	
31	SWITCH	1	A-0500000101	Ø	SW-1
32	HEAT SINK	1	A-1600000101	Ø	
33	SCREW	1	A-0132100801	Ø	
34	HEX NUT	1	A-0300003001	Ø	
35	WASHER	1	A-0340003001	Ø	
36	4 1 Mhz CRYSTAL	1	A-1501000101	Ø	Y-1
37	LINE FILTER	1	A-1440000101	Ø	T-1
38	FERR BEADS	33	A-1430000101	Ø	FB-1 TO
39	FLAT CABLE	2	A-2000002501	Ø	W-1,W-2
40	KEYBOARD	1	A-6100000101	Ø	
41	CASE USE	1			
42	~~POWER SUPPLY~~ US>	1	A-6000000101	Ø	PS-1
43	MOUNT SCREWS SUPPLY	12			
44	MANUAL	1			
45	PACKING MAT	1			

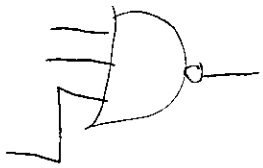
BILL OF MATERIAL

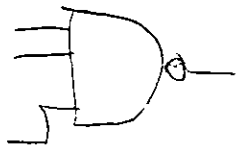
ITEM #	DESC	QUANTITY	PART #	REV #
1	SCHEMATIC	1	D-4010000501	0
2	PC BOARD	1	A-4090000501	0
3	VCS CON BOARD	1	A-4090000201	3
4	CUSTOM CHIP	1	A-5501000101	0 IC-12
5	6502	1	A-1320650201	0 IC-17
6	6821	1	A-1320682101	0 IC-18
7	128K ROM	1	A-1350400101	0 IC-16
8	2016 RAM	4	A-1340201601	0 IC-3,4,13,14
9	7805 REG	1	A-1245780501	0 IC-11
10	74LS157	3	A-1305015701	0 IC-5,6,7
11	74LS374	1	A-1305037401	0 IC-10
12	74LS00	1	A-1305000001	0 IC-20
13	4066	4	A-1315406601	0 IC-1,2,8,9
14	R 1K .25W	1	A-1001010201	0 R-6
15	R 10K .25W	4	A-1001010301	0 R-1 to 4
16	R 20K .25W	1	A-1001020301	0 R-7
17	R 330K .25W	1	A-1001033401	0 R-5
18	R- CAL	1	T B D	0 R-8
19	CAP 2200uF	1	A-1150222201	0 C-19
20	CAP 10uF	3	A-1140110001	0 C-16,29,36
21	CAP 10pF	2	A-1120310001	0 C-23,24
22	CAP .002uf	1	A-1120320201	0 C-30
23	CAP .22uF	4	A-1101322401	0 C-12,13,20,22
24	CAP .1uF	7	A-1120310401	0 C-5,14,15,18,26 C-27
25	CAP .01uF	19	A-1120310301	0 C-1-4,6-11,17 C-21,25,31-35
26	DIODE IN914	3	A-1202091401	0 CR1-3
27	PWR & CAS. JACK	3	A-0430000101	0 J1-3
28	44 PIN CONN	1	A-0400004401	0 C-1 CN1
29	KEYBOARD CONN	1	A-0440000101	0 C-2
30	SHIELD BOX	1	D-3000000301	1 CN2
31	SWITCH	1	A-0500000101	0 SW-1
32	HEAT SINK	1	A-1600000101	0
33	SCREW	1	A-0132100801	0
34	HEX NUT	1	A-0300003001	0
35	WASHER	1	A-0340003001	0
36	1 Mhz CRYSTAL	1	A-1501000101	0 Y-1
37	LINE FILTER	1	A-1440000101	0 T-1
38	FERR BEADS	33	A-1430000101	0 FB-1 TO 11
39	FLAT CABLE	2	A-2000002501	0 W-1,W-2
40	KEYBOARD	1	A-6100000101	0
41	CASE	1		
42	POWER SUPPLY	1	A-6000000101	0 PS-1
43	MOUNT SCREWS	12		
44	MANUAL	1		
45	PACKING MAT	1		

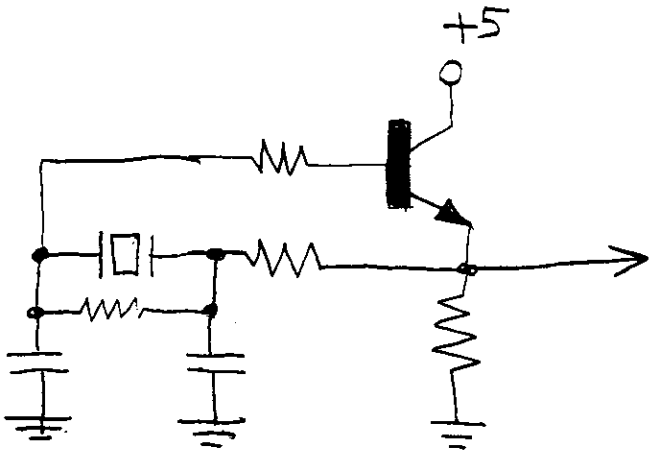
EXPANSION CONNECTOR (44 PIN FEMALE)

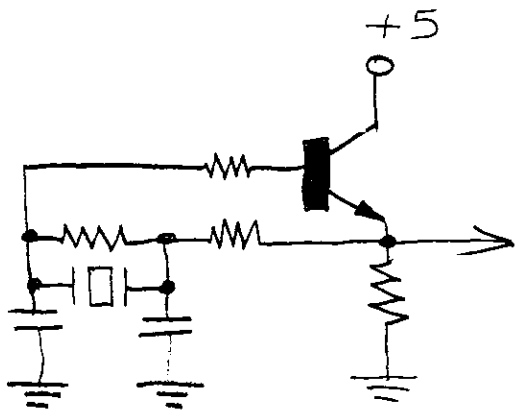
PIN	SIGNAL	FUNCTION
W	GR/W	Gated R/W output (for RAMs)--LSTTL
13	Ø2	Phase two output--MOS
19	CR/W	Buffered R/W (for I/O devices)--LSTTL
17	Res	Reset output--LSTTL
16	IRQ	Interrupt request input--MOS, 1ØK pull-up
15	NMI	Non-maskable interrupt input--MOS, 1ØK pull-up
18	RDY	Ready input--MOS, 1ØK pull-up
14	SYNC	Op-code sync output--MOS
C	A15	Address line 15--MOS (all)
D	A14	" " 14
E	A13	" " 13
F	A12	" " 12
H	A11	" " 11
J	A1Ø	" " 1Ø
K	A9	" " 9
L	A8	" " 8
M	A7	" " 7
N	A6	" " 6
P	A5	" " 5
R	A4	" " 4
S	A3	" " 3
T	A2	" " 2
U	A1	" " 1
V	AØ	" " Ø
2Ø	I/O	Low-active I/O select ($9CØØ-$9FFF)--MOS
3	CB2	PIA I/O or cassette output--MOS
4	CB1	PIA input or cassette input--MOS
21	RAM2	Low-active RAM select ($1ØØØ-$17FF)--MOS
Y	RAM3	Low-active RAM select ($18ØØ-$1FFF)--MOS
X	CROM	Low-active ROM select ($AØØØ-$BFFF)--MOS
5	D7	Data Line 7--MOS (all)
6	D6	" " 6
7	D5	" " 5
8	D4	" " 4
9	D3	" " 3
1Ø	D2	" " 2
11	D1	" " 1
12	DØ	" " Ø
2	+5V	(Total pins 2 and B: 15Ø mA MAX)
B	+5V	
1	GND	
22	GND	
A	GND	
Z	GND	


A15
A14






+5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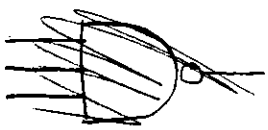
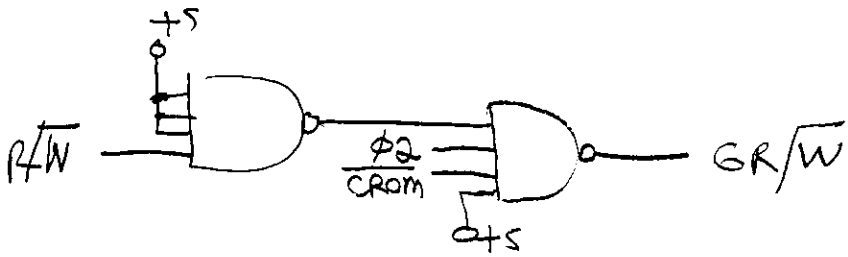
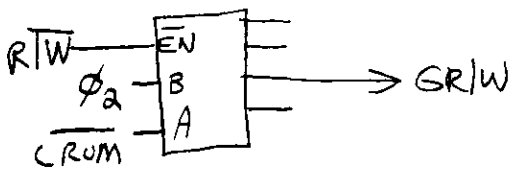
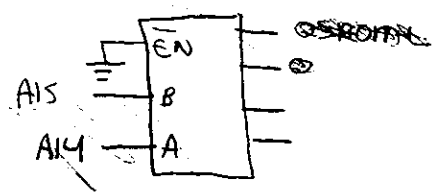



+5
R/W
Φ2
CROM
+5
GR/W


R/W
Φ2
CROM
EN
B
A
GR/W


EN
A15
B
A14
A

WHAT HAPPENS TO LSTTL AND CMOS
IF INPUT LEVELS ARE
APPLIED WITH NO POWER?

IN FRODOSYSTEM

VD LINES ~~SEE~~ 1-LS LOAD OFF
1-4006 SWITCH OFF

VA LINES (VA0, VA4, VA6, VA8-VA10, VA11) SEE: 1-LS LOAD OFF
VA? LINES (VA1, VA2, VA3, VA5, VA7) SEE: 1-LS LOAD OFF
~~VA11 SEES: 1 LS~~ 1-MOS LOAD OFF
VA12 SEES: 1-MOS LOAD OFF
1-10K RESISTOR TO +5 OFF)

IN BURRO

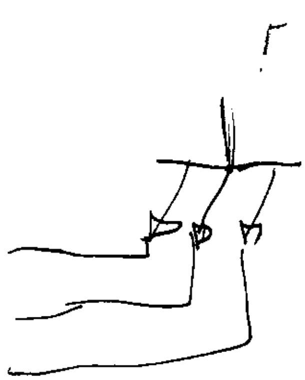
NO POWER

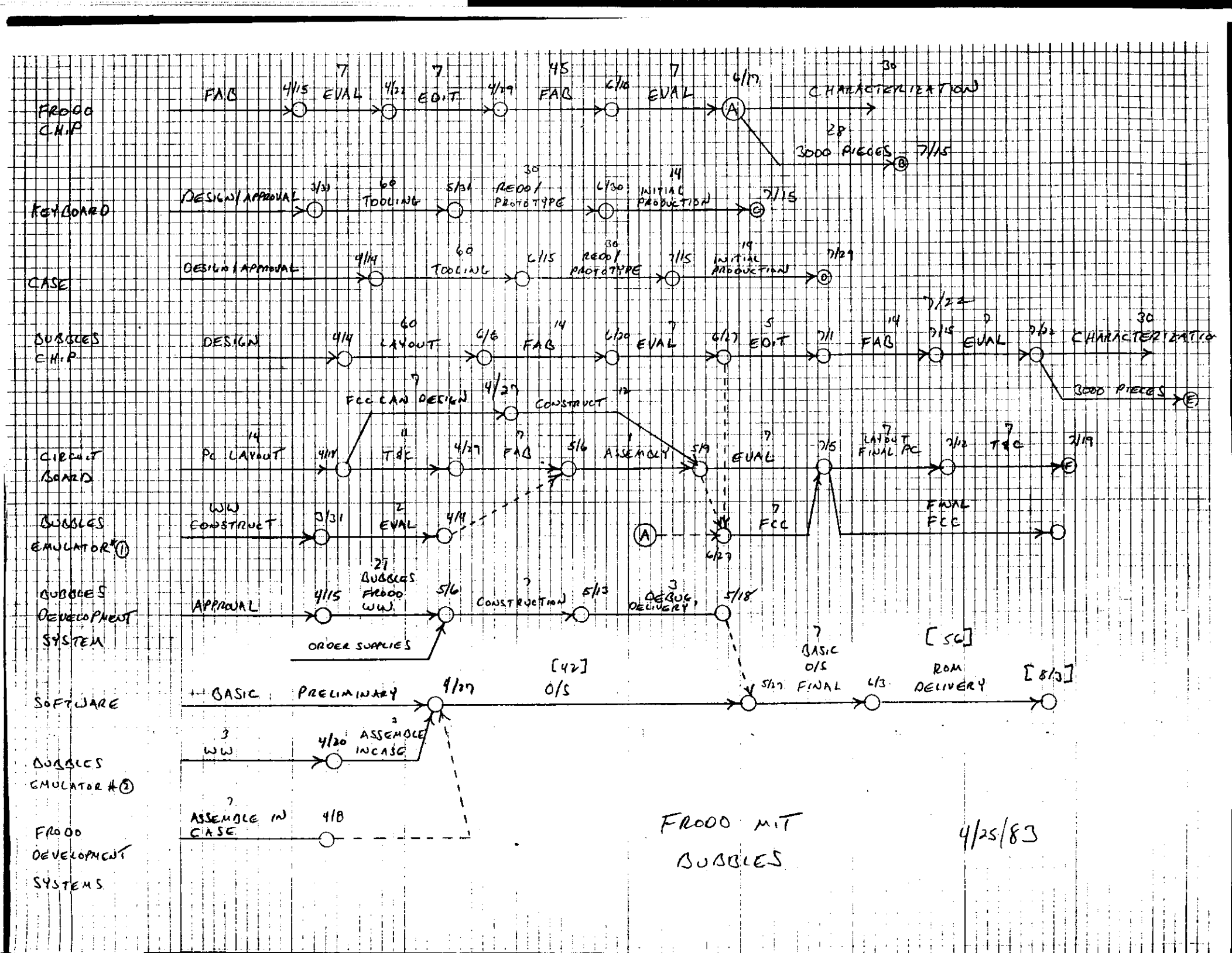
VA0 — LS
VA1 — LS, MOS
VA2 — LS, MOS
VA3 — LS, MOS
VA4 — LS
VA5 — LS
VA6 — LS
VA7 — LS
VA8 — LS
VA9 — LS
VA10 — LS
VA11 — LS
VA12

VD0
VD1
VD2
VD3
VD4
VD5
VD6
VD7

ADD PULL

64
8
512K BITS




FROOO CHIP
FAB
4/15
7
EVAL
4/22
7
EDIT
4/29
45
FAB
6/10
7
EVAL
4/17
A
30
CHARACTERIZATION
28
3000 PIECES
7/15
KEYBOARD
DESIGN/APPROVAL
3/31
60
TOOLING
5/31
30
REDO/PROTOTYPE
6/30
14
INITIAL PRODUCTION
7/15
CASE
DESIGN/APPROVAL
4/14
60
TOOLING
6/15
30
REDO/PROTOTYPE
7/15
19
INITIAL PRODUCTION
7/29
BUBBLES CHIP
DESIGN
4/4
60
LAYOUT
6/6
14
FAB
6/20
7
EVAL
6/27
5
EDIT
7/1
14
FAB
7/15
7
EVAL
7/22
30
CHARACTERIZATION
3000 PIECES
FCC CAN DESIGN
7
4/27
CONSTRUCT
12
CIRCUIT BOARD
14
PC LAYOUT
4/11
11
T&C
4/27
7
FAB
5/6
1
ASSEMBLY
5/9
7
EVAL
7/5
7
LAYOUT FINAL PC
7/12
7
T&C
7/19
BUBBLES EMULATOR #1
WW CONSTRUCT
3/31
2
EVAL
4/19
A
7
FCC
6/27
FINAL FCC
BUBBLES DEVELOPMENT SYSTEM
APPROVAL
4/15
27
BUBBLES FROOO WW
5/6
ORDER SUPPLIES
7
CONSTRUCTION
5/13
3
DEBUG DELIVERY
5/18
SOFTWARE
BASIC
PRELIMINARY
4/27
[42]
O/S
5/27
7
BASIC O/S FINAL
6/3
[5C]
ROM DELIVERY
[8/3]
BUBBLES EMULATOR #2
3
WW
4/20
2
ASSEMBLE INCASE
FROOO DEVELOPMENT SYSTEMS
ASSEMBLE IN CASE
4/18
FROOO MIT BUBBLES
4/25/83

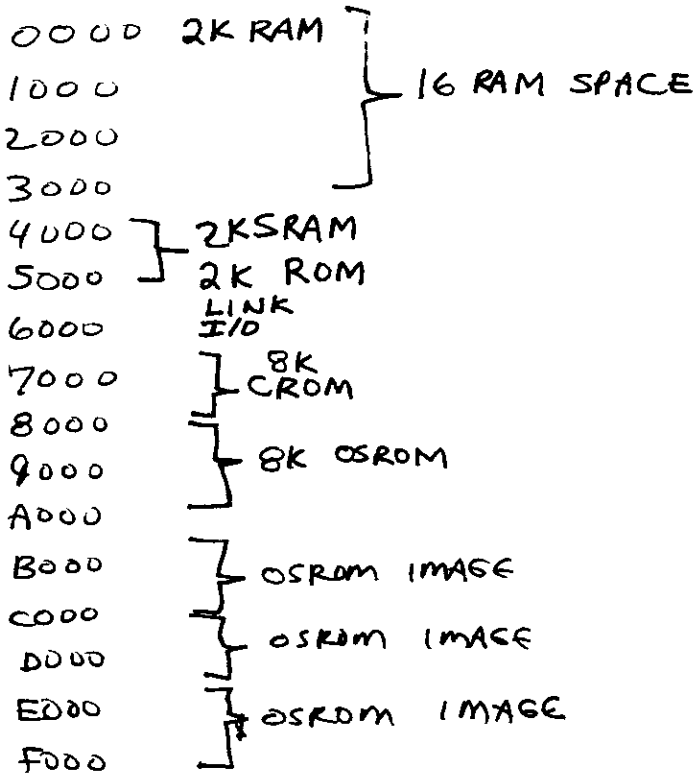
GRADUATE COST COMPARISON

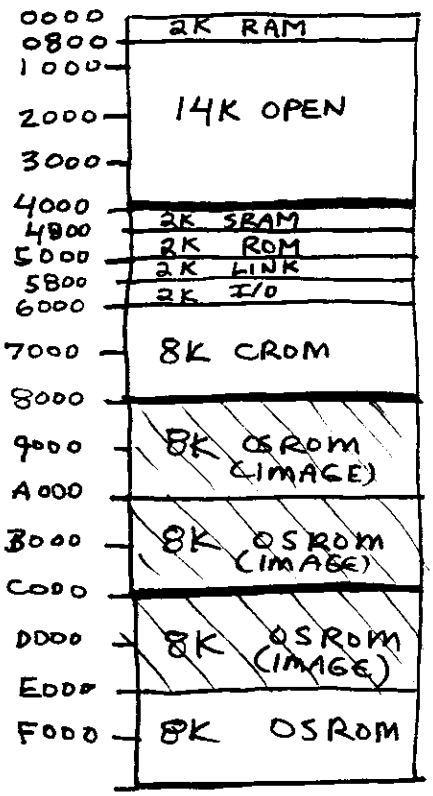
DESCRIPTION	ORIGINAL BOM		PRESENT BOM	
	QUANTITY	COST	QUANTITY	COST
PC BOARD	1	3.00	1	3.00
POWER CONN	1	0.06	1	0.06
44 PIN CONN	1	0.50	1	0.50
24 PIN CONN	1	0.45	1	0.45
KEYBOARD CON	1	0.10	1	0.10
SHIELD BOX	2	0.24	*B 1	0.50
SWITCH	1	0.08	1	0.08
HEAT SINK	1	0.06	1	0.06
HT SINK HDWE	1	0.01	1	0.00
CRYSTAL	1	0.70	1	0.70
6502	1	2.15	1	2.15
(6520) 6821	1	1.50	1	1.15
ROM 64K	2	5.25	2	4.50
2016 RAM	4	8.00	4	8.00
7805 REGULAT	1	0.29	1	0.29
(74LS157/257	3	0.42	*B 1	0.54
FRODO	1	1.25	1	1.25
74LS374	1	0.30	1	0.30
74LS00	1	0.09	1	0.09
4066	4	0.56	*B 1	0.28
RESISTORS	7	0.04	9	0.04
CAP 2200MF	1	0.20	1	0.20
CAP 10MF	6	0.12	6	0.12
CAP 10PF	2	0.02	2	0.02
CAP .002MF	1	0.01	1	0.01
CAP .01MF	23	0.25	19	0.25
LINE FILTER	1	0.10	1	0.10
DIODE 1N914	1	0.01	*C 3	0.03
FERR BEADS	9	0.07	*B 45	0.34
FLAT CABLE	1	0.10	U 2	0.20
VCS CONN PCB	1	0.35	1	0.35
KEYBOARD	1	2.25	*K 1	3.25
CASE	1	1.60	1	1.60
POWER SUPPLY	1	1.30	*B 1	2.15
MOUNT SCREWS	12	0.01	12	0.01
MANUAL	1	0.10	1	0.10
PKG MATERIAL	1	0.50	1	0.50
BUBBLES			*B 1	
74LS04			1	0.14
74LS10			U 1	0.14
74LS74			*B 1	0.15
CAP .22MF			U 4	0.16
CAP .1MF			*B 5	0.15
CAP 330PF			U 1	0.01
CASSETTE JAK			*C 2	0.16
BOTTOM PLATE			U 1	0.20
TRIM RESISTO			*B 1	0.02
		32.04		34.40

NOTE: *B=BUBL; *C-CASS; *K=KYBD; U=USI

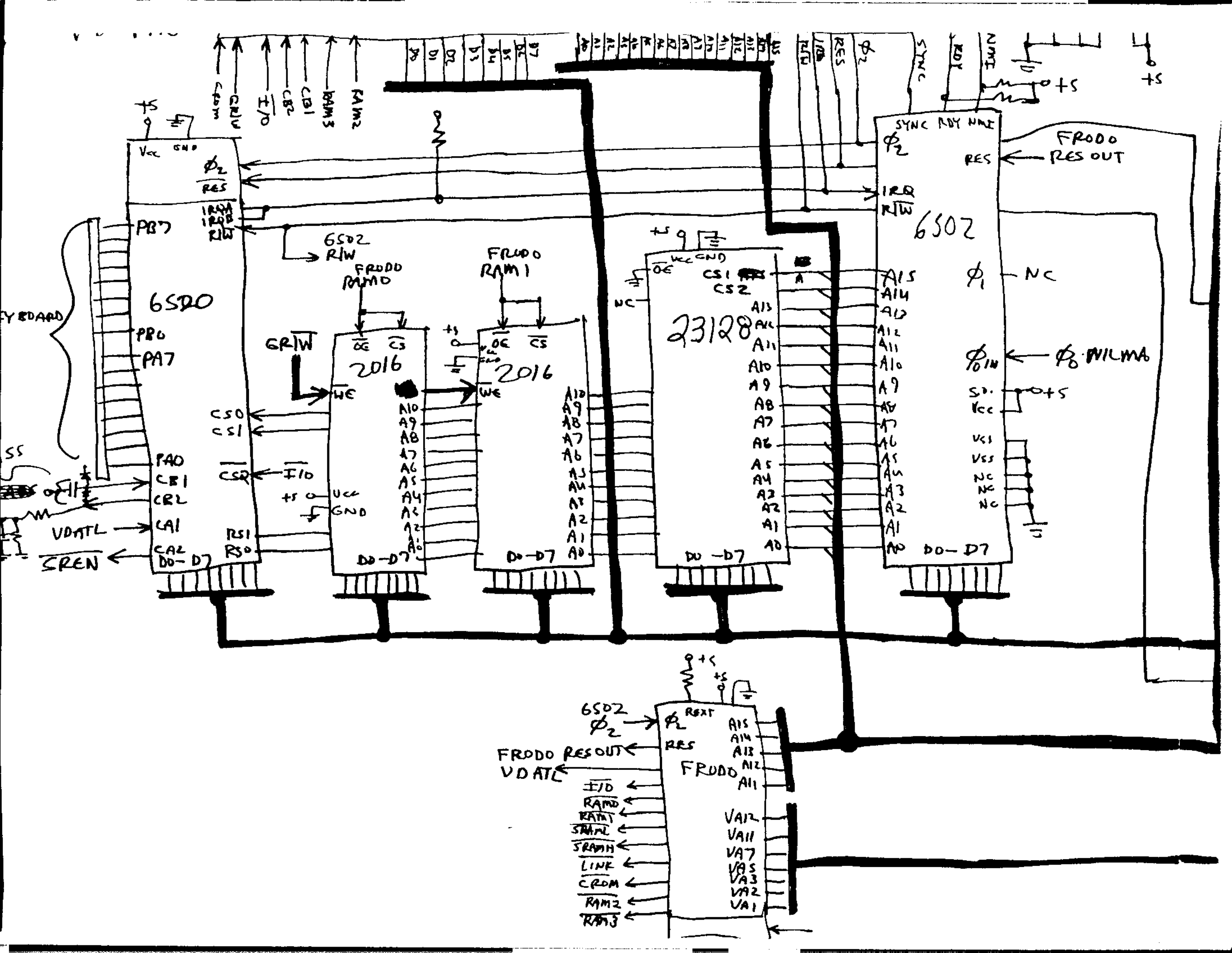
SWITCH A15, A14 INTO FRODO CHIP

CS OF 8K ROM GOES TO A15

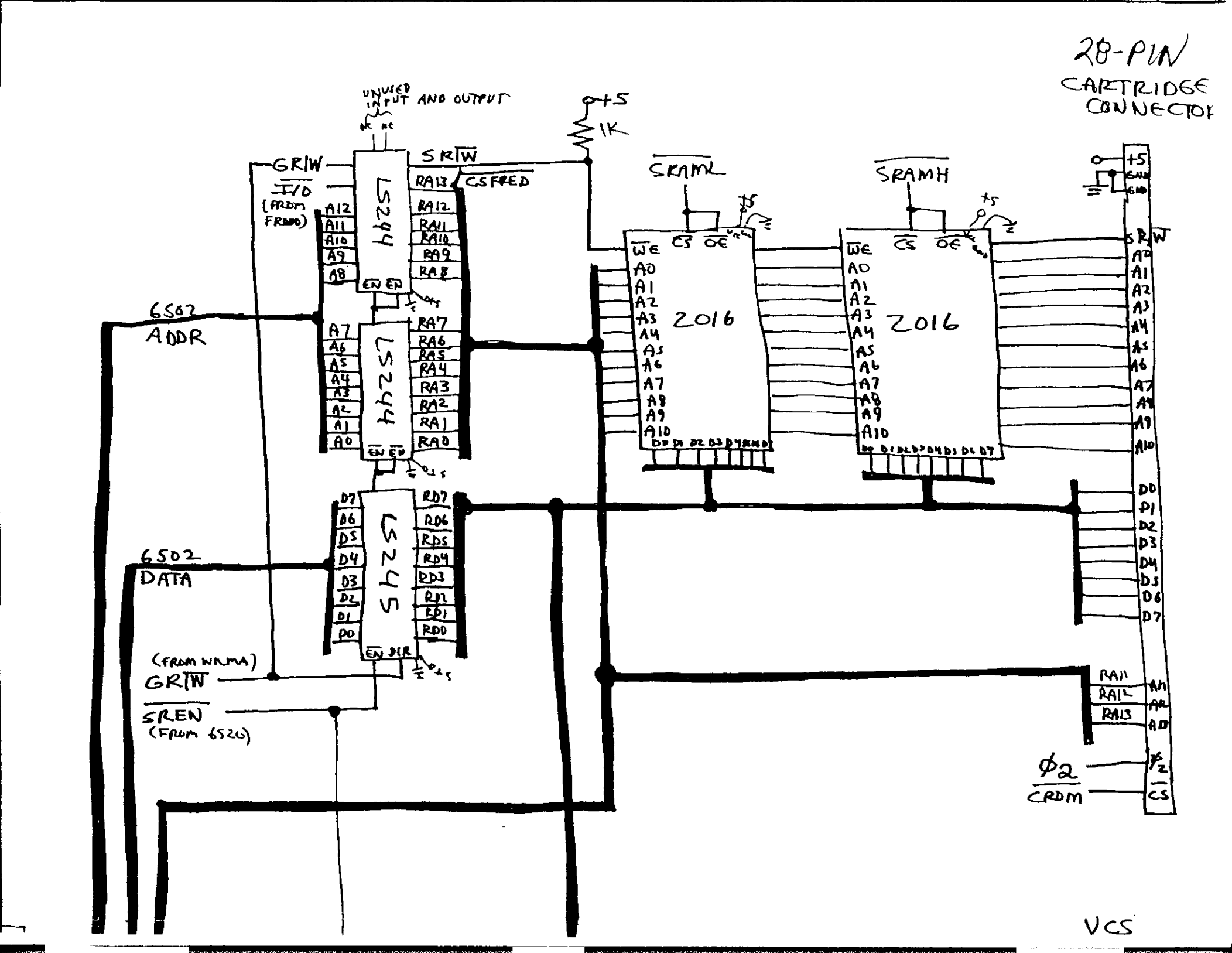


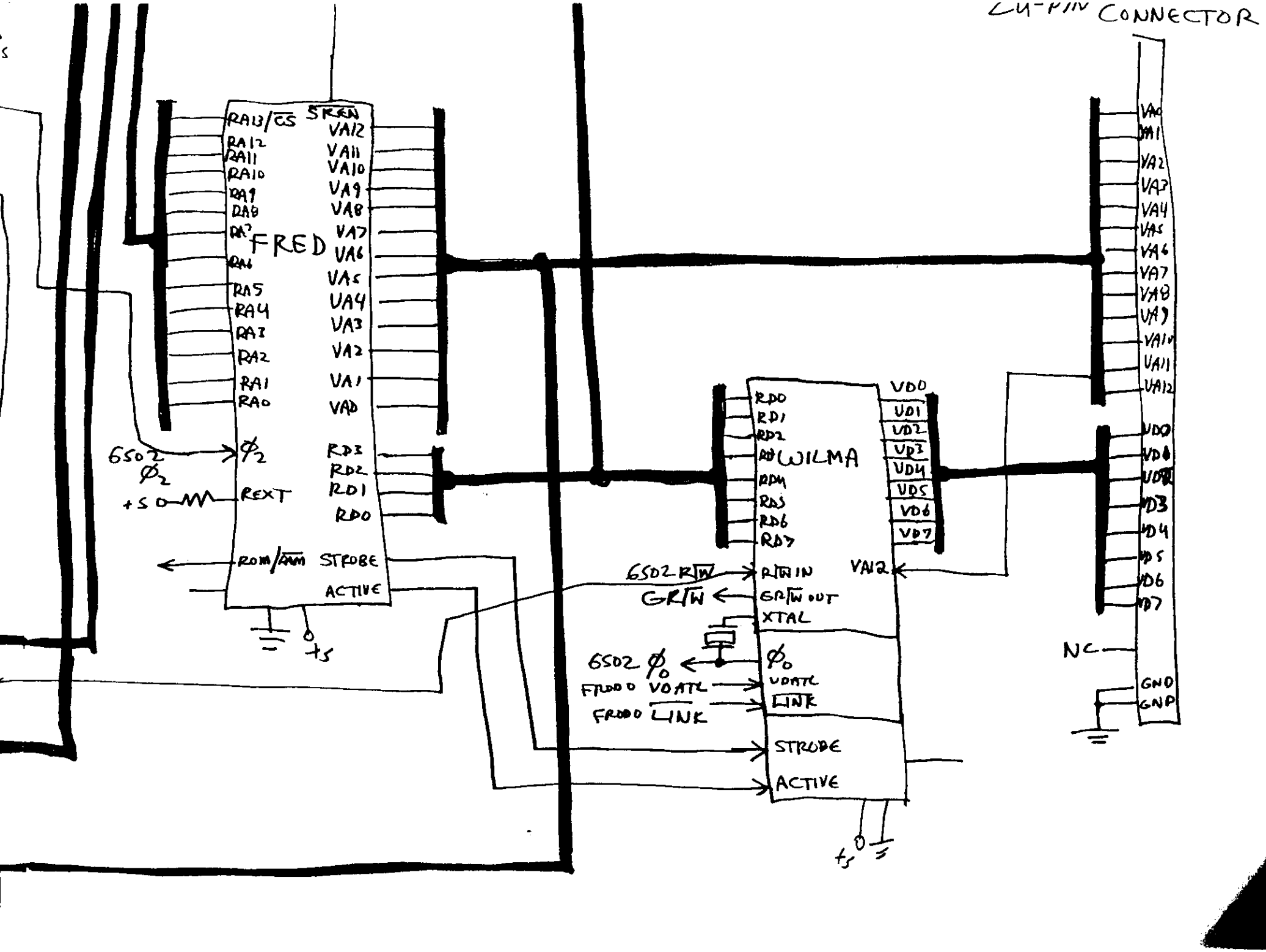


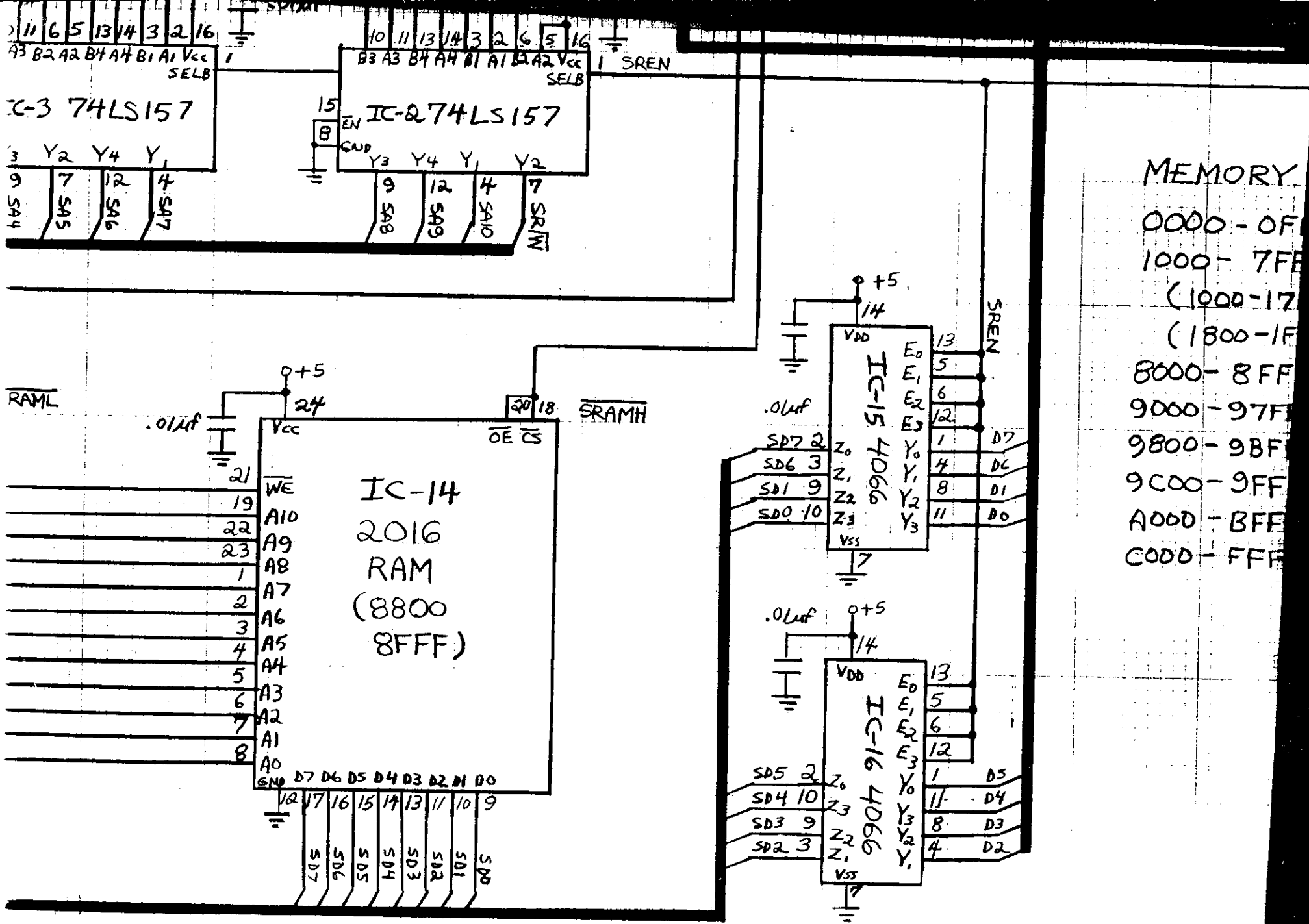
0000 – 07FF	2K RAM
0800 – 3FFF	14K EXPANSION
4000 – 47FF	2K SRAM
4800 – 4FFF	2K VCS ROM
5000 – 57FF	2K LINK
5800 – 5FFF	2K I/O
6000 – 7FFF	8K CROM
8000 – 9FFF	8K OSROM IMAGE
A000 – BFFF	8K OSROM IMAGE
C000 – DFFF	8K OSROM IMAGE
E000 – FFFF	8K OSROM

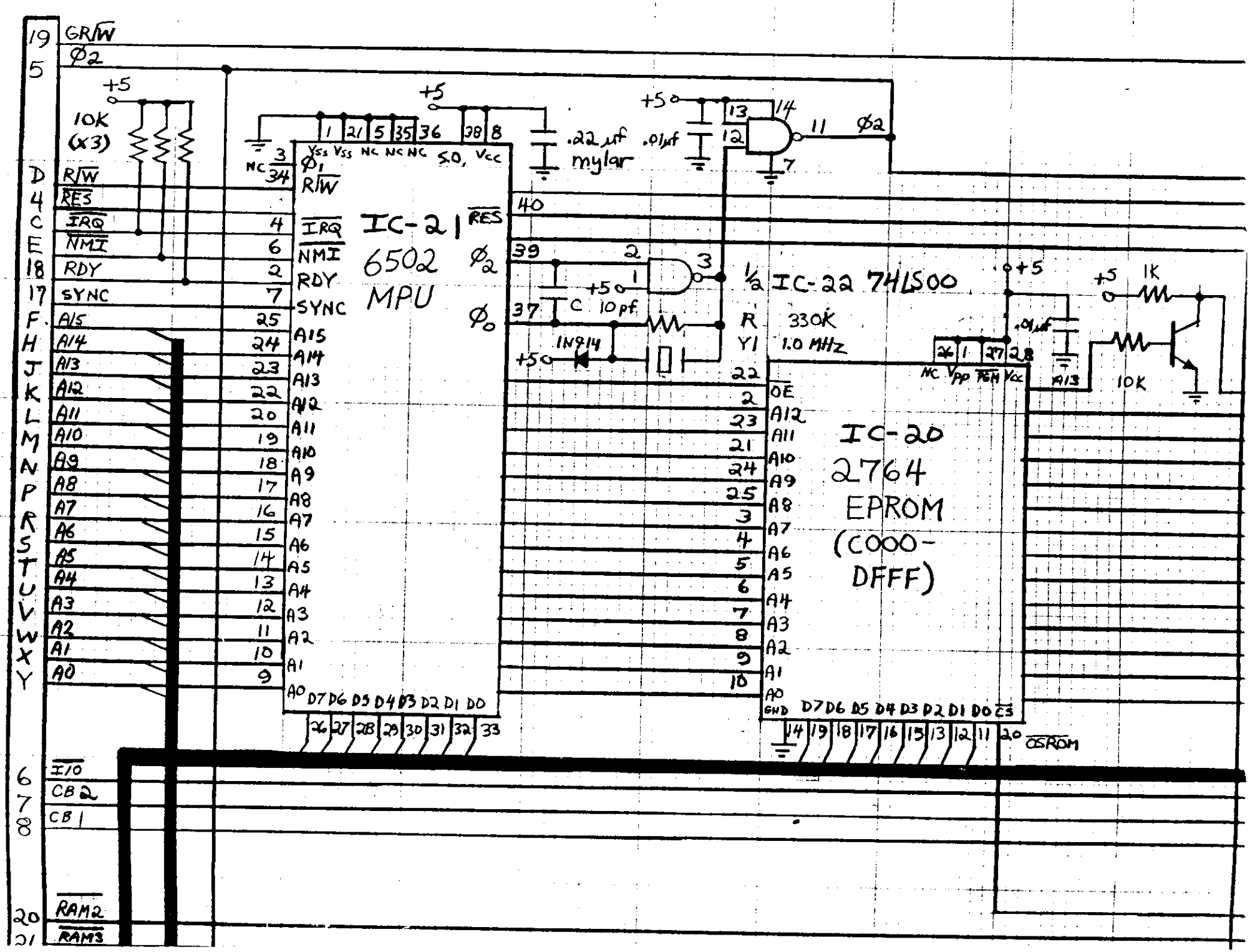


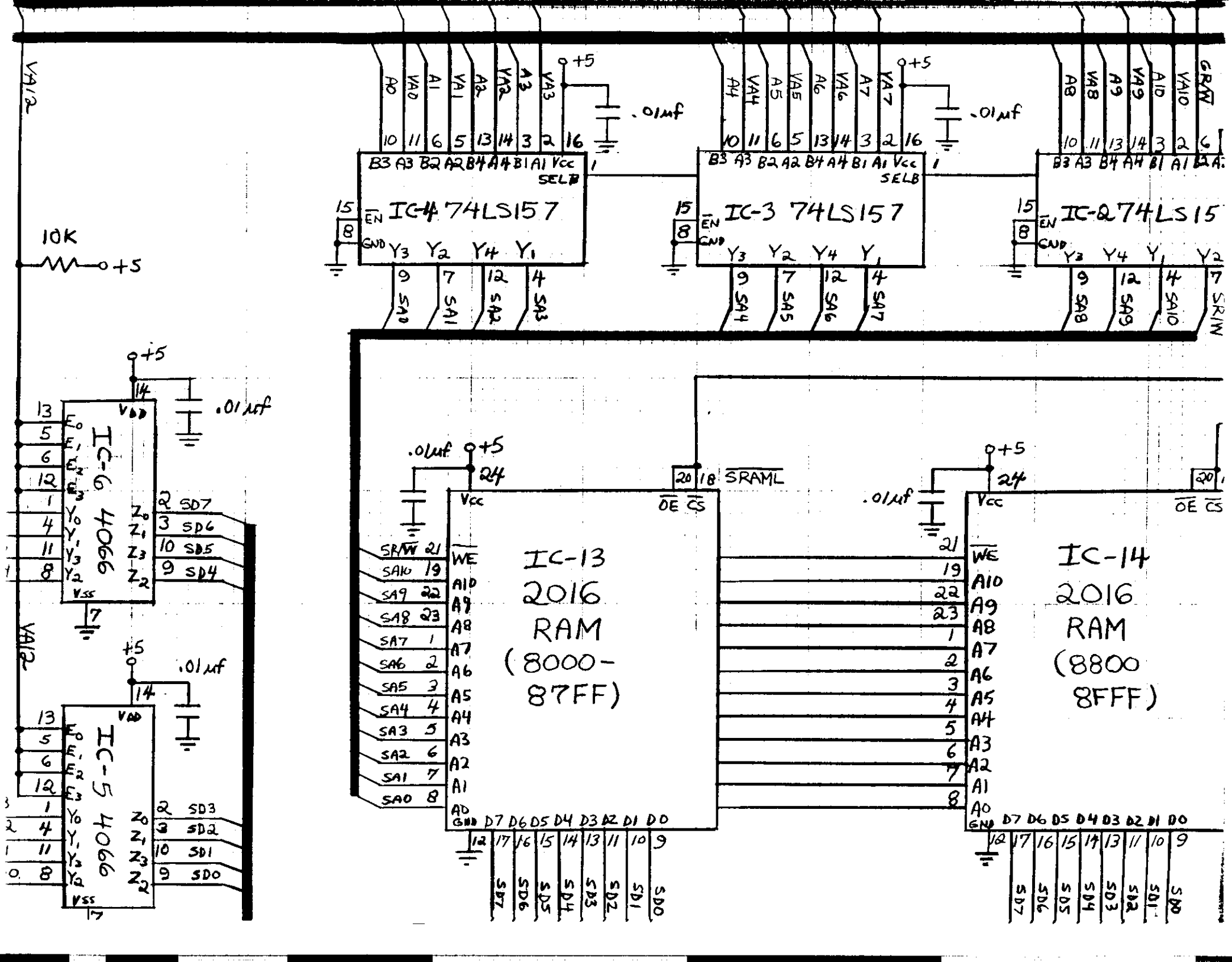
6502
6520
2016
2016
23128
FRODO
FRODO RES OUT
Φ0 WILMA
6502 R/W
FRODO RAM0
FRODO RAM1
GR/W
6502 Φ2
FRODO RES OUT
VDATL
VDATL
SREN
KEYBOARD

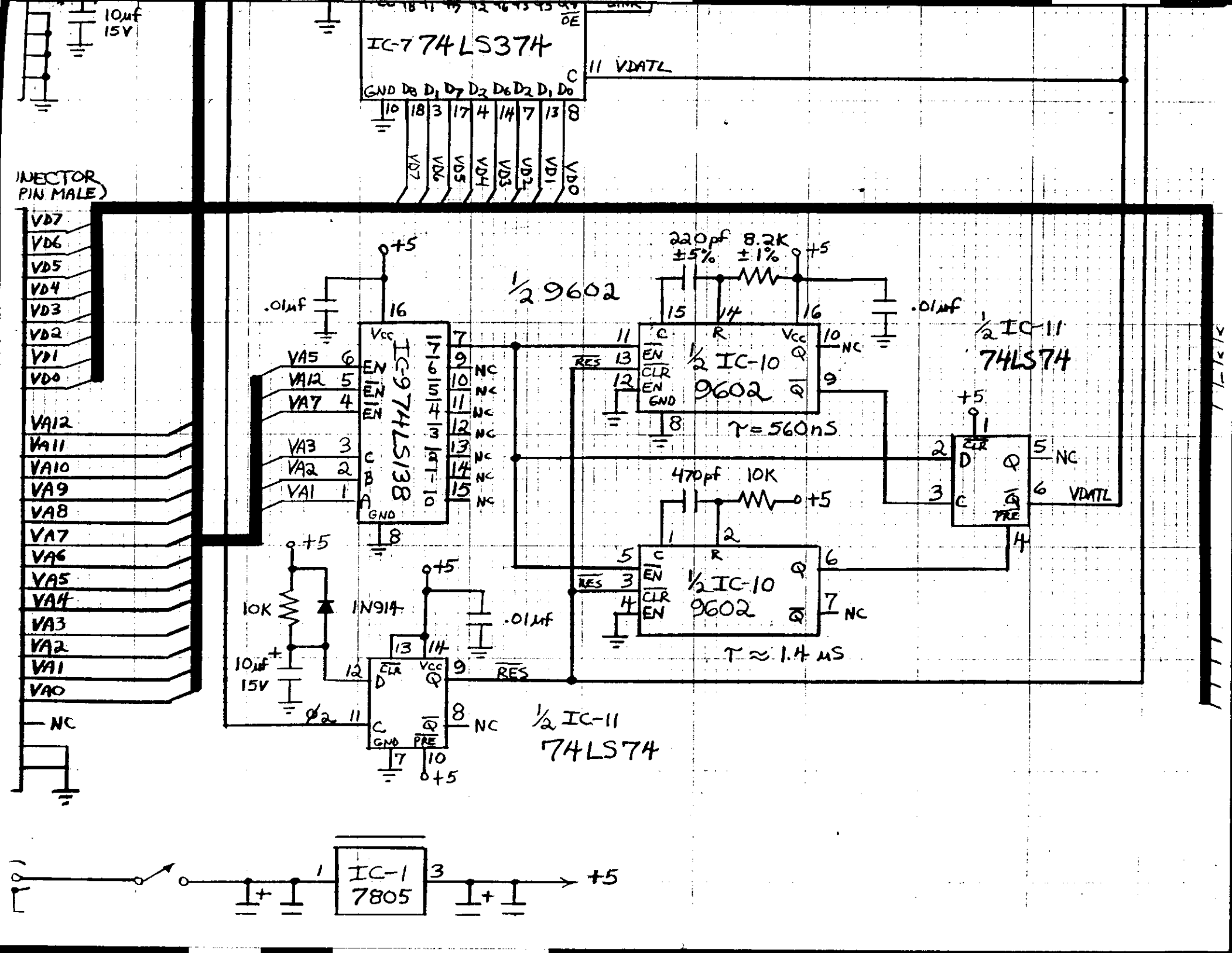

28-PIN
CARTRIDGE
CONNECTOR
UNUSED INPUT AND OUTPUT
+5
1K
GR/W
I/O
(FROM FRED)
SR/W
RA13
CSFRED
LS244
LS244
LS245
6502
ADDR
6502
DATA
(FROM WRAM)
GR/W
SREN
(FROM 6520)
SRAML
SRAMH
2016
2016
WE
CS
OE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
D0
D1
D2
D3
D4
D5
D6
D7
RA11
RA12
RA13
Φ2
CROM
VCS

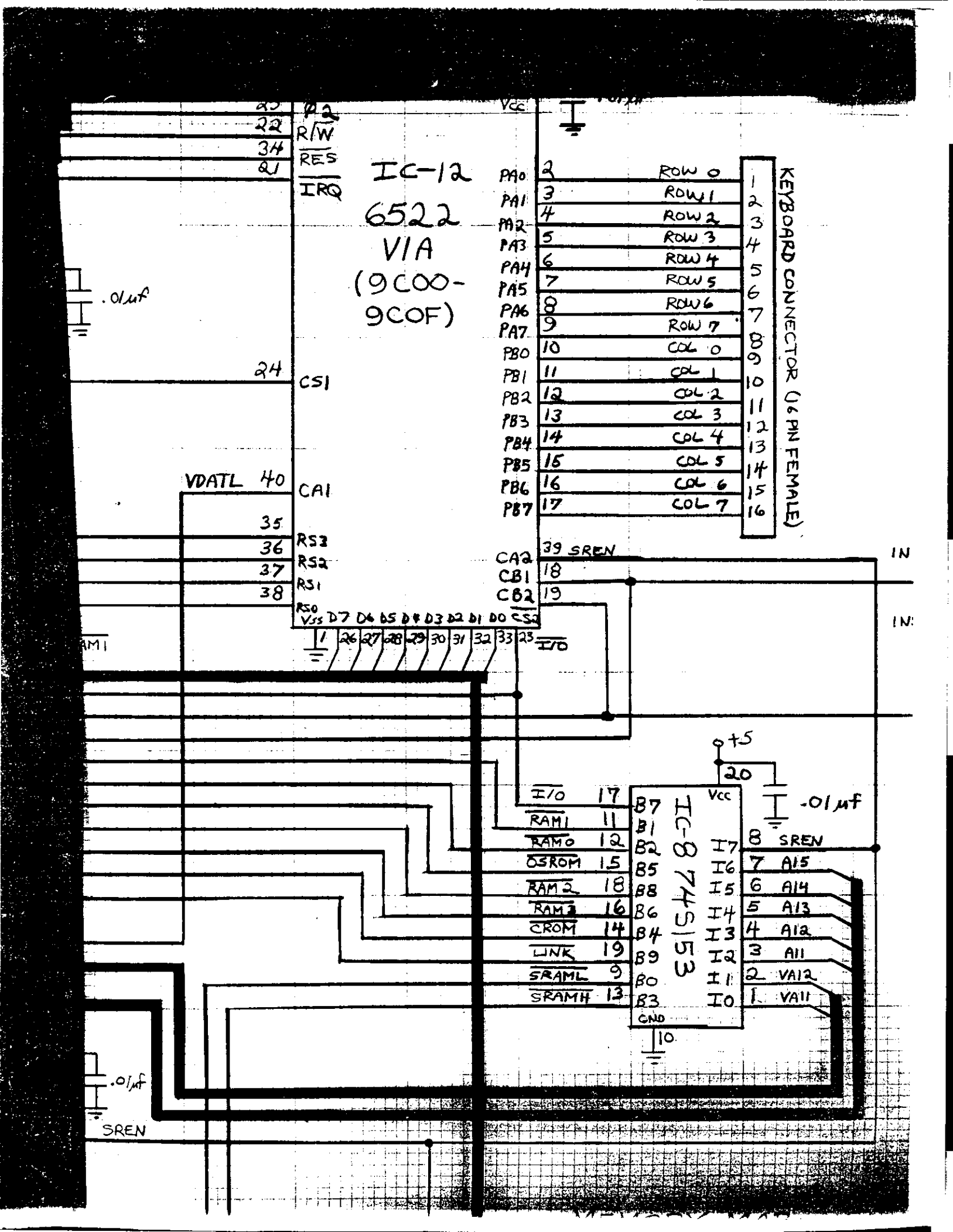

64-PIN CONNECTOR
FRED
RA13/CS
SREN
RA12
RA11
RA10
RA9
RA8
RA7
RA6
RA5
RA4
RA3
RA2
RA1
RA0
VA12
VA11
VA10
VA9
VA8
VA7
VA6
VA5
VA4
VA3
VA2
VA1
VA0
RD3
RD2
RD1
RD0
6502 Φ2
Φ2
+5
REXT
ROM/RAM
STROBE
ACTIVE
WILMA
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
VD0
VD1
VD2
VD3
VD4
VD5
VD6
VD7
6502 R/W
R/W IN
G R/W
G R/W OUT
XTAL
6502 Φ0
Φ0
FRODO VOLATE
VOLATE
FRODO LINK
LINK
STROBE
ACTIVE
VA12
NC
GND
GND


IC-3 74LS157
IC-2 74LS157
SELB
SREN
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SRAMH
RAML
+5
.01µf
IC-14
2016
RAM
(8800
8FFF)
IC-15 4066
IC-16 4066
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
D7
D6
D5
D4
D3
D2
D1
D0
MEMORY
0000 - 0F
1000 - 7FF
(1000-17
(1800-1F
8000 - 8FF
9000 - 97F
9800 - 9BF
9C00 - 9FF
A000 - BFF
C000 - FFF
CONTRACT NO.


EXPANSION CONNECTOR (44-PIN FEM
19 GR/W
5 Ø2
+5
10K (x3)
R/W
RES
IRQ
NMI
RDY
SYNC
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
I/O
CB2
CB1
RAM2
RAM3
IC-21
6502
MPU
Vss Vss NC NC NC SO, Vcc
Ø1
R/W
IRQ
NMI
RDY
SYNC
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7 D6 D5 D4 D3 D2 D1 D0
RES
Ø2
Ø0
.22 µf mylar
.01µf
C 10pf
IN914
R 330K
Y1 1.0 MHz
1/2 IC-22 74LS00
IC-20
2764
EPROM
(C000-DFFF)
OE
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
GND
D7 D6 D5 D4 D3 D2 D1 D0
CS
OSROM
NC Vpp PGM Vcc
A13
1K
10K


VA12
10K
+5
.01μf
IC-4 74LS157
IC-3 74LS157
IC-2 74LS15
B3 A3 B2 A2 B4 A4 B1 A1 Vcc
SELB
EN
GND
Y3 Y2 Y4 Y1
SA0 SA1 SA2 SA3
SA4 SA5 SA6 SA7
SA8 SA9 SA10 SRW
IC-6 4066
IC-5 4066
VDD
VSS
SD7 SD6 SD5 SD4
SD3 SD2 SD1 SD0
SRAML
IC-13 2016 RAM (8000-87FF)
IC-14 2016 RAM (8800 8FFF)
Vcc
GND
WE
OE CS
A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0


10µf 15V
IC-7 74LS374
OE
C
11 VDATL
GND D8 D1 D7 D2 D6 D2 D1 D0
10 18 3 17 4 14 7 13 8
VD7 VD6 VD5 VD4 VD3 VD2 VD1 VD0
INJECTOR PIN MALE
VD7 VD6 VD5 VD4 VD3 VD2 VD1 VD0
VA12 VA11 VA10 VA9 VA8 VA7 VA6 VA5 VA4 VA3 VA2 VA1 VA0
NC
+5
.01µf
16
Vcc
IC-9 74LS138
VA5 6
VA12 5
VA7 4
VA3 3
VA2 2
VA1 1
EN
EN
EN
C
B
A
GND
8
7 6 5 4 3 2 1 0
9 NC
10 NC
11 NC
12 NC
13 NC
14 NC
15 NC
1/2 9602
220pf ±5%
8.2K ±1%
+5
15 14 16
C R Vcc
RES 13
EN
CLR
EN
GND
12
8
11
10 NC
Q
9
Q
1/2 IC-10 9602
τ=560nS
.01µf
1/2 IC-11 74LS74
+5
1
CLR
2
D
Q
5 NC
3
C
Q
6 VDATL
PRE
4
470pf
10K
+5
1 2
5
C
R
EN
RES 3
CLR
EN
4
Q
6
Q
7 NC
1/2 IC-10 9602
τ≈1.4 mS
10K
IN914
+5
.01µf
10µf 15V
13 14
12
CLR
D
Vcc
Q
9
RES
Ø2 11
C
GND
Q
PRE
8 NC
7
10
+5
1/2 IC-11 74LS74
IC-1 7805
1
3
+5


IC-12
6522
VIA
(9C00-
9C0F)
Vcc
Φ2
R/W
RES
IRQ
.01μf
CS1
CA1
VDATL
RS3
RS2
RS1
RS0
Vss D7 D6 D5 D4 D3 D2 D1 D0 CS2
I/O
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7
CA2
CB1
CB2
SREN
ROW 0
ROW 1
ROW 2
ROW 3
ROW 4
ROW 5
ROW 6
ROW 7
COL 0
COL 1
COL 2
COL 3
COL 4
COL 5
COL 6
COL 7
KEYBOARD CONNECTOR (16 PIN FEMALE)
IN
IN:
+5
.01μf
IC-8 74LS153
B7 B1 B2 B5 B8 B6 B4 B9 B0 B3
I7 I6 I5 I4 I3 I2 I1 I0
GND
I/O
RAM1
RAM0
OSROM
RAM2
RAM3
CROM
LINK
SRAML
SRAMH
A15
A14
A13
A12
A11
VA12
VA11
SREN

* HOW TO WORK BANKING INFO INTO FRODO?

~~* HOW TO TELL WILMA THAT IT SHOULDN'T DRIVE DATA TO VCS IF VCS IS WORKING INTERNALLY~~

~~* NEED ROM CS FOR EXPANSION PORT~~

$$CROM = \overline{SREN} \cdot A14 \cdot \ldots \text{CPU ADDR}$$
$$+$$
$$SREN \cdot \$VROM \cdot \$$$
$$+$$
$$SREN \cdot \overline{VROM} \cdot \$ \text{ CPU ADDR}$$

NOTE: VCS CAN ADDRESS 16K BYTES OF ROM (4 CONTIGUOUS BANKS OF 4K BYTES)

OR 4K OF SHARED RAM:

		A13	A12
TRIGGER ADDRESSES:	ADDR 1 -	0	0
	ADDR 2 -	0	1
	ADDR 3 -	1	0
	ADDR 4 -	1	1
	ADDR 5 -	RAM	

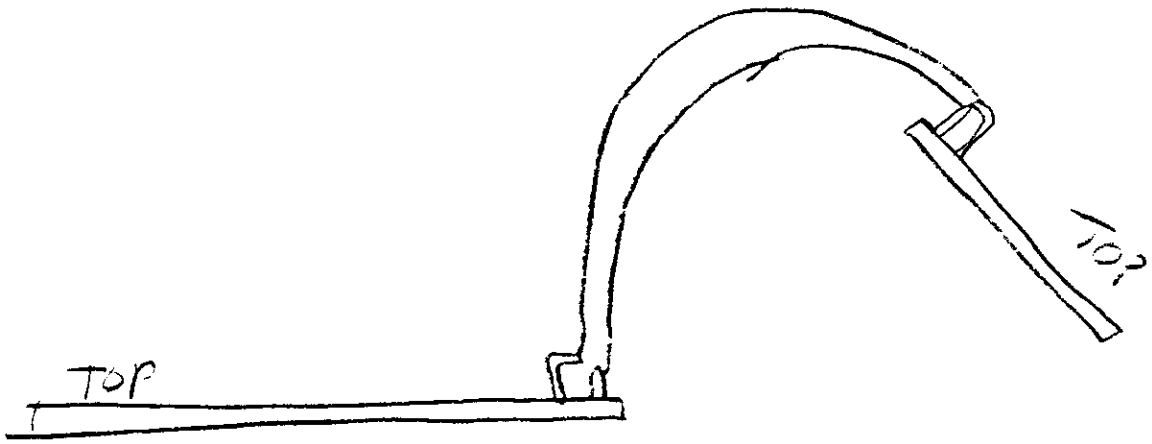
DELETED

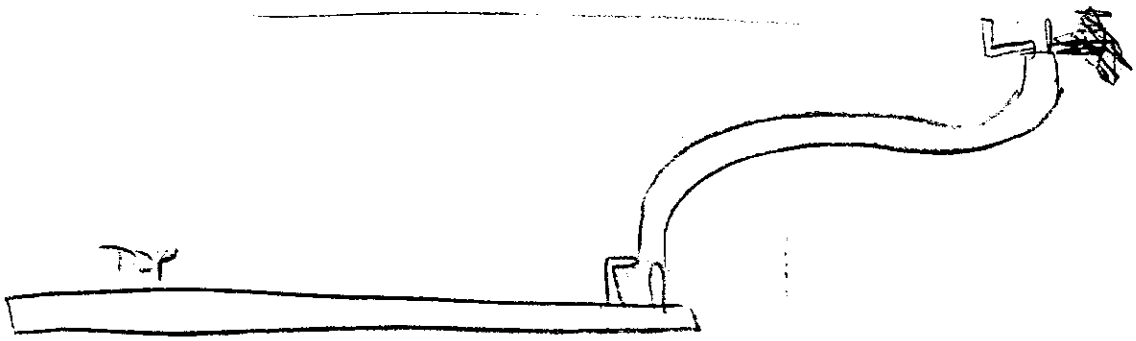
1 - 20	374	
3 - 16	157	
4 - 14	4086	
1 - 14	74LS00	
138	$\Delta = -10$	
1 - 28	ROM	
1 - 16	DECODER	
182		

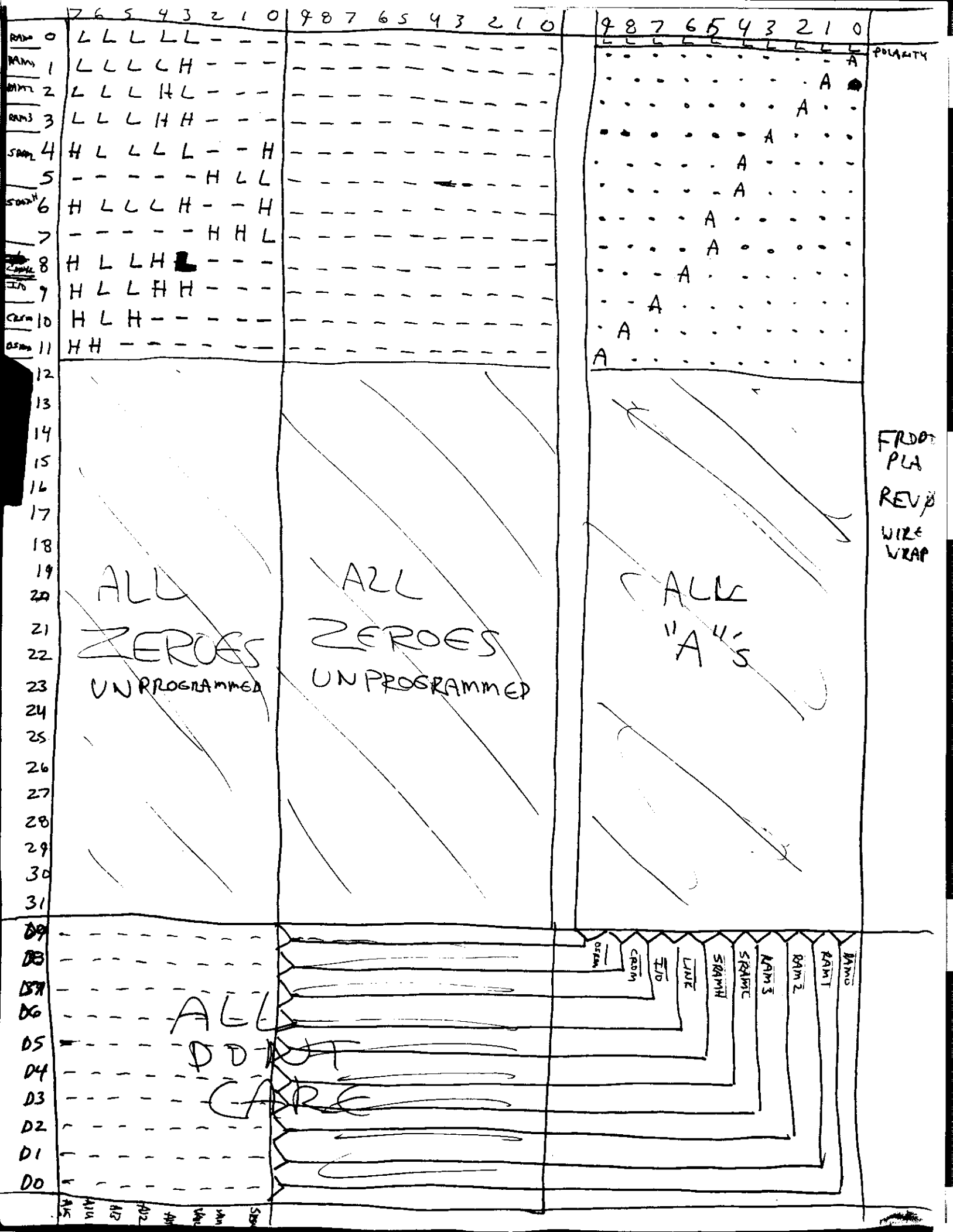
ADDED

1 - 40	
1 - 28	
3 - 20	
	128

$\Delta = -54$


TOP
TOP


TOP


7 6 5 4 3 2 1 0
9 8 7 6 5 4 3 2 1 0
9 8 7 6 5 4 3 2 1 0
POLARITY
FROM PLA REV Ø WIRE WRAP
ALL ZEROES UNPROGRAMMED
ALL ZEROES UNPROGRAMMED
CALL "A"S
ALL DON'T CARE
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
RAM0
RAM1
RAM2
RAM3
SRAM
SRAM
LINE
FID
CROM
DSTB

FIELD PROGRAMMABLE LOGIC ARRAY (18X32X10) 82S152 (O.C.)/82S153 (T.S.)

INTEGRATED FUSE LOGIC
SERIES 20

FPLA PROGRAM TABLE (Logic)