PARALLEL BUS INTERFACE

Specifications

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Draft of 2/3/83

1.0 THE PARALLEL BUS INTERFACE (PBI)

The Parallel Bus Interface Connector is a 50-pin connector (See figure 1.0) with the following signals:

PIN 3 through PIN 9 are A0 through A6 respectively. PIN 11 through PIN 18 are A7 through A14 respectively. PIN 20 is A15. These are the CPU address lines. The CPU addresses the Parallel Bus Interface devices using these lines.

PIN 21 through PIN 28 are D0 through D7 respectively. These are the processor data lines. The CPU transmits and receives data and control information from the Parallel Bus Interface devices on these lines.

PIN 31 is for the Buffered Phase 2 Clock (B02) Output to the Parallel Bus Interface devices.

PIN 35 is the $\overline{IRQ}$ (Interrupt Request) input from the Parallel Bus Interface devices. A PBI device can pull this input low to invoke the device handler that services the parallel bus device. This input is "open drain".

PIN 46 is the Latched Read/Write (LR/$\overline{W}$) Output to the Parallel Bus Interface devices. This line is "high" for a read cycle. It is "low" for a write cycle.

PIN 34 is the Reset ($\overline{POR}$) output to the Parallel Bus Interface devices. This output resets any device so designed on power up and when the RESET key on the CPU keyboard is hit.

PIN 49 is audio in signal from the Parallel Bus devices. This line is connected directly to the audio summation network of the CPU. The audio signal is 1 volt Peak to Peak.

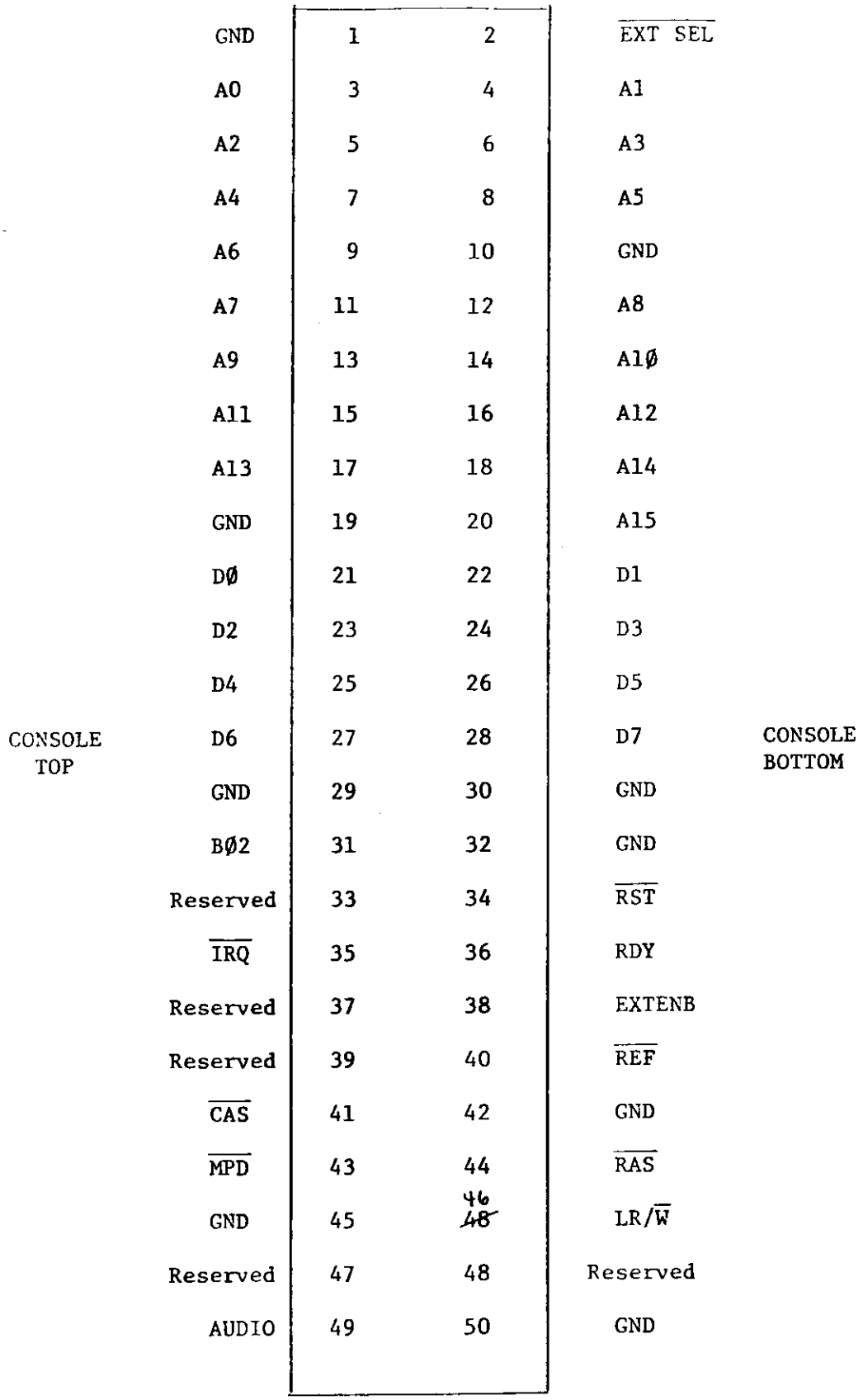


FIGURE 1.0 PBI CONNECTOR
(Looking into the CPU Connector)

PIN 38 is External Decoder Enable (EXTENB) Output. This output goes high when an address on the CPU bus is an allowed address for a PBI device. The CPU generates the EXTENB signal for all segments of the CPU memory map except:

(a) The Active segments of the O.S. ROM. Any disabled segments of the O.S. ROM generate the EXTENB signal when addressed.

(b) The region occupied by the internal cartridge (if present).

PIN 2 is the External Select ($\overline{\text{EXTSEL}}$) Input. This input is generated by the (external) decoder resident in the PBI device. This signal should go low whenever the EXTENB is enabled and the selected PBI device uses the address generated on the CPU Bus. This input is used to disable the CPU decoder for the duration of the current bus cycle.

PIN 36 is the RDY input to the CPU. A slow PBI device can extend the CPU bus cycle by pulling this line low when it is addressed.

PIN 40 is the Refresh ($\overline{\text{REF}}$) output. This output may be used for the refresh timing of voltile memories connected to the PBI.

PIN 43 is Math Pak Disable ($\overline{\text{MPD}}$) input from the PBI devices. This input is pulled to the "low" state whenever a Parallel Bus device is selected by the CPU and the device has a handler resident in the region D800H to DFFFH.

PIN 44 is ROW Address Strobe ($\overline{\text{RAS}}$) output to the Parallel Bus devices. This output may be used for external memory expansion.

PIN 41 is the Column Address Strobe ($\overline{\text{CAS}}$) output to the Parallel Bus devices. This output may be used for external memory expansion.

PINS 33, 37, 39, 47 and 48 are reserved.

PINS 1, 10, 19, 29, 30, 32, 42, 45 and 50 are Signal grounds (GND).

ELECTRICAL LEVELS:

D. C. Characteristics

All PBI outputs from the CPU will have the capability of driving one LSTTL gate.

All PBI inputs except $\overline{\text{IRQ}}$ should have the drive capability of the output of an LSTTL gate.

The $\overline{\text{IRQ}}$ input is "open drain" and in the "low" state should present the following characteristics:

V = 0.4V (max) I = 1.6mA (min Sink current)

AC Characteristics

To be specified.

2.0 Parallel Bus Devices

The Parallel bus will support three types of devices:

2.1 External Memory:

The PBI will allow the user to expand the local RAM externally to up to 64K. This will allow external memory expansion of a 16K CPU.

2.2 Parallel Bus Peripherals (PBPs)

The PBPs have the following characteristics:

(a) They interface to the CPU through a well defined handler/O.S. interface. The code for this interface is resident in CPU memory location D600H to D7FFH (COMM A & COMM B areas). The ROM containing this code is physically located in a Parallel Bus Adapter. (See Section 3.0)

The O.S. can support up to 8 PBPs at one time.

(b) Each PBP has a unique handler that resides in the CPU memory space at locations D800H to DFFFH. The ROMs containing the code for these handlers are physically resident in the respective peripherals. (The memory space occupied by the handlers actually contains the Math-pak within the S-16. The Math-pak is disabled whenever any EBP is enabled. See (c) below).

(c) Location D1FFH in the CPU memory map is reserved for passing control information between the CPU and the PBPs.

The CPU linearly selects the PBI devices by writing into location D1FFH.

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	DØ	Location D1FFH.

Writing a "1" into Dx (x=0 to 7) selects device Dx (x=0 to 7).
Writing a "0" into Dx (x=0 to 7) de-selects device Dx (x=0 to 7).

The CPU can thus select up to 8 PBI devices.

If the $\overline{IRQ}$ line is pulled "low" the CPU polls location D1FFH. A read from this location returns the PBI devices' interrupt status.

7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	IØ

2.2 Parallel Bus Peripherals (PBPs) (continued)

(c) continued....

If bit Ix (x=0 to 7) is "1", then device Dx (x=0 to 7) has interrupted. If bit Ix (x=0 to 7) is "0" then device Dx (x=0 to 7) has not interrupted. The device is required to clear its interrupt status bit when its interrupt is serviced by the CPU.

(d) The PBPs should assert $\overline{\text{MPD}}$ only when they are selected. The PBPs should assert $\overline{\text{EXTSEL}}$ only when they are selected and if EXTENB is asserted.

(e) The PBPs may respond to any one of the selects D1 through D7. It is recommended that the PBPs have configuration switches to allow them to respond to any one of the selects D1 through D7. The PBPs should not respond to device select DØ. DØ is reserved for use by Atari.

(f) A peripheral handler may respond to address in the region D800H-DFFH only when it is selected. Location D800H contains the device I.D. of an PBP. If a slot that contains no peripheral is selected, address D800H should return FFH as data.

(g) A peripheral may respond to addresses in the region D100H to D1FEH only when it is selected.

(h) The PBPs will have priority over the SIO peripheral when they are addressed generically.

(i) The data between the CPU and an PBP is passed under the control of the peripheral handler for the PBPs.

(j) The PBPs will work if a cartridge is present in the cartridge slot.

2.3 "External Application" Cartridges:

The External Application Cartridge are a generalization of the PBPs. They have the following characteristics:

(a) An "External Applications" Cartridge (EAC) can reside at any or all of the addresses in the region 0000H to BFFFH for which the EXTENB is generated. They may respond to these addresses only when "opened."

(b) The EACs must be "opened" by the S-16 through the slot select location in the same was as the PBPs.

(c) The EACs must conform to the EXTENB/EXTSEL protocol.

2.3 "External Application" Cartridges: (continued)

(d) The EACs must have a "handler" (resident in locations D800H to DFFFH) that controls their operation. The EACs must conform to conditions (d) thru (g) of Section 2.2 above.

(e) The EACs will work if a cartridge is present in the internal cartridge slot.

3.0 THE PBI ADAPTER CONCEPT:

The use of the PBI shall require a PBI adapter. The PBI adapter shall provide, at a minimum, the following:

(1) Buffers for the Address, Data, LR/$\overline{W}$, BØ2, $\overline{RAS}$, $\overline{CAS}$, $\overline{RST}$, $\overline{REF}$ and EXTENB Signals.

(2) 512 bytes of ROM that contain code for the CPU's software interface to the PBPs. This code is resident in locations D600 to D7FF in the CPU memory map. The Adapter will have to decode this address space to generate Chip Select for the ROM.

Any PBI device that does not use the PBI adapter will have to provide (1) above. It will also have to provide (2) above if it is a PBP or an EAC.

The PBI adapter may optionally provide the following in addition to (1) and (2) above:

(a) RAM memory expansion for a CPU that has less than 64K RAM.

(b) Device Select address decode (DIFFH and write). This decode may be bussed to the PBI devices connected after the adapter on one of the reserved lines.

(c) IRQ Status decode (DIFF and read). This decode may be bussed to the PBI devices connected after the adapter on one of the reserved lines.

(d) Power Supply to support the PBI devices connected to the adapter. Such a power supply may source +5, +12 and -12V. These power signals may be bussed to devices connected after the adapter on reserved lines.

Parallel Bus Interface

Specfications

Steve Miller

4/XX/83

I. Introduction

The Parallel Bus Interface (PBI) is method to extend the bus of the ATARI Surely series computers for expansion and enhancement. It will provide a standard interface to peripherals using the expansion box or stand alone unit. This feature will then allow other peripheral manufacturers to design special devices for a limited applications where it would not be profitable for ATARI. Using the PBI as a upgrade path for the smaller computers, the novice can expand their system as their needs grow. An example of this is a ram expansion for the 600 allowing for a full 64K. Due to timing restrictions only one device can be connected to the bus at any one time with the exclusion of the ram module for the 600. Thus to allow for many devices there must be a expansion box.

A. References

(1) S-16 Expansion Box Specfication A.Chopra
(2) Parallel Bus Interface A.Chopra

II. Bus Definition

A. Connector

The PBI signals will be accessible by a 50-pin connection on the computer. This connection consists of a 50-pin, gold plated, card edge (25-pins on each side) with .100 inch centers. It will mate to a standard .100 center 25-dual position circuit connector (i.e. AMP 67987-4) as in figure 1.

Post Size: .025" square

Housing Material: Green glass-filled polyester

Contact Material: Copper alloy 725

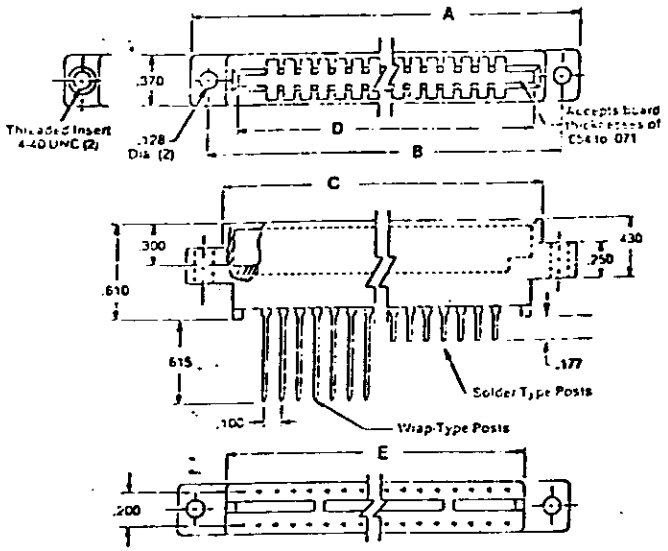
Contact Finish: Selectively plated gold flash on post for solderability. See table below for plating thickness on contact area. Gold plating per MIL-G-45240, Type II

Replacement Contacts: .000015" gold plated, Part No. 1-67957-5; .000050" gold plated, Part No. 1-67957-7

Polarizing Keys: Nylon material—Intercontact Type, Part No. 67654-4; 67343

Threaded Insert: Brass, 4-40 UNC

Housing Marking: Marking shown on previous page is standard.



No. of Dual Positions	Dimensions A	B	C	D	E	Contact Plating*	Connector Part Nos. for Wrap-Type Posts: Without Threaded Inserts	With Threaded Inserts	Connector Part Nos. for Solder Type Posts: Without Threaded Inserts	With Threaded Inserts
15	2.34	2.075	1.76	1.600	1.65	.000015	67972-1	67974-1	67987-1	67994-1
						.000050	4-67972-1	4-67974-1	4-67987-1	4-67994-1
18	2.64	2.375	2.06	1.900	1.95	.000015	67972-2	67974-2	67987-2	67994-2
						.000050	4-67972-2	4-67974-2	4-67987-2	4-67994-2
22	3.04	2.775	2.46	2.300	2.35	.000015	67972-3	67974-3	67987-3	67994-3
						.000050	4-67972-3	4-67974-3	4-67987-3	4-67994-3
25	3.34	3.075	2.76	2.600	2.65	.000015	67972-4	67974-4	67987-4	67994-4
						.000050	4-67972-4	4-67974-4	4-67987-4	4-67994-4
28	3.64	3.375	3.06	2.900	2.95	.000015	67972-5	67974-5	67987-5	67994-5
						.000050	4-67972-5	4-67974-5	4-67987-5	4-67994-5
30	3.84	3.575	3.26	3.100	3.15	.000015	67972-6	67974-6	67987-6	67994-6
						.000050	4-67972-6	4-67974-6	4-67987-6	4-67994-6
31	3.94	3.675	3.36	3.200	3.25	.000015	67972-7	67974-7	67987-7	67994-7
						.000050	4-67972-7	4-67974-7	4-67987-7	4-67994-7
35	4.34	4.075	3.76	3.600	3.65	.000015	67972-8	67974-8	67987-8	67994-8
						.000050	4-67972-8	4-67974-8	4-67987-8	4-67994-8
36	4.44	4.175	3.86	3.700	3.75	.000015	67972-9	67974-9	67987-9	67994-9
						.000050	4-67972-9	4-67974-9	4-67987-9	4-67994-9
40	4.84	4.575	4.26	4.100	4.15	.000015	5-67972-0	5-67974-0	5-67987-0	5-67994-0
						.000050	5-67972-0	5-67974-0	5-67987-0	5-67994-0
43	5.14	4.875	4.56	4.400	4.45	.000015	5-67972-1	5-67974-1	5-67987-1	5-67994-1
						.000050	5-67972-1	5-67974-1	5-67987-1	5-67994-1
50	5.84	5.575	5.26	5.100	5.15	.000015	5-67972-2	5-67974-2	5-67987-2	5-67994-2
						.000050	5-67972-2	5-67974-2	5-67987-2	5-67994-2
60	6.84	6.575	6.26	6.100	6.15	.000015	5-67972-3	5-67974-3	5-67987-3	5-67994-3
						.000050	5-67972-3	5-67974-3	5-67987-3	5-67994-3

*Minimum gold plating thickness on contact area.
Note: Connectors with contacts having .000030" min. gold plating on contact area are also available. Consult AMP Incorporated.
• Normally shipped within 3 days ARD.

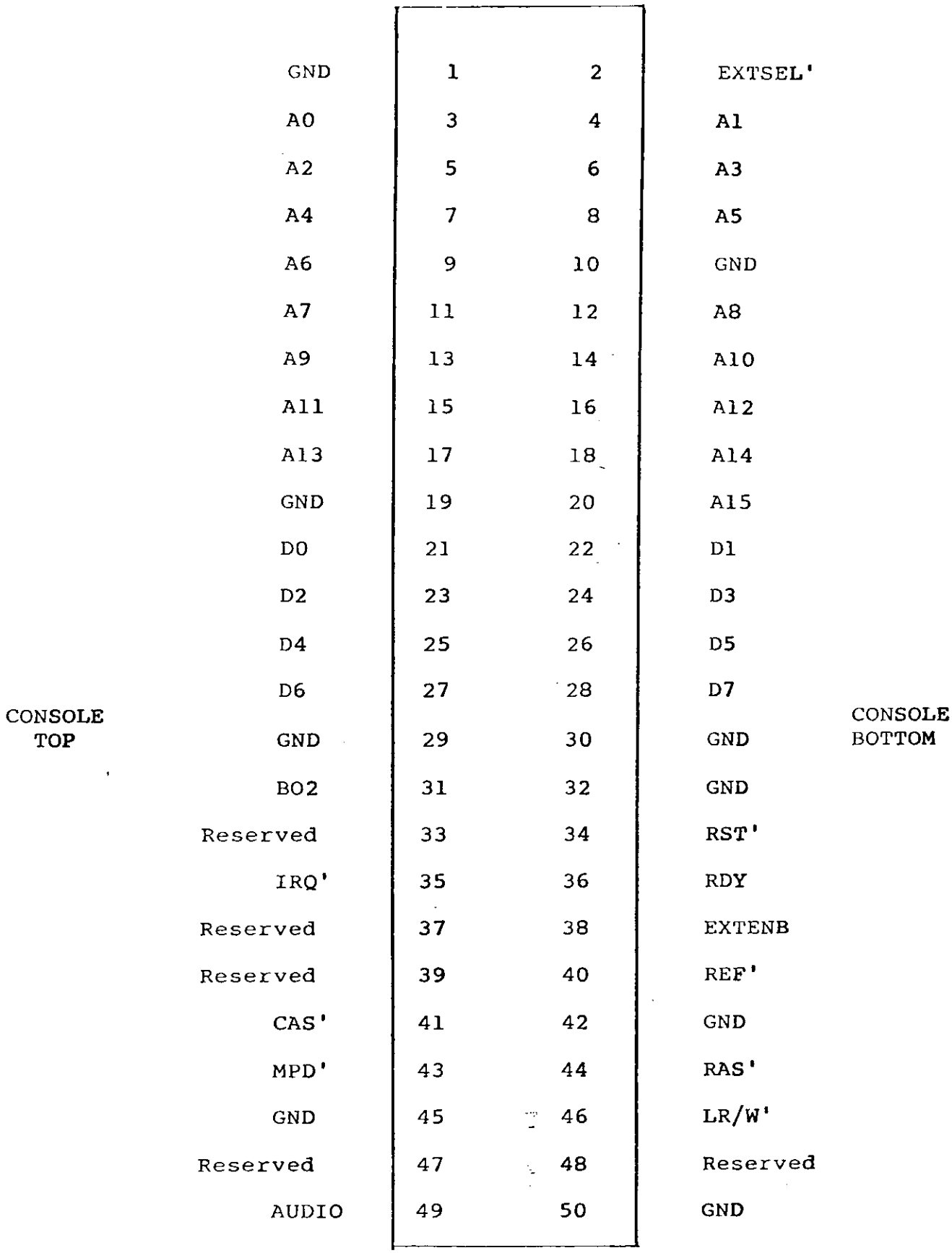


Figure 2 PBI Connector
(Looking into the Computer)

B. Signals

Shown in figure 2 is the pin-out of the connector looking into the computer. The signal pin numbers and signal names are described below.

Pin 2	EXTSEL'	External Select (Input) ==> This open collector line is generated internally by the Parallel Bus Device (PBD). This signal should be active low whenever EXTENB is active and the PBD is selected and there is a valid PBD address on the bus. EXSEL' causes a CAS' inhibit on the main board allowing a remapping process. Although PBD can be mapped in any VALID RAM location, these devices should follow the ATARI guidelines for PBD locations so future ATARI devices can be used. The drive device should be capable of sinking 5 mA.
Pin 3	A0	Address Line 0 (Output) ==> Address line 0 is a unbuffered output from the microprocessor.
Pin 4	A1	Address Line 1 (Output) ==> Address line 1 is a unbuffered output from the microprocessor.
Pin 5	A2	Address Line 2 (Output) ==> Address line 2 is a unbuffered output from the microprocessor.
Pin 6	A3	Address Line 3 (Output) ==> Address line 3 is a unbuffered output from the microprocessor.
Pin 7	A4	Address Line 4 (Output) ==> Address line 4 is a unbuffered output from the microprocessor.
Pin 8	A5	Address Line 5 (Output) ==> Address line 5 is a unbuffered output from the microprocessor.
Pin 9	A6	Address Line 6 (Output) ==> Address line 6 is a unbuffered output from the microprocessor.
Pin 11	A7	Address Line 7 (Output) ==> Address line 7 is a unbuffered output from the microprocessor.

Pin 12	A8	Address Line 8 (Output) ==> Address line 8 is a unbuffered output from the microprocessor.
Pin 13	A9	Address Line 9 (Output) ==> Address line 9 is a unbuffered output from the microprocessor.
Pin 14	A10	Address Line 10 (Output) ==> Address line 10 is a unbuffered output from the microprocessor.
Pin 15	A11	Address Line 11 (Output) ==> Address line 11 is a unbuffered output from the microprocessor.
Pin 16	A12	Address Line 12 (Output) ==> Address line 12 is a unbuffered output from the microprocessor.
Pin 17	A13	Address Line 13 (Output) ==> Address line 13 is a unbuffered output from the microprocessor.
Pin 18	A14	Address Line 14 (Output) ==> Address line 14 is a unbuffered output from the microprocessor.
Pin 20	A15	Address Line 15 (Output) ==> Address line 15 is a unbuffered output from the microprocessor.
Pin 21	D0	Data Line 0 (Bi-directional) ==> Data line 0 is a buffered line in the 12XX models and unbuffered in the 600 and 800 computers.
Pin 22	D1	Data Line 1 (Bi-directional) ==> Data line 1 is a buffered line in the 12XX models and unbuffered in the 600 and 800 computers.
Pin 23	D2	Data Line 2 (Bi-directional) ==> Data line 2 is a buffered line in the 12XX models and unbuffered in the 600 and 800 computers.
Pin 24	D3	Data Line 3 (Bi-directional) ==> Data line 3 is a buffered line in the 12XX models and unbuffered in the 600 and 800 computers.

Pin 25	D4	Data Line 4 (Bi-directional) ==> Data line 4 is a buffered line in the 12XX models and unbuffered in the 600 and 800 computers.
Pin 26	D5	Data Line 5 (Bi-directional) ==> Data line 5 is a buffered line in the 12XX models and unbuffered in the 600 and 800 computers.
Pin 27	D6	Data Line 6 (Bi-directional) ==> Data line 6 is a buffered line in the 12XX models and unbuffered in the 600 and 800 computers.
Pin 28	D7	Data Line 7 (Bi-directional) ==> Data line 7 is a buffered line in the 12XX models and unbuffered in the 600 and 800 computers.
Pin 31	BO2	Buffered Phase 2 Clock (Output) ==> This clock output line is a buffered phase 2 clock from the processor.
Pin 34	RST'	Reset (Output) ==> Reset is a active low signal which occurs either on power-up or by depressing the reset key.
Pin 35	IRQ'	Interrupt Request (Input) ==> This open collector line creates a interrupt on the microprocessor. The interrupt can then invoke the handler rom or other service routines for the PBD. The driving device should be capable of sinking 5 mA.
Pin 36	RDY	Ready (Input) ==> This open collector input signal allows the PBD to halt the microprocessor ONLY during read cycles. This will extend the read cycle for slow peripherals. The driving device should be capable of sinking 5 mA.
Pin 38	EXTENB	External Decoder Enable (Output) ==> This output goes high when there is a valid ram access. Any PBD can map during a valid EXTENB but the PBD should only map in according to ATARI specified address locations.

Pin 40	REF'	Refresh (Output) ==>This output can be for refresh timing on voltile memories connected to the PBI.
Pin 41	CAS'	Column Address Strobe (Output) ==> This output can be used for access of DRAM external to the computer. Due to timing restrictions caution should be taken when using this signal in the expansion box.
Pin 43	MPD'	Math Pack Disable (Input) ==> This open collector input is used to disable the math pack section of the OS rom (D800H-DFFFH). This should be done when the PBD is selected and has a handler resident. The driving device should be capable of sinking 5 mA.
Pin 44	RAS'	Row Address Strobe (Output) ==> This output can be used for access of DRAM external to the computer. Due to timing restrictions caution should be taken when using this signal in the expansion box.
Pin 46	LR/W'	Latched Read Write (Output) ==> This output is active high for a read cycle and active low for a write cycle.
Pin 49	AUDIO	Audio In (Input) ==> This line is tied directly to the audio summation network of the computer. The audio signal input is 1 V peak to peak with 1K ohm input impedance.
Pins 1,10,19,29,30,32,42,45,50		GND
Pins 33,37,39,47,48		Reserved

III. Parallel Bus Devices

The PBI is designed to support two types of devices which are the expansion box and external ram for the 600. The expansion box supports both PBD and external application cartridges.

A. External Ram

The PBI will allow the user to expand ram externally up to 64K. This feature can only be used in the 600 since all other units are already equiped with 64K.

B. Parallel Bus Peripherals (PBP)

The PBPs have the following characteristics:

1. The interface between the PBP and the CPU is defined through the handler/OS resident in the OS rom. The OS can support 8 devices at one time with only one enabled at any given interval.

2. Every PBP has a unique handler that resides in the CPU memory from D800H-DFFFH. The roms containing the code for these handlers are physically resident on the respective PBPs. To access this handler, the math pack must be disabled with MPD'. When the math pack is disabled (this should happen whenever the PBP is selected and has a external handler) the computer will generate EXTENB for the math pack area. The PBP must the generate the correct EXTENB|EXTSEL' protocol. If the device does not generate EXTSEL' the CPU will access (in the 64K computers) a unused area of ram. This area should not be used since all computers of this series do not have that area of ram.

3. The location D1FFH in the CPU memory map is reserved for passing control information between the CPU and the PBPs. The CPU selects one of the PBP devices by writing a "1" into the desired bit in location D1FFH. The device can be deselected by writing a "0" into the desired bit.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Therefore the CPU can then access 8 devices, one at a time.

3. continued.....

If the IRQ' line is pulled "low" the cpu can read the status for location D1FFH and locate the requesting PBP. A "1" in a bit Ix (where x=0 to 7) corresponds to a interrupt in PBP x. If the bit is a "0" then the device has not caused the interrupt. The PBP must clear the interrupt flag when the interrupt is being serviced.

7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0

4. The PBP should assert MPD' only when they are selected. The PBP should assert EXTSEL' only when they are selected and if EXTENB is asserted.

5. The PBP may respond to any of the selects any one of the selects D0 through D7. It is recommened that the PBPs have configuration switches to allow them to respond to any one of the selects. Some of the systems use the PBI to support internal devices therefore the user should check their manual for device locations. If the system has devices in specific location those are reserved in that computer.

6. A peripheral handler may respond to address in the region D800H-DFFFH only when it is selected. The location D800H contains the device I.D. of the PBP.

7. A peripheral may respond to address in the region D100H to D1FEH only when selected.

8. The PBP will have priority over the SIO peripheral when they are address generically.

9. The data between the CPU and the PBP is passed under the control of the peripheral handler for the PBPs.

10. The PBPs will work if a cartridge is present in the cartridge slot.

11. The CPU address space from D600H to D7FFH is reserved for PBI devices as follows:

Device	Range	Size
D0	D600H-D61FH	32 Bytes
D1	D620H-D63FH	32 Bytes
D2	D640H-D65FH	32 Bytes
D3	D660H-D67FH	32 Bytes
D4	D680H-D69FH	32 Bytes
D5	D6A0H-D6BFH	32 Bytes
D6	D6C0H-D6DFH	32 Bytes
D7	D6E0H-D6FFH	32 Bytes

The region from D700H to D7FF is reserved for use by ATARI. The CPU address space from D600H to D7FFH is always mapped to the PBI and does not require the EXTENB|EXTSEL' protocol. Some units may have devices mapped on the PBI, these devices are only active when selected but care must be taken when using using a unit with onboard devices.

C. External Application Cartridges

The "External Application Cartridge" (EAC) is a generalization of the PBP. They have the following characteristics:

1. An EAC can reside at any or all of the locations in the region 0000H to BFFFH for which the EXTENB is generated. They may respond to these address only when "opened".

2. The EACs must be opened by the protocol given for the PBPs.

3. The EACs must conform to the EXTENB|EXTSEL' protocol.

4. The EACs must have a handler (resident at location D800H-DFFFH) that controls their operation. The EACs must conform to the conditions (4) through (11) of section III. B. above.

5. The EACs will work if a cartridge is present in the internal cartridge slot.

IV. Interface Requirements

For peripherals to interface through the PBI to the computer the following requirements must be followed.

A. D.C. Characteristics

All PBI outputs from the CPU have the capability of driving ONE LSTTL load.

All PBI open collector input lines must be able to sink 5 mA (min) at .4 V(max).

All PBI non-open collector input lines execpt AUDIO must have the drive capability of one LSTTL gate.

All PBI signals except AUDIO will be at standard TTL logic levels.

The AUDIO input line must drive a 1K Ohm input impedance with a 1V peak to peak signal.

B. A.C. Characteristics

Given in Figure 3 are the worst case timing requirements for the PBI.

Symbol	Min	Max	Units	Description
T_{CYC}			nS	Clk period
T_{O2H}	219	297	nS	Phase 2 duty cycle
T_{ADS}		145	nS	Address setup
T_{ADH}	10		nS	Address hold
T_{XNS}		215	ns	EXTENB setup
T_{XNH}	15		nS	EXTENB hold
T_{XSS}		253	nS	EXTSEL' setup
T_{XSH}	100		nS	EXTSEL' hold
T_{DIS}	62		nS	Data in setup
T_{DIH}	10		nS	Data in hold
T_{DOS}		112	nS	Data out setup
T_{DOH}	10		nS	Data out hold
T_{RWS}		228	nS	R/W' setup
T_{RWH}	10		nS	R/W' hold
T_{RFS}		150	nS	Refresh setup
T_{RFH}	15		nS	Refresh hold
T_{RDS}	200		nS	Ready setup
T_{RSS}	187	305	nS	RAS' setup
T_{RSH}	10		nS	RAS' hold
$T_{CSS\ re}$	295	385	nS	CAS' setup on read cycle
$T_{CSS\ wr}$	409	522	nS	CAS' setup on write cycle
T_{CSH}	10		nS	CAS' hold read or write