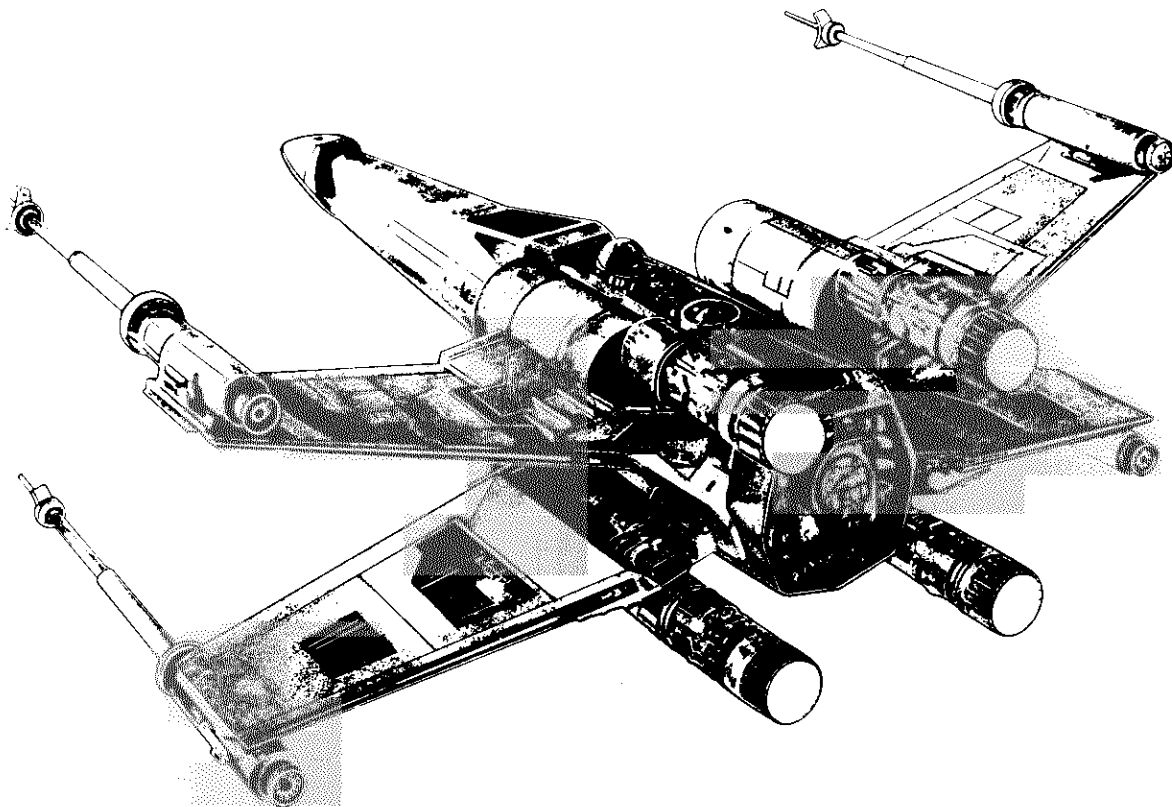


NOTE

This staple temporarily holds the schematic package together. Remove the staple before using these schematics.



Schematic Package Supplement to

STAR WARS*

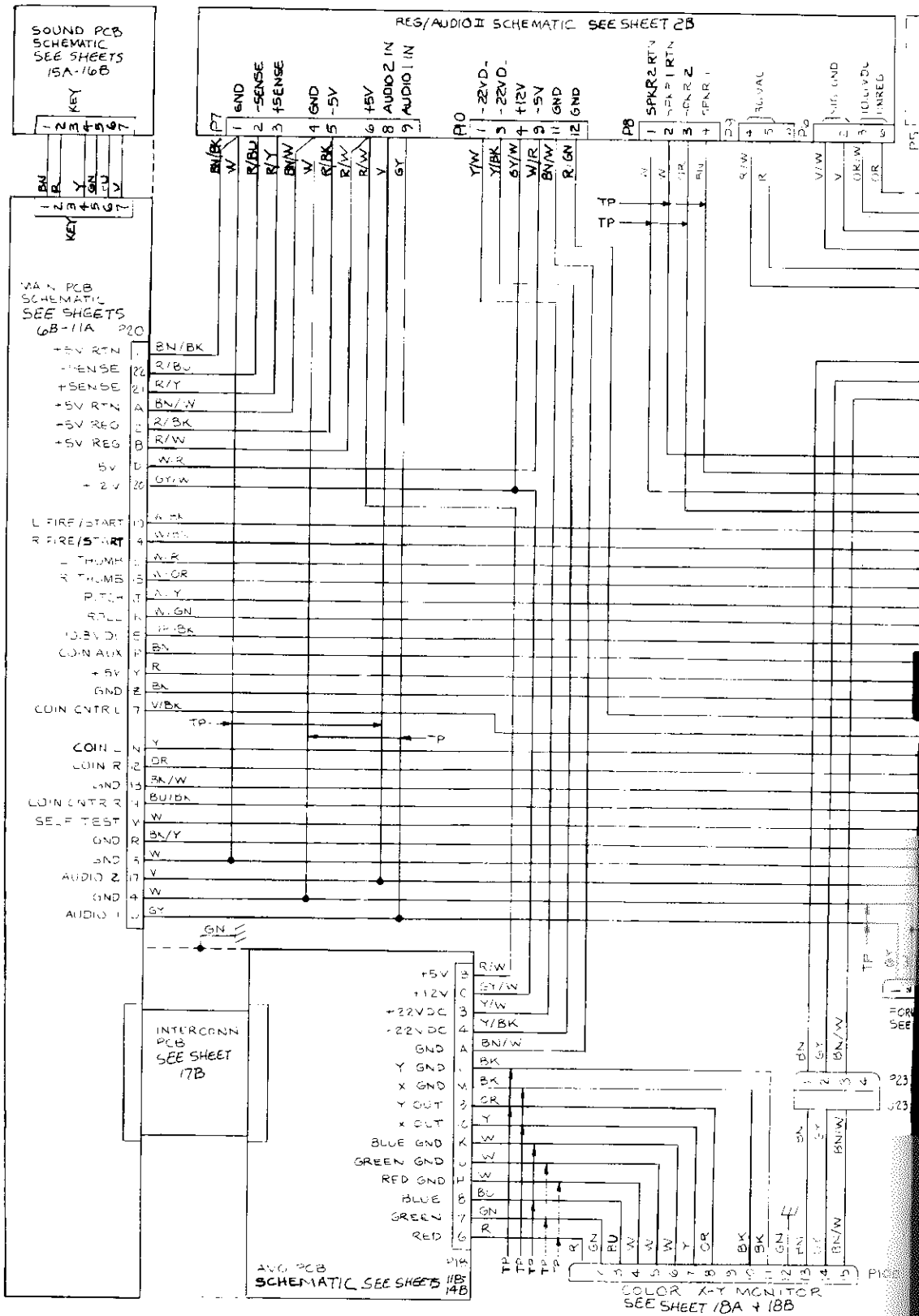
Operators Manual

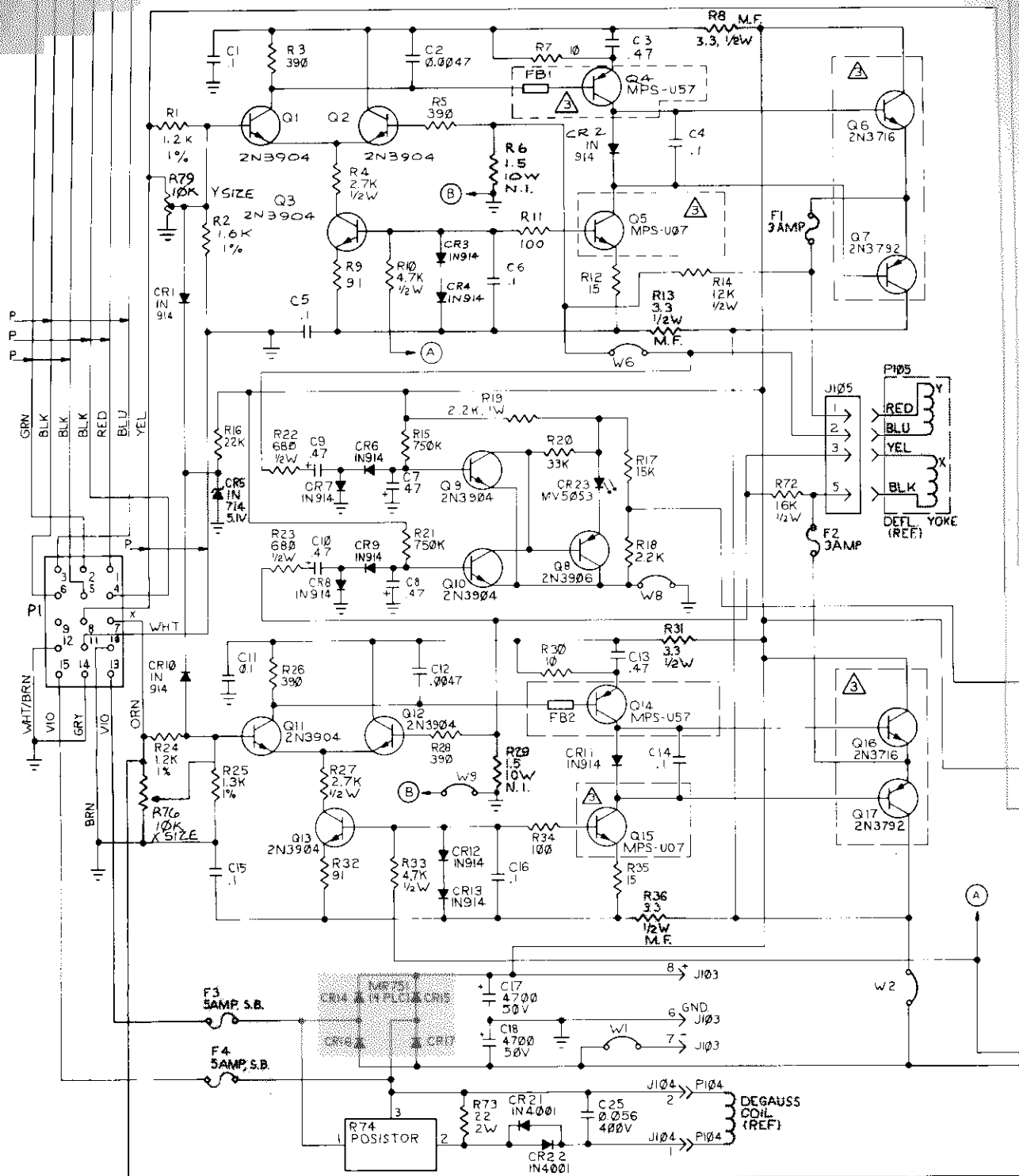
*Trademarks of Lucasfilm, Ltd. used by Atari, Inc. under license.

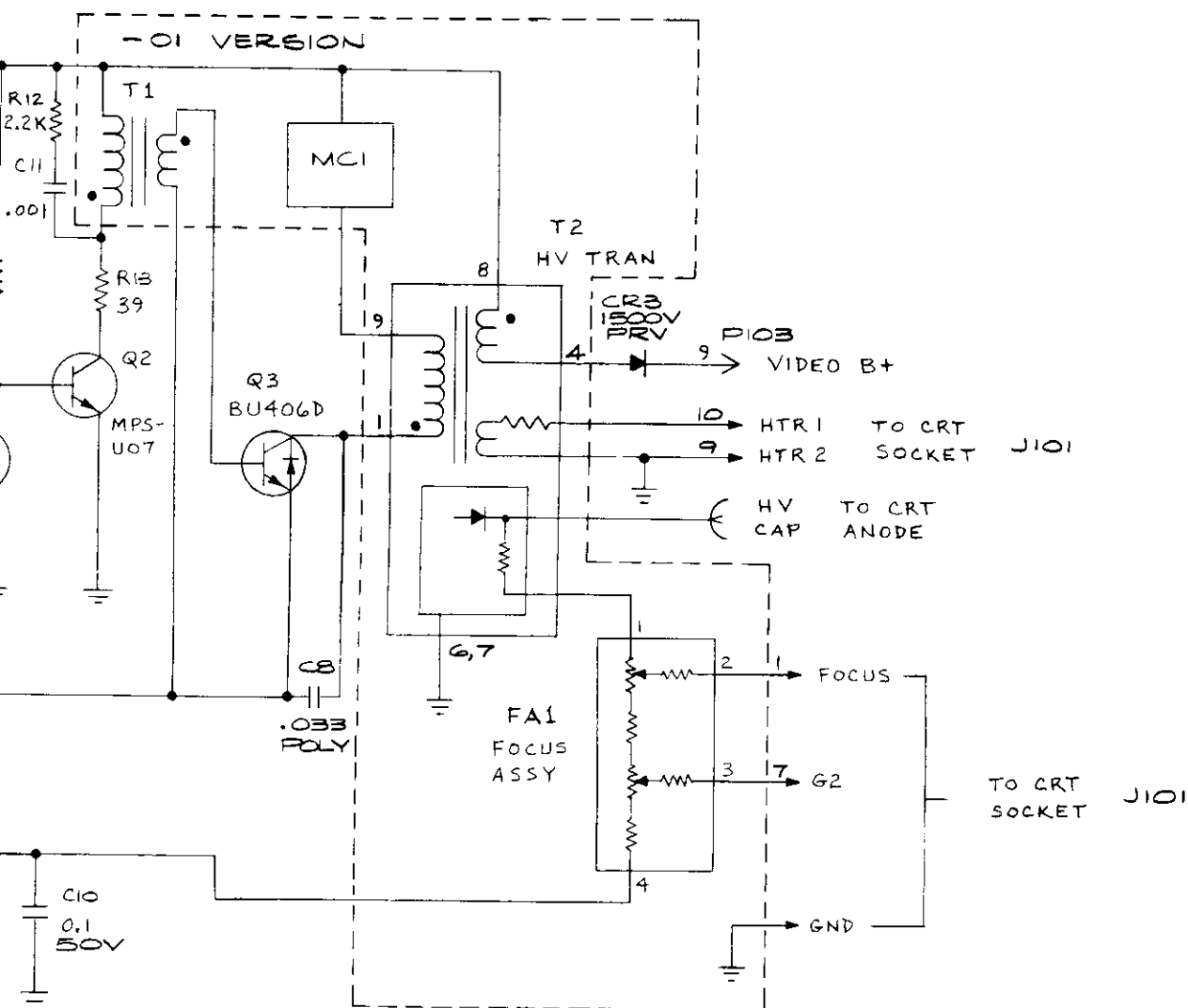
6M



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NOTE: UNLESS OTHERWISE SPECIFIED -

1. ALL RESISTOR VALUES IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE μf .

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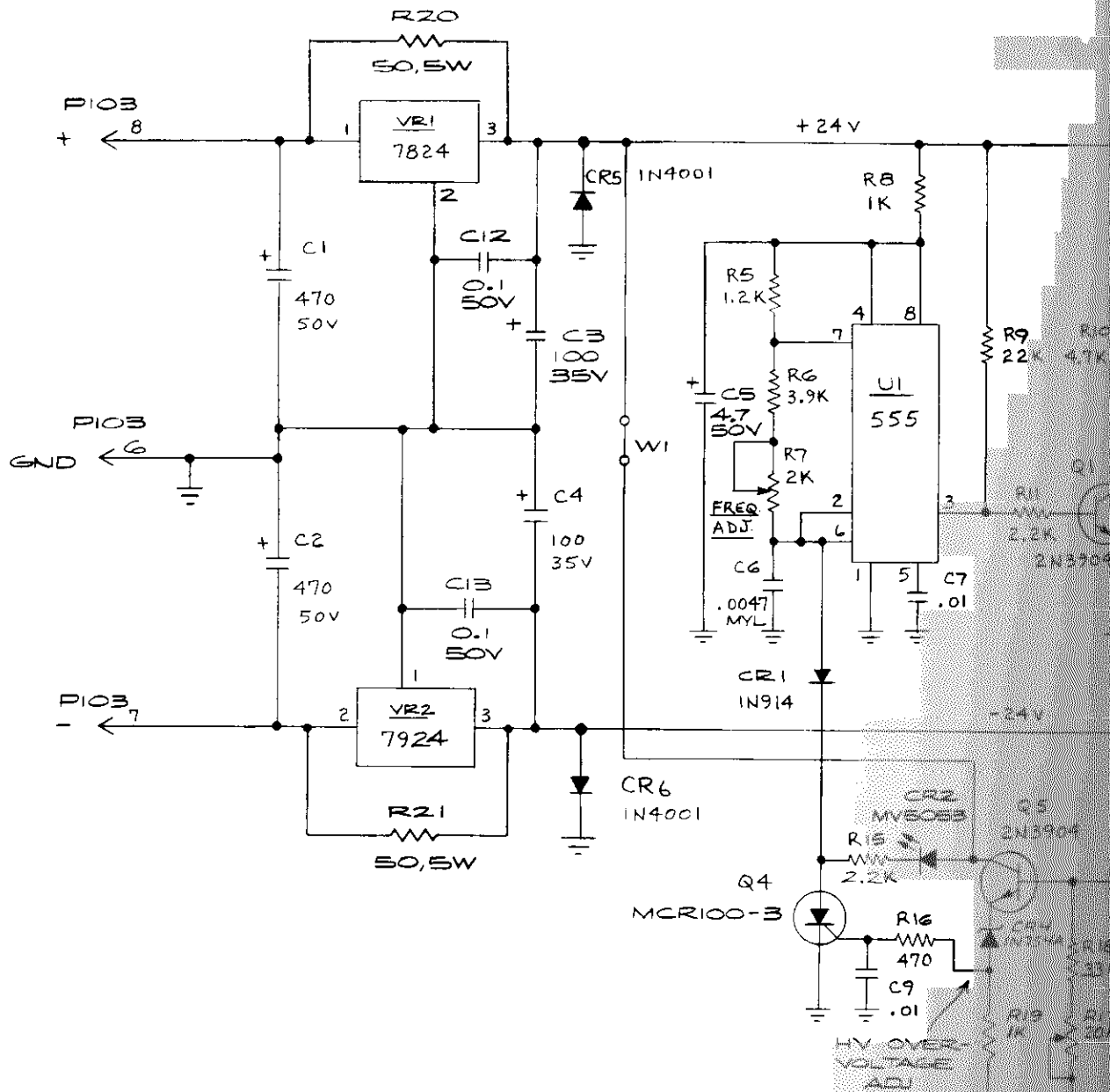
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STAR WARS Color X-Y High-Voltage PCB

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SP-225 Sheet 18A
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P3

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STAR WARS Interconnect PCB

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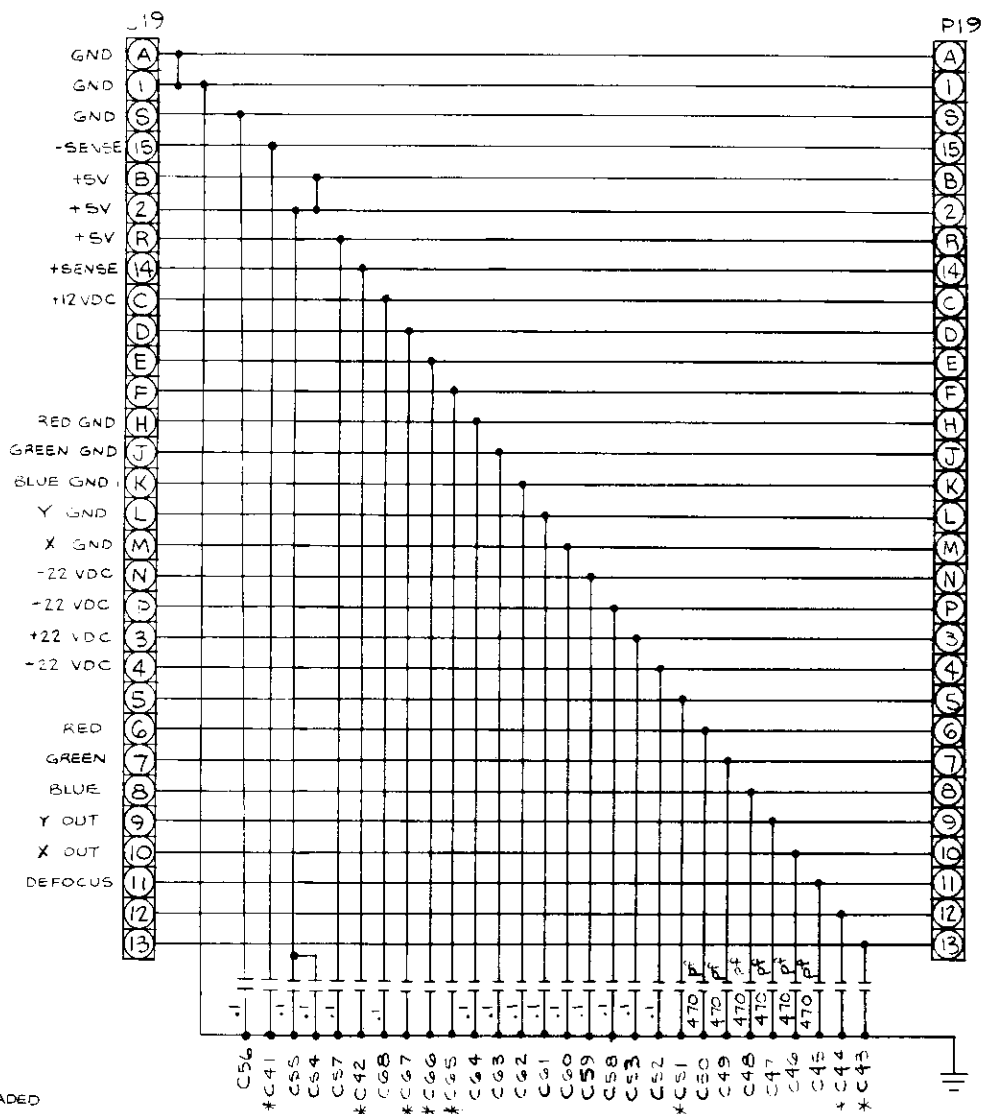
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SP-225 Sheet 17B
1st printing

P1		P2
1		1
2		2
3		3
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J20

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18
C
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P
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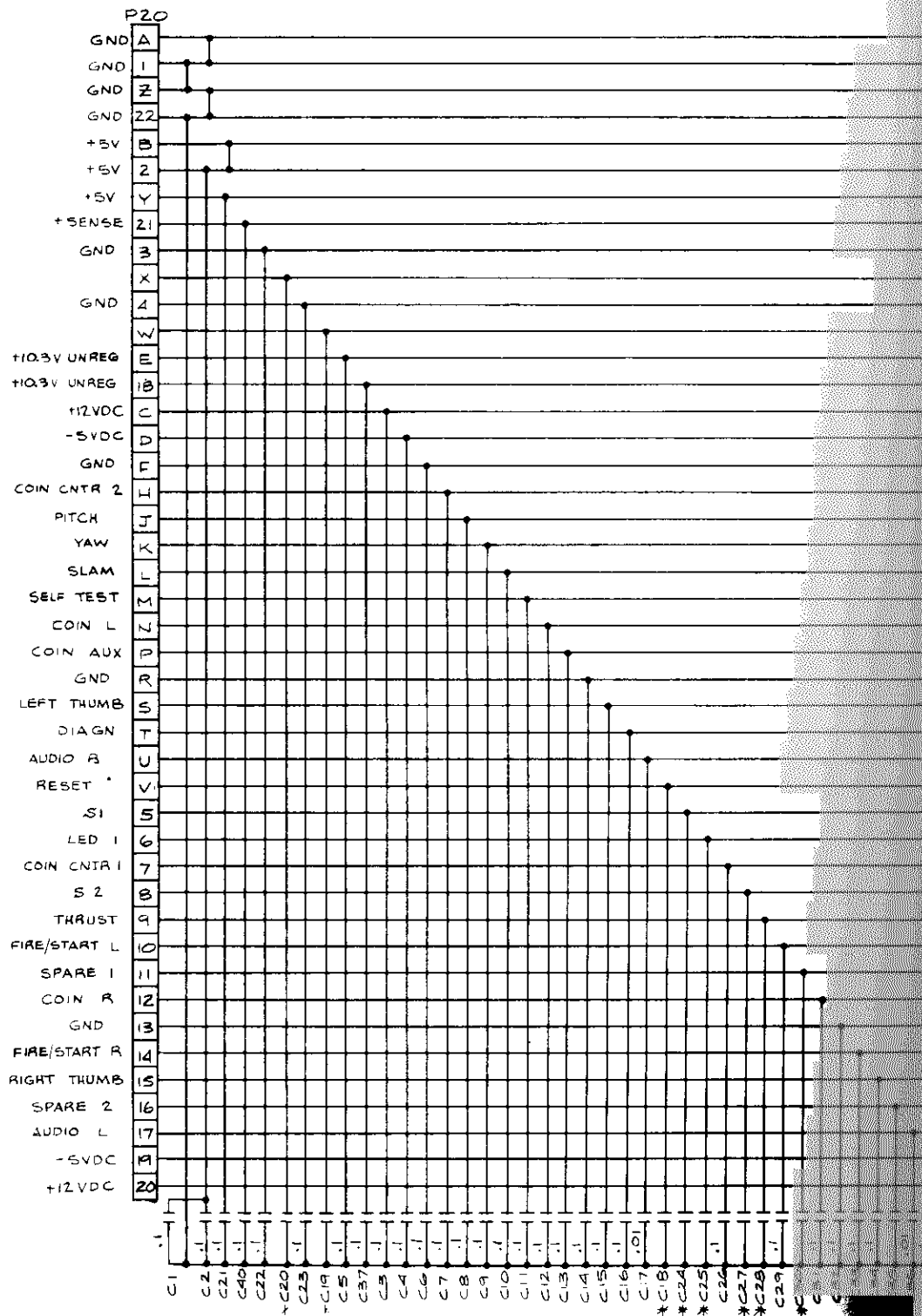
STAR WARS EMI Shield PCB



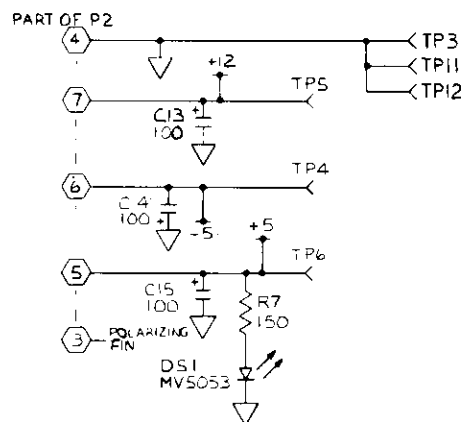
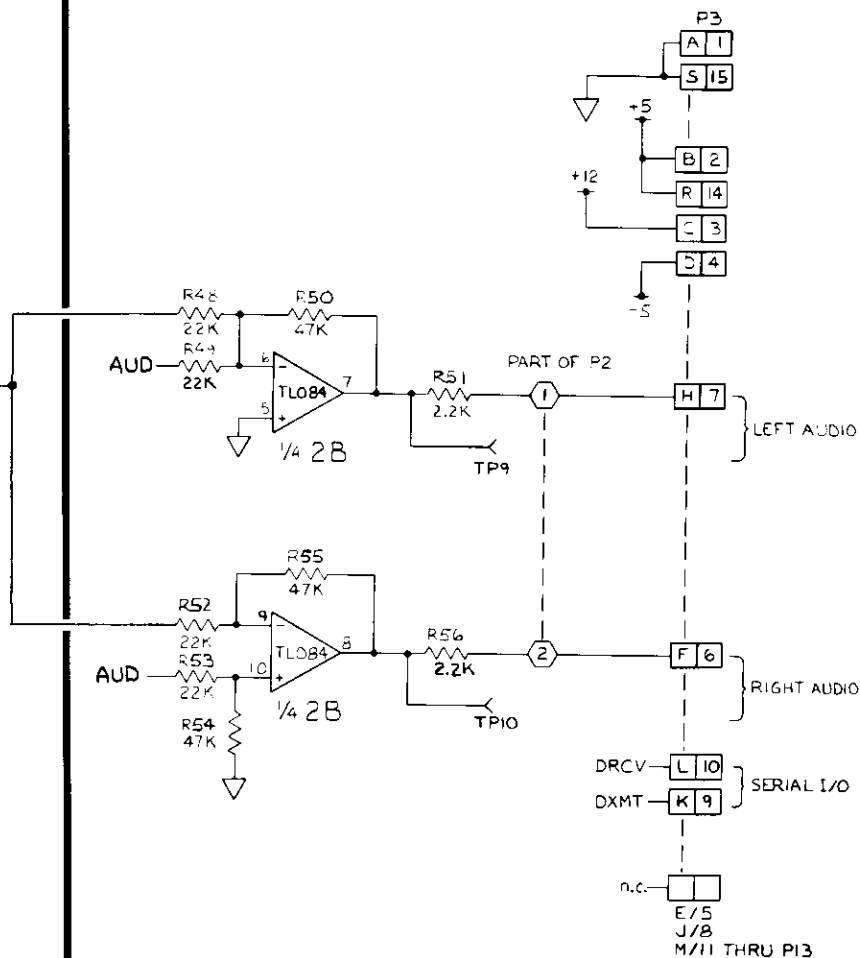
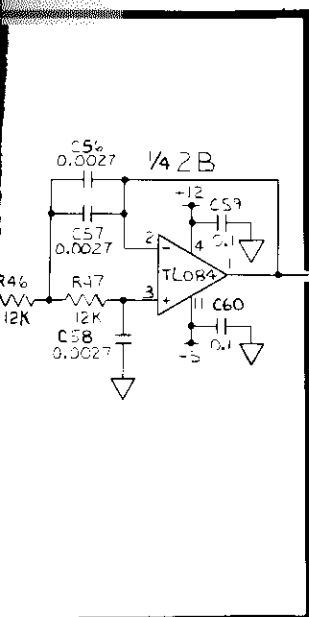
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Output and Summing Amplifiers



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STAR WARS Sound PCB

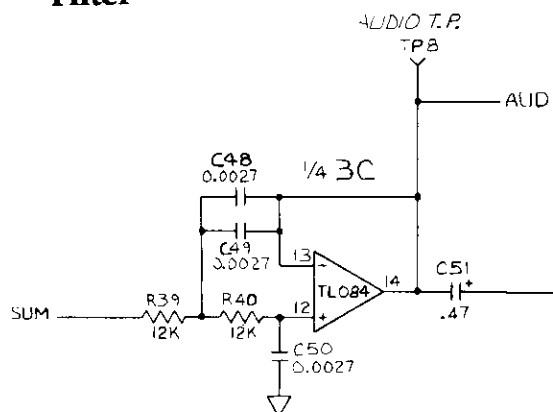


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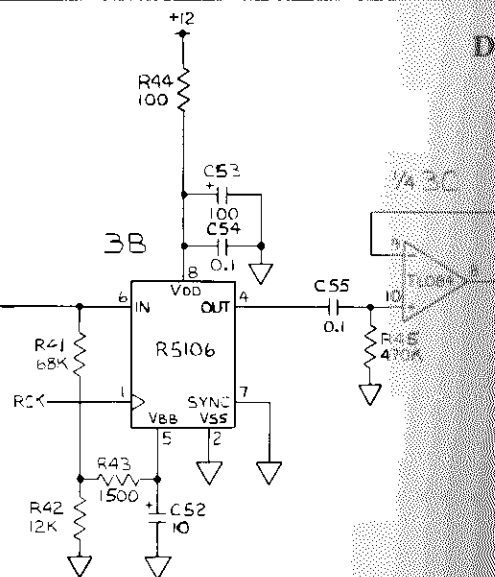
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1st printing

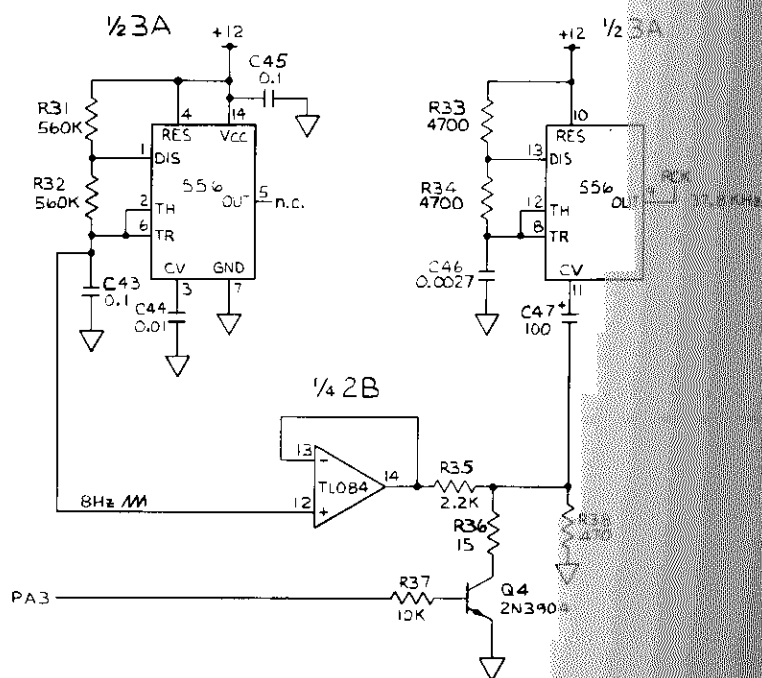
Filter

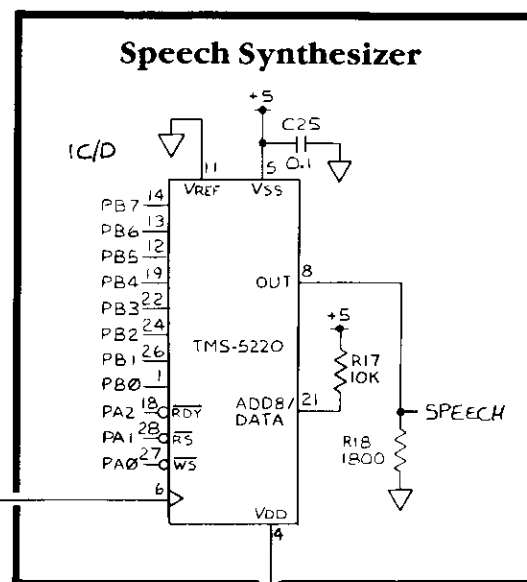
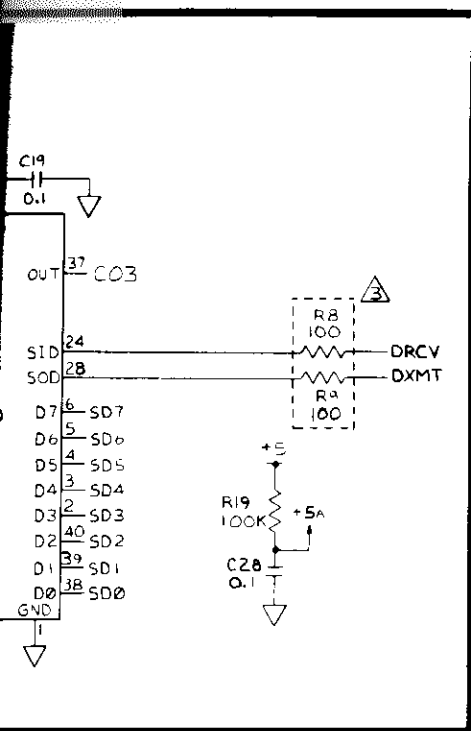


Delay

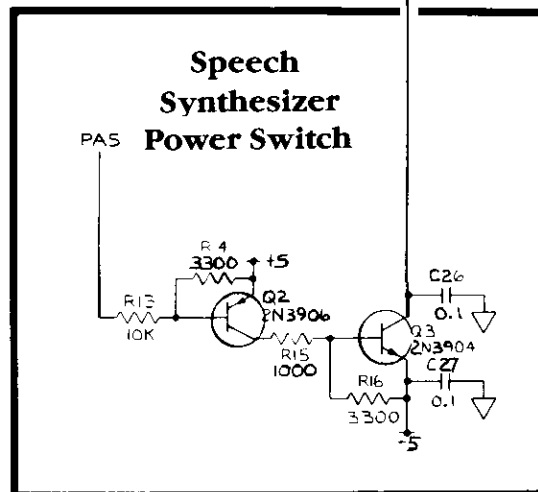
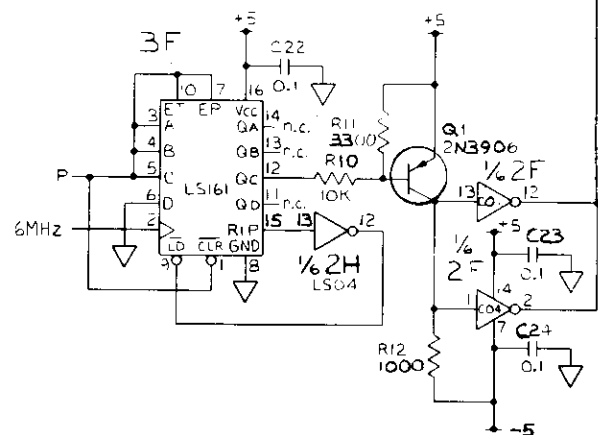


Delay Clock





Speech Synthesizer Clock Generator



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STAR WARS Sound PCB

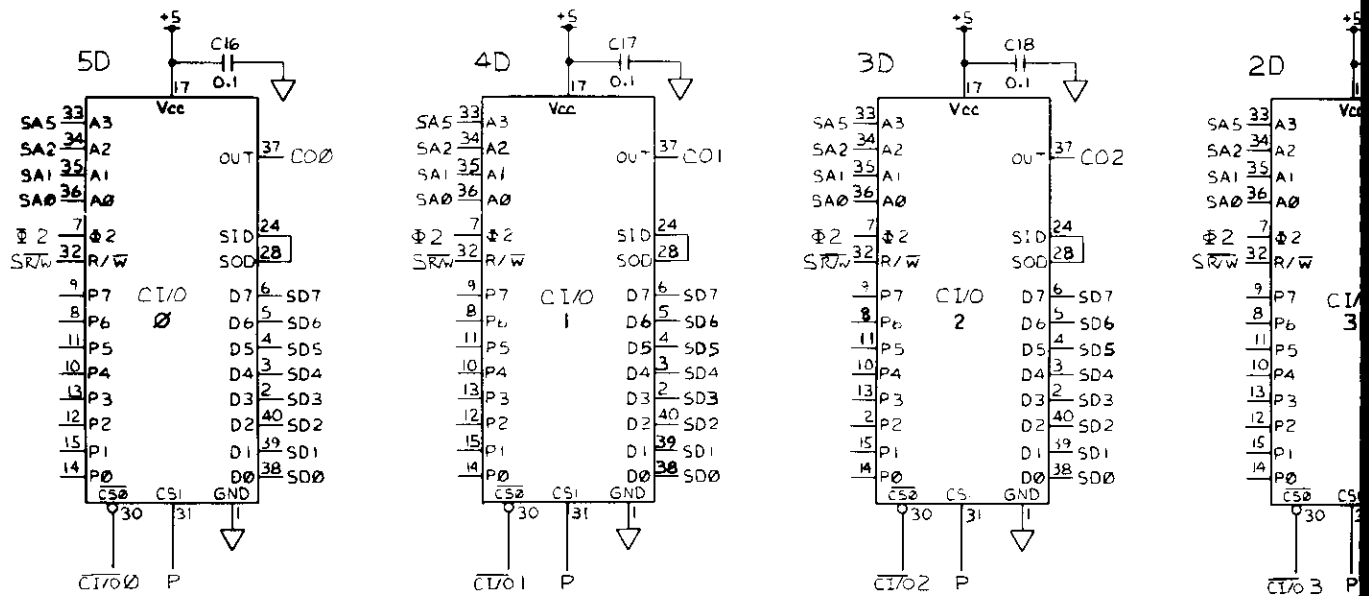


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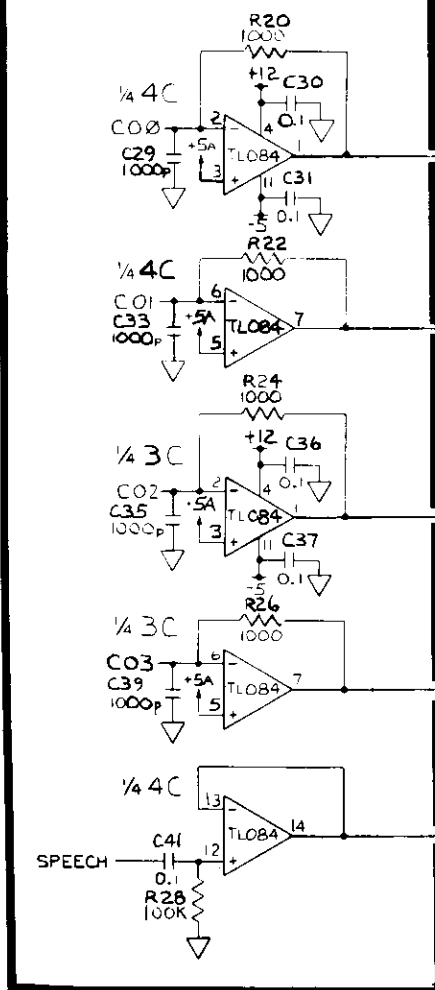
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1st printing

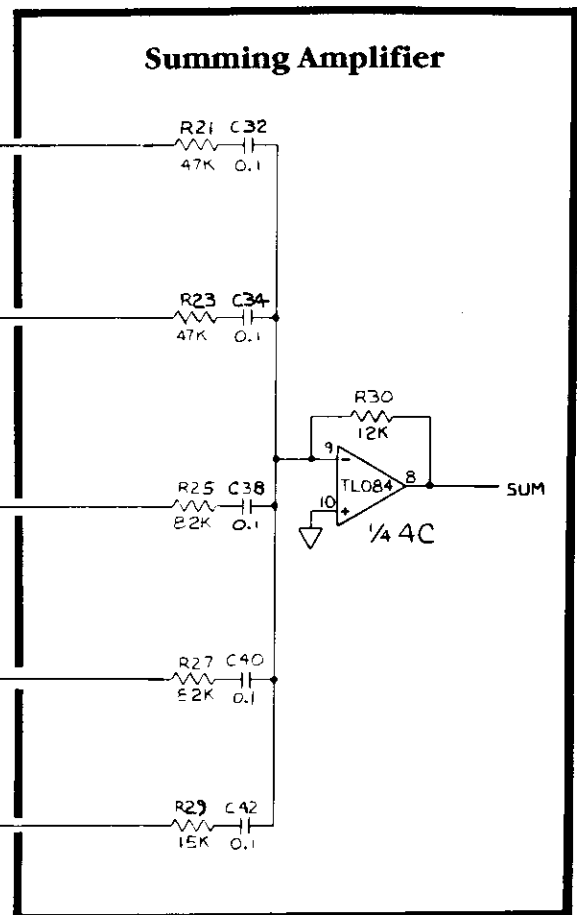
Music and Sound Effects Generators



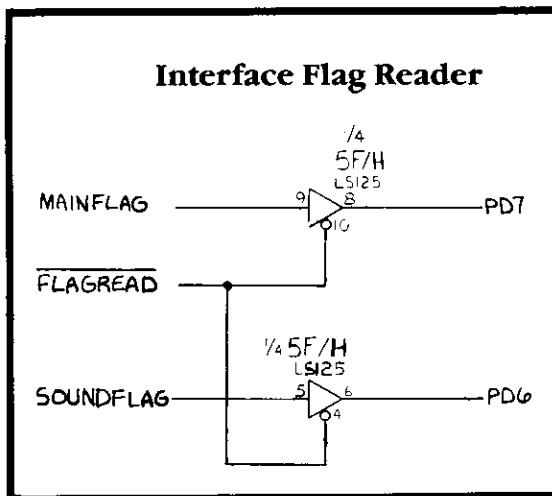
Buffers



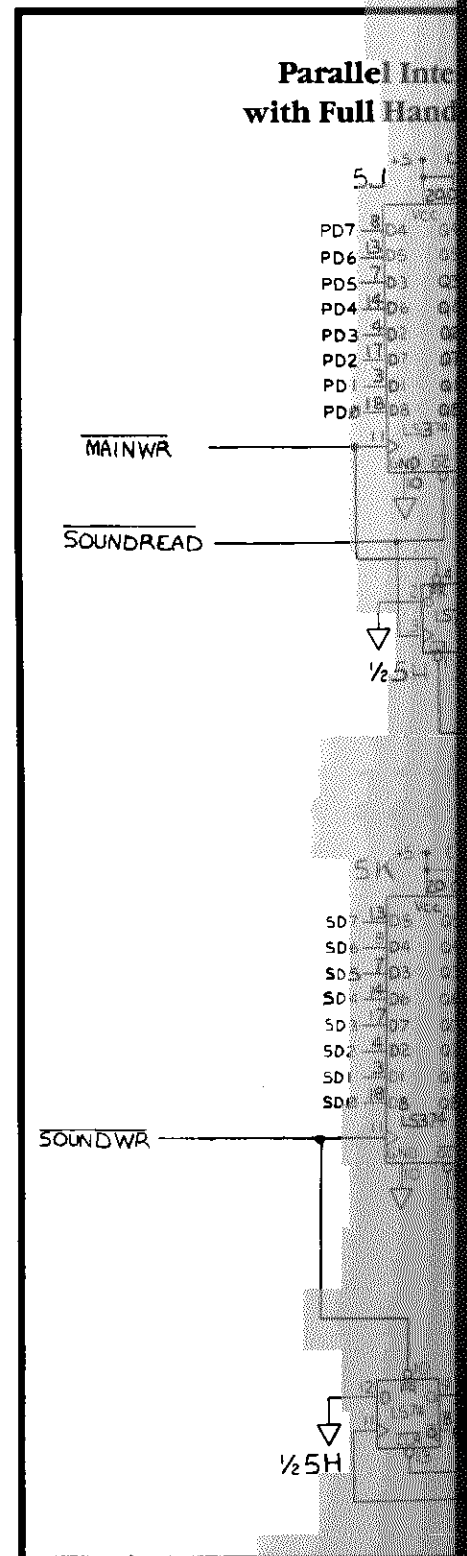
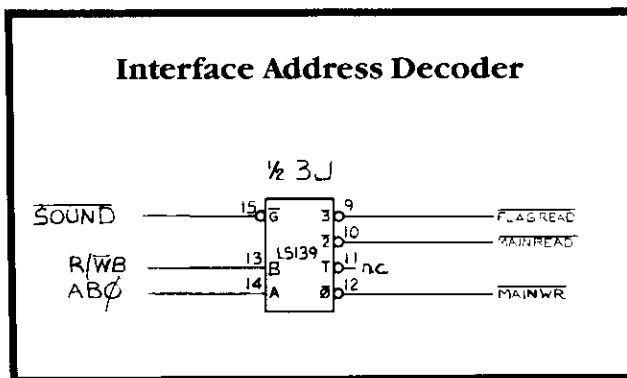
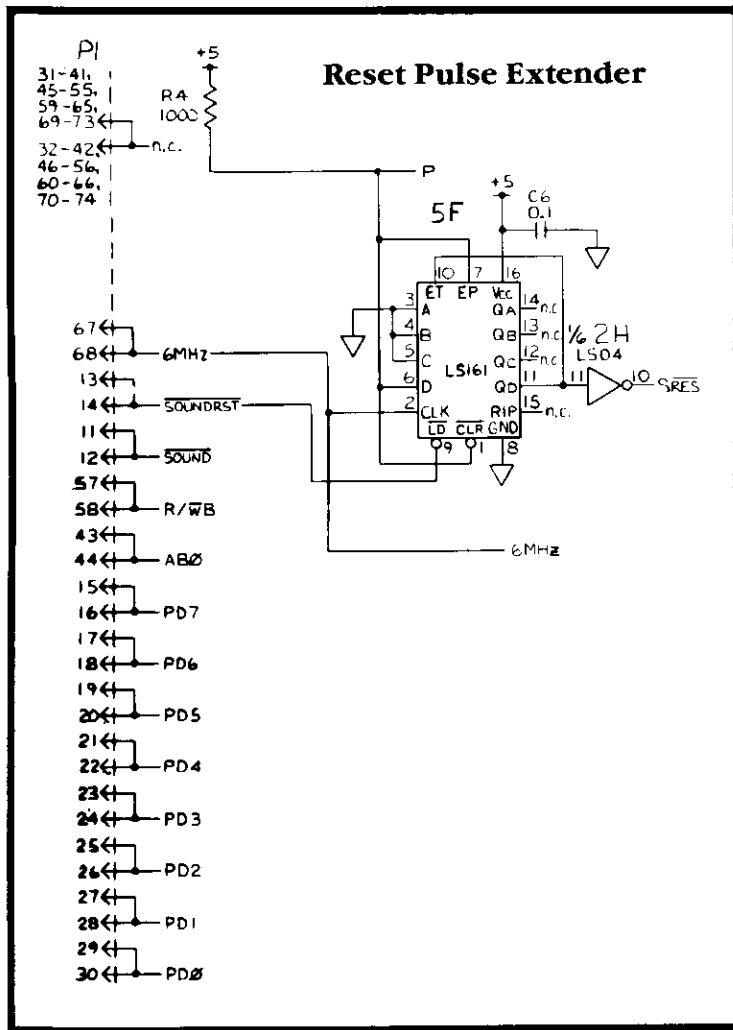
Summing Amplifier



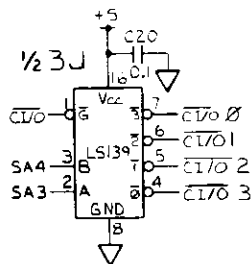
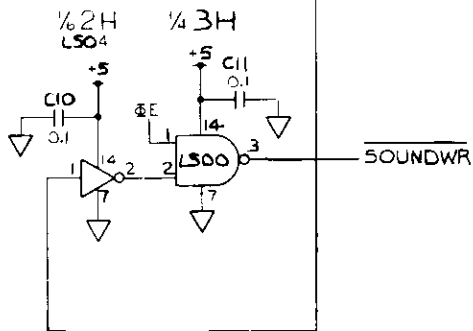
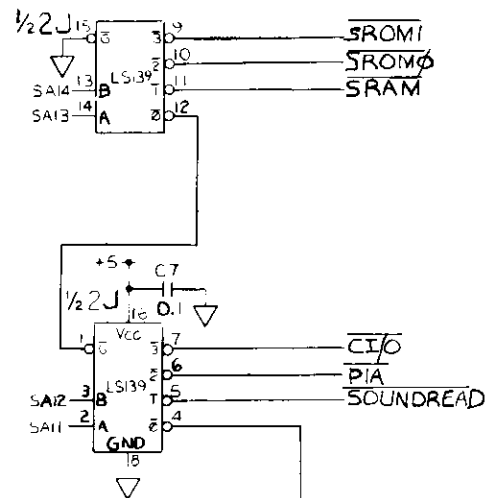
The diagram shows two digital signals over time. The top signal, labeled 'SOUNDFLAG', is a square wave that transitions from low to high at a specific point. The bottom signal, labeled 'SRES', is a square wave that transitions from low to high at a later point. The signal 'MAINREAD' is shown as a low-level line with a single dot indicating a specific event or state change.



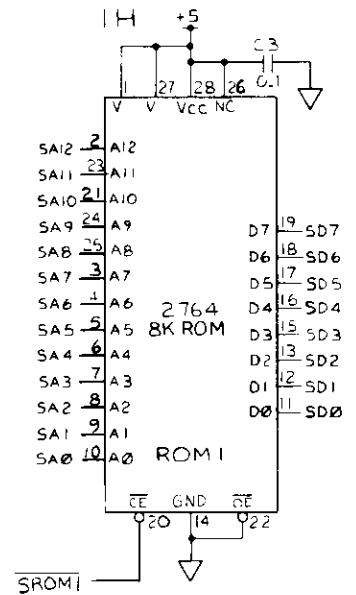
SP-225 Sheet 15A
1st printing



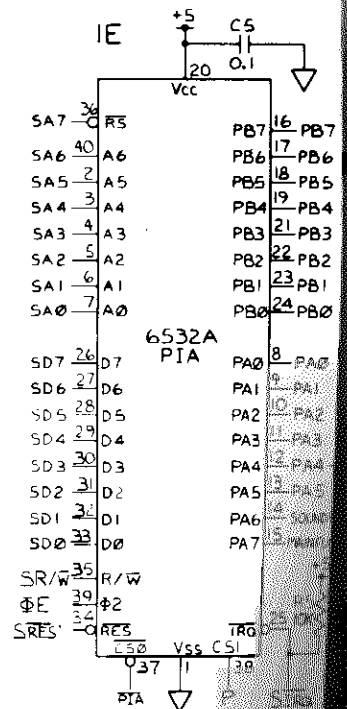
Address Decoders



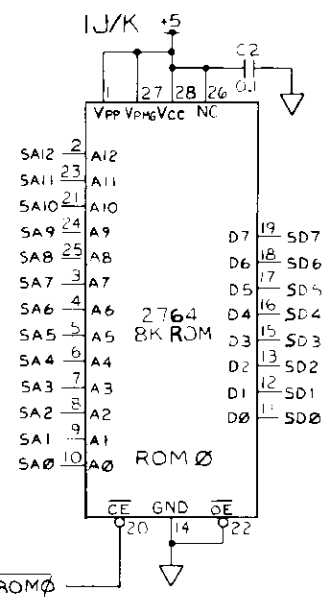
Sound



Peripheral Inter



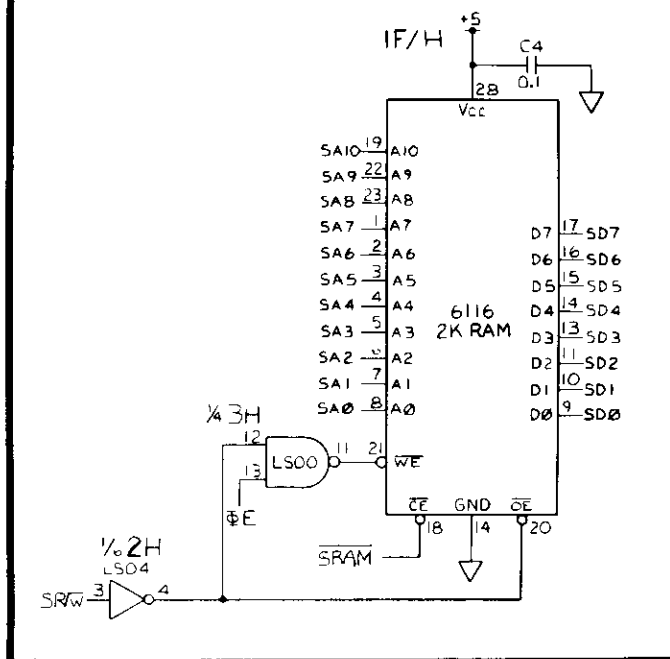
ROM



Interface Adapter



Sound RAM



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STAR WARS Sound PCB



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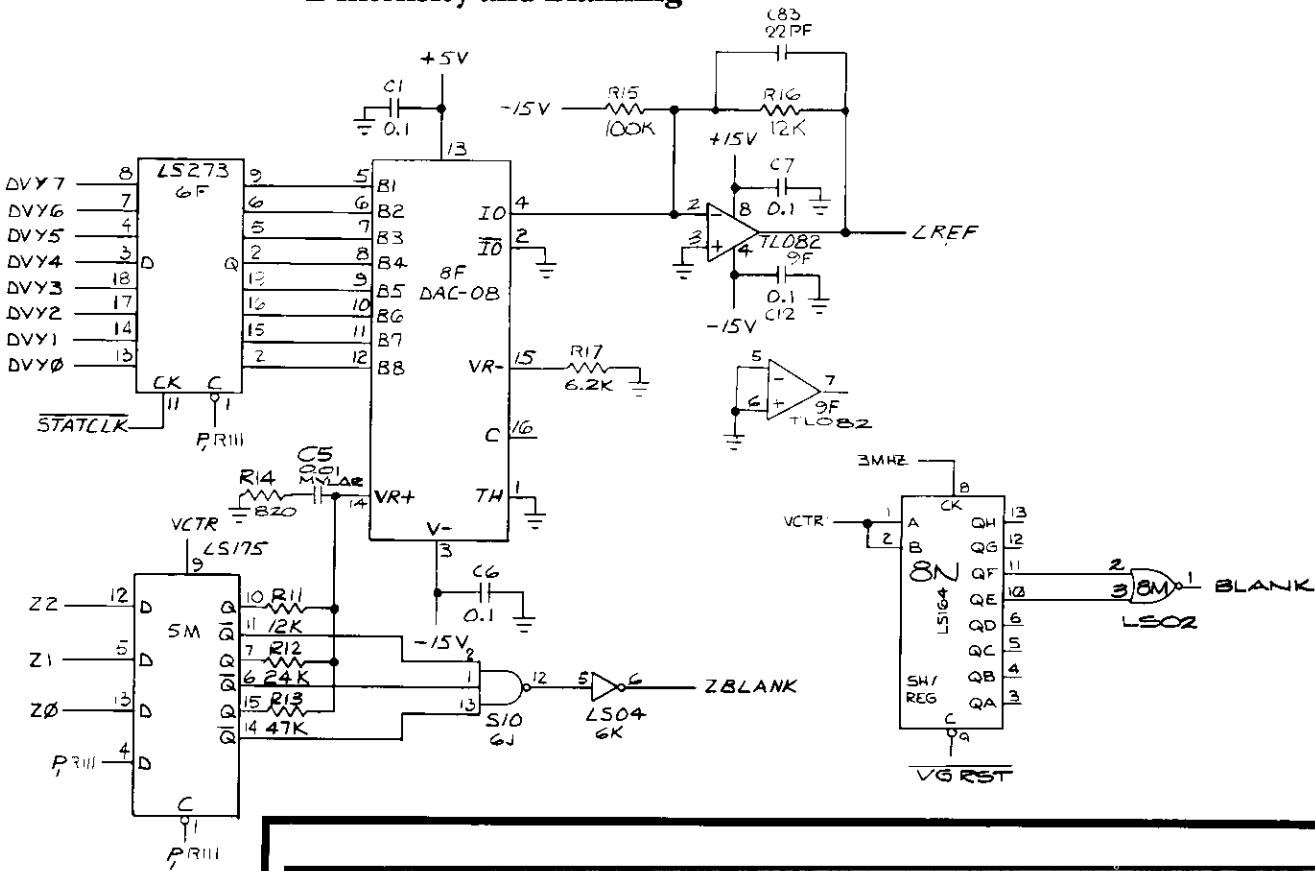
SP-225 Sheet 15B
1st printing

Bipolar Offset Adjustments

Perform the following procedure to adjust the bipolar offset current:

1. Set the game to the Self-Test Mode and select the Bipolar Offset Test Display as described in Chapter 2 of the game manual.
2. Adjust XBIP (R92) and YBIP (R88) so that the displayed-box line width is $\frac{1}{8}$ -inch or less.

Z-Intensity and Blanking



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STAR WARS Analog Vector-Generator PCB

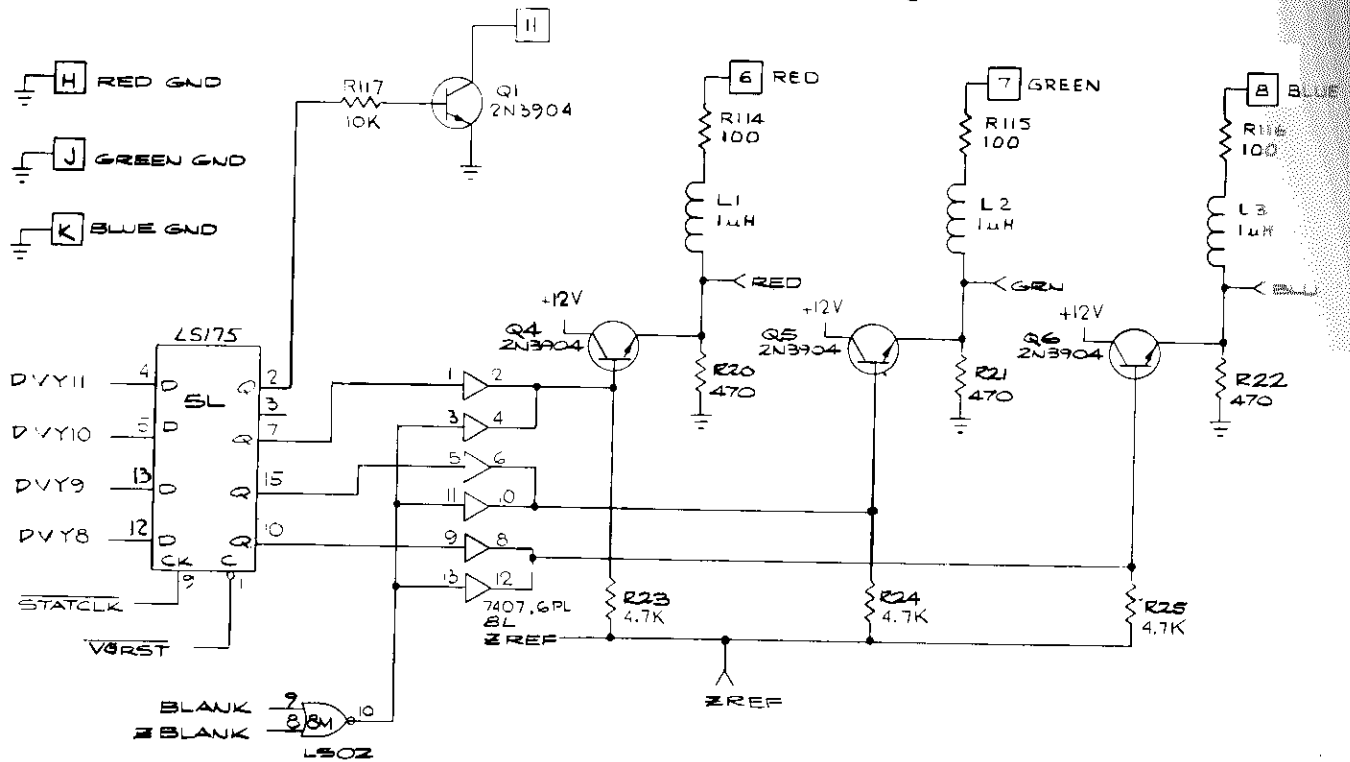


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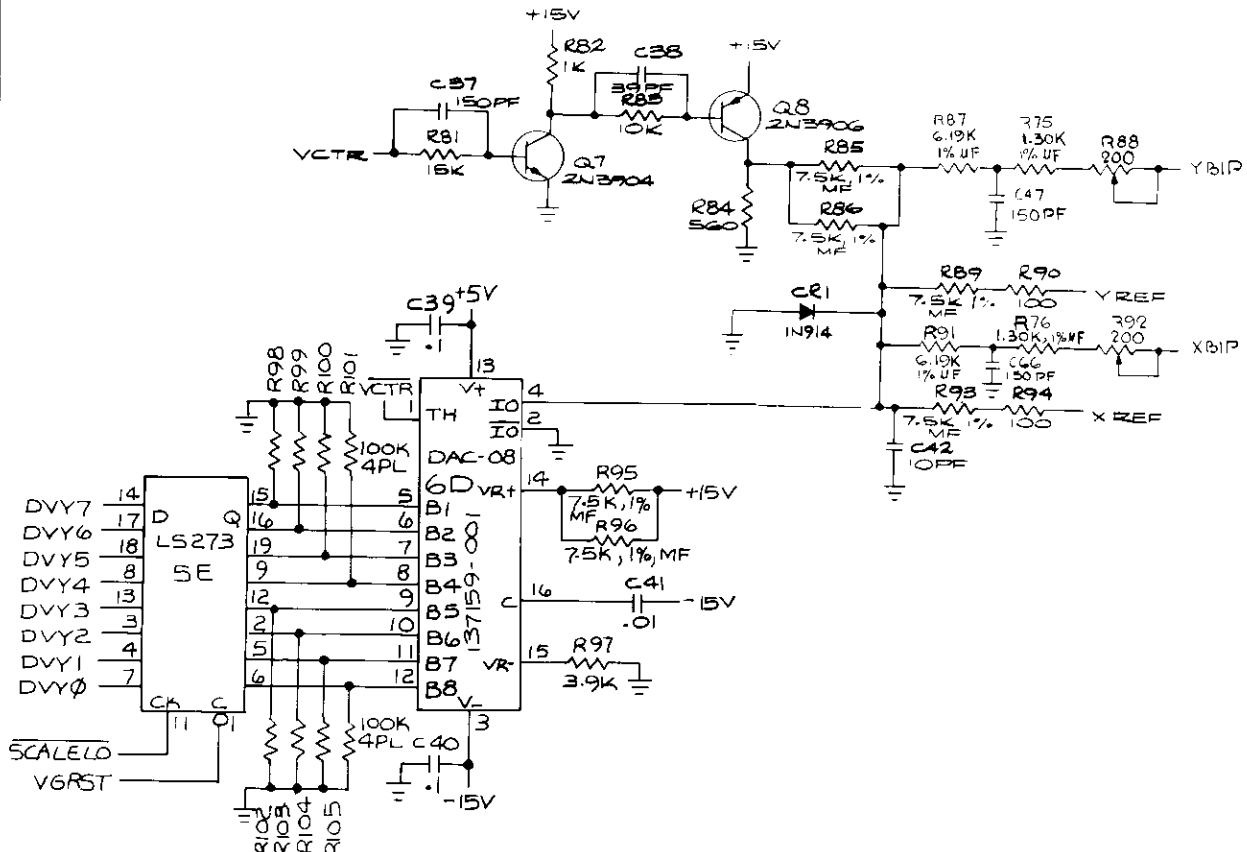
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SP-225 Sheet 14B
1st printing

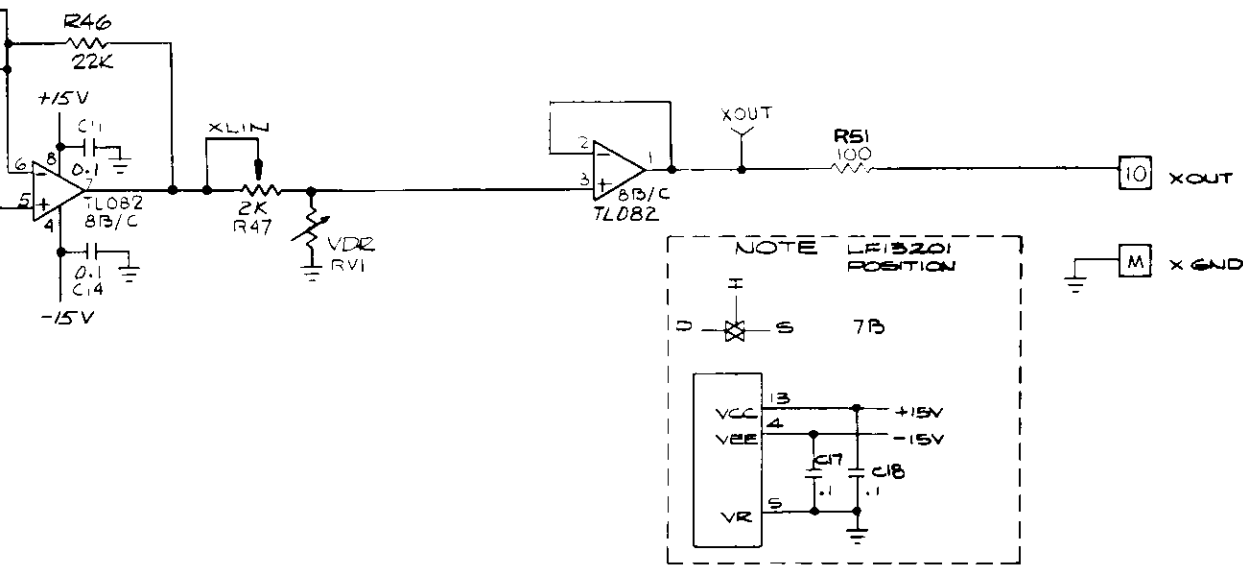
R-G-B Output



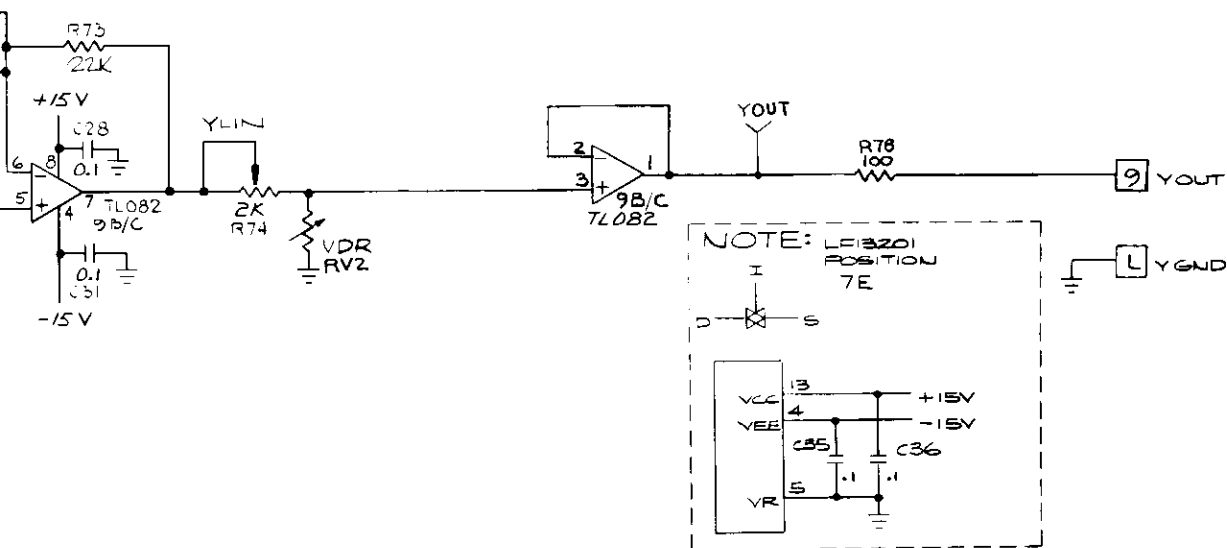
DAC Reference and Bipolar Current Sources



X-Axis Output



Y-Axis Output



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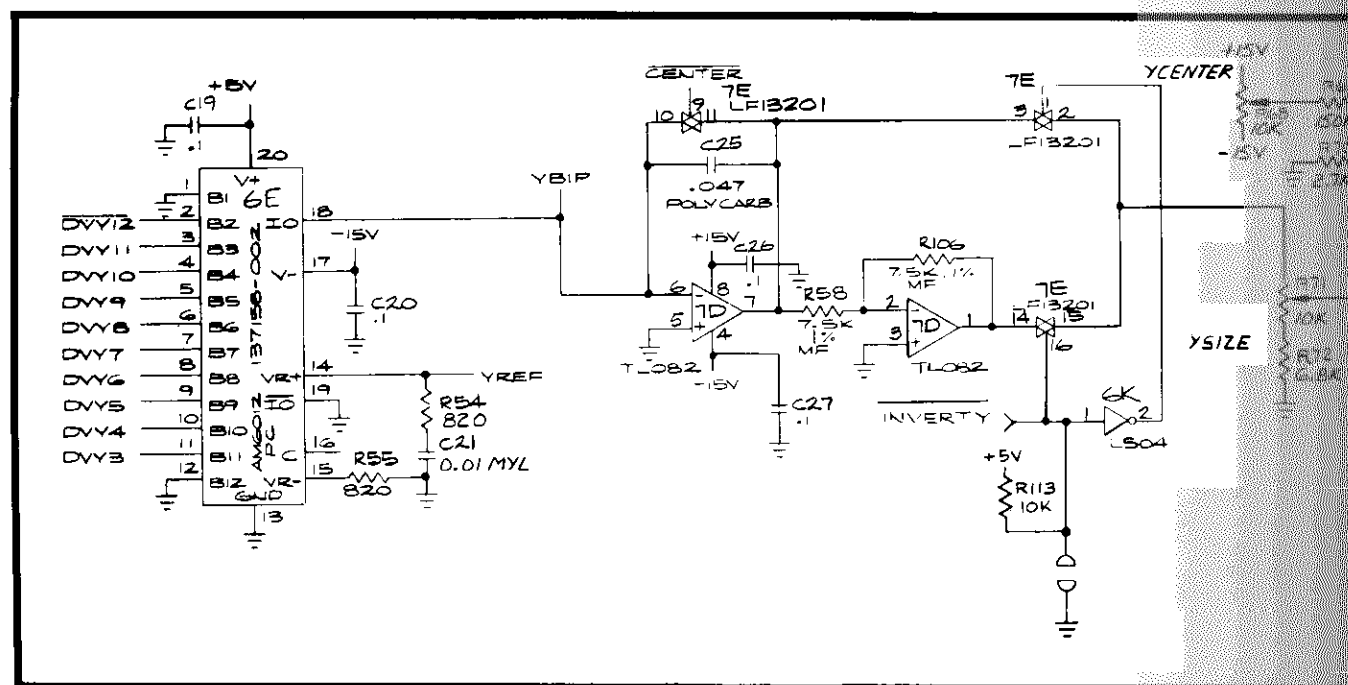
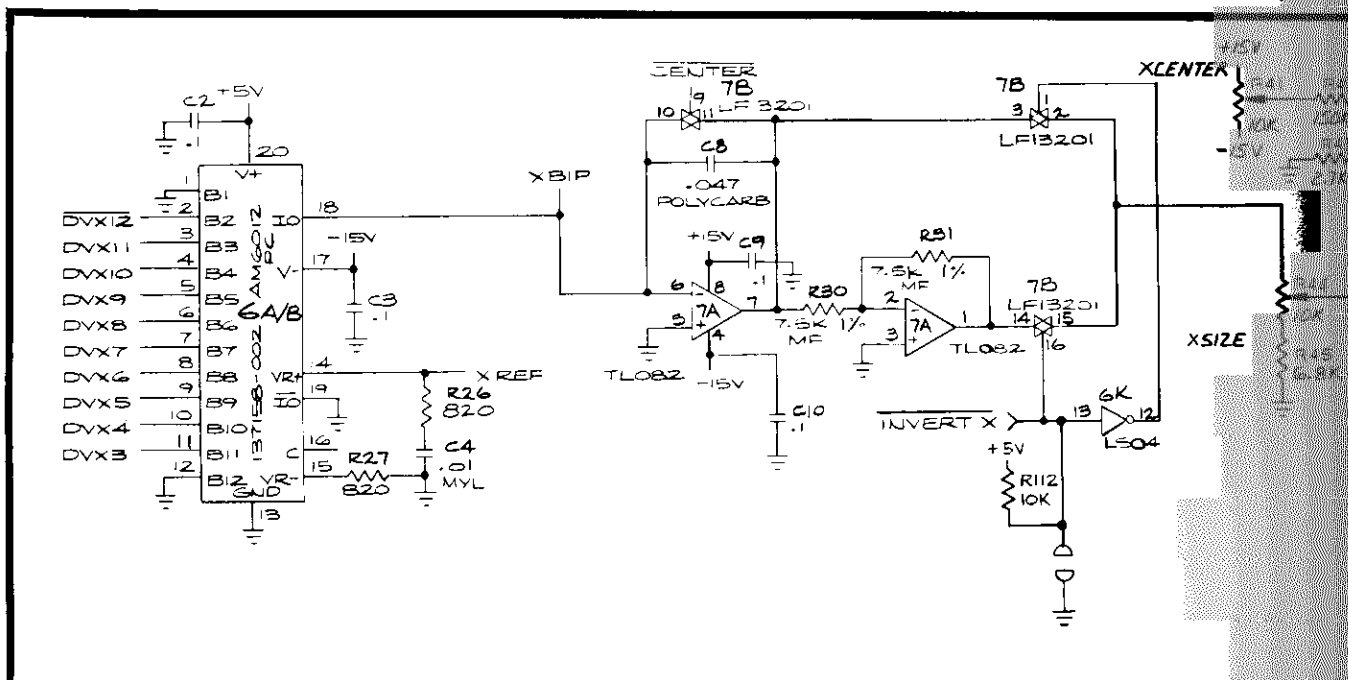
STAR WARS Analog Vector-Generator PCB



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SP-225 Sheet 14A
1st printing



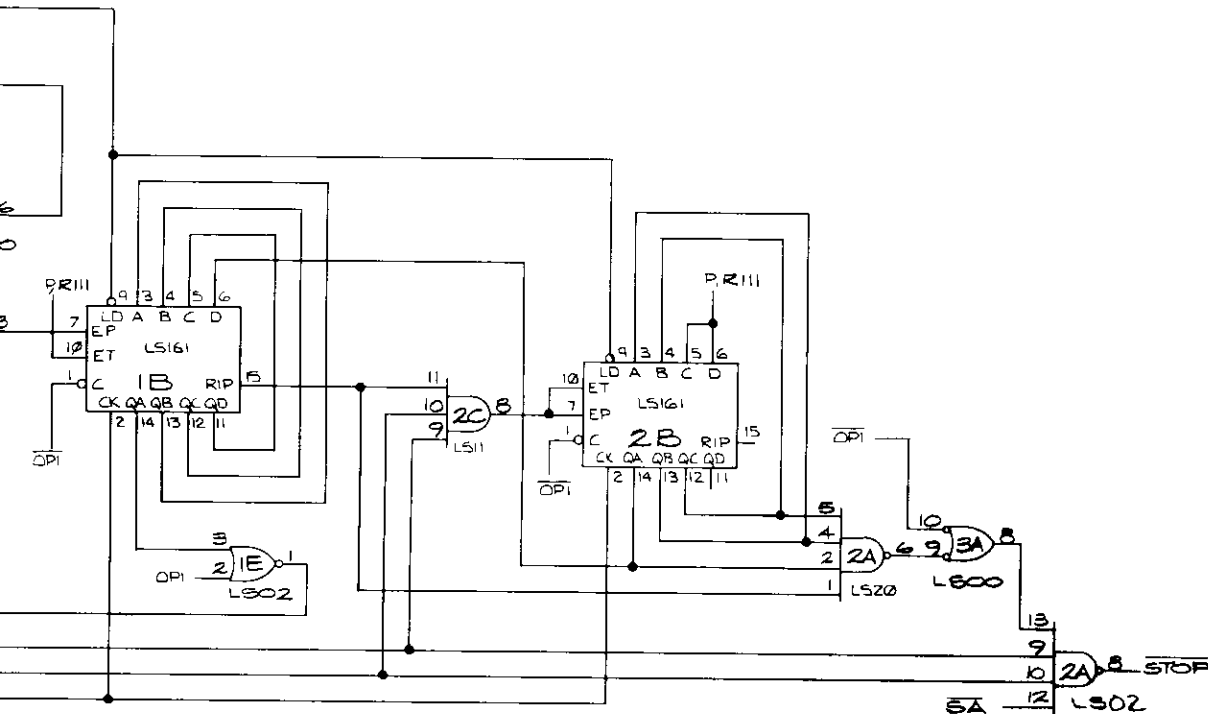
X and Y Video Adjustments

Perform the following procedure to adjust the display size, centering, and linearity:

1. Set the game to the SelfTest Mode and select the Cross-hatch Pattern Display as described in Chapter 2 of the game manual.
2. Adjust XCENTER (R41) and YCENTER (R68) so that the crosshatch pattern is centered on the screen.

3. Adjust XSIZE (R44) and YSIZE (R71) so that the crosshatch pattern covers the entire visible area of the screen.
4. Adjust XLIN (R47) and YLIN (R74) so that the crosshatch lines are straight and the diamond shape is symmetrical. Since the linearity adjustment changes the size of the display, it may be necessary to repeat step 3 to obtain the correct display size.

Vector Timer



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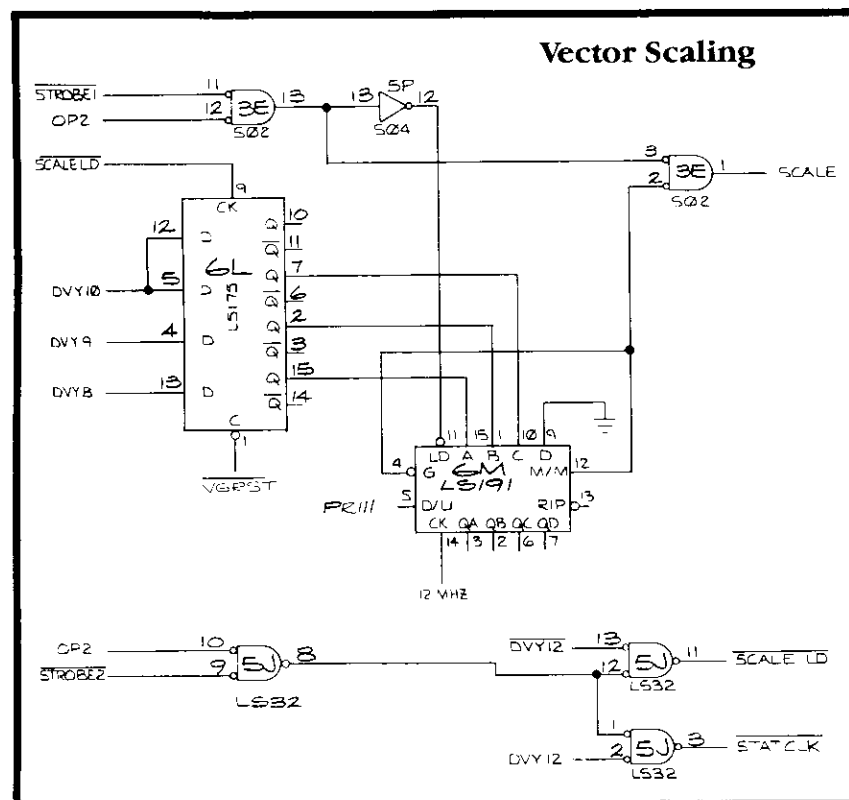
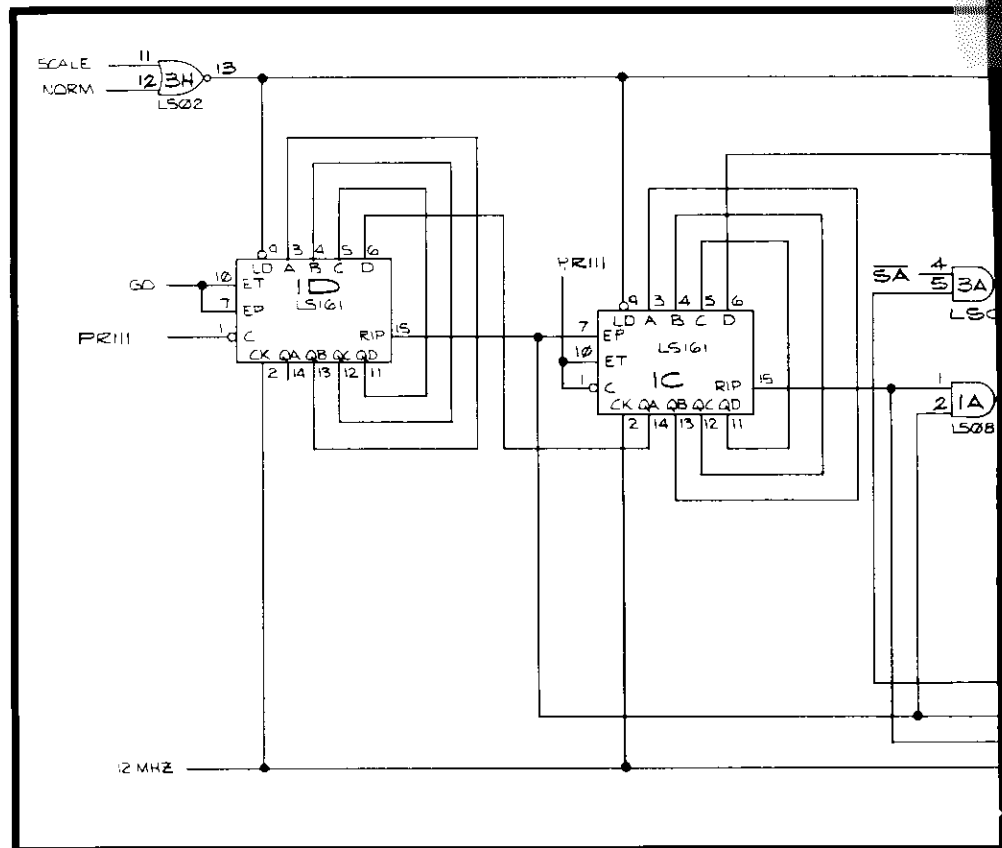
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STAR WARS Analog Vector-Generator PCB

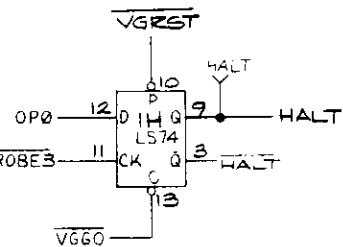
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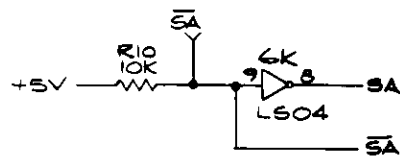
SP-225 Sheet 13B
1st printing



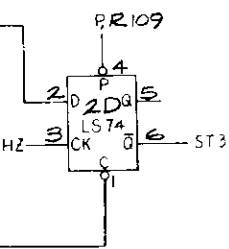
Halt Flag



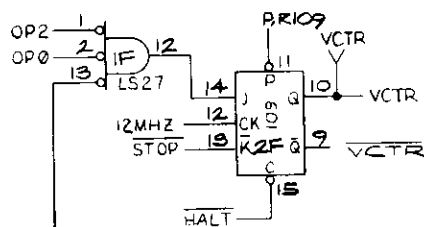
Signature Analysis



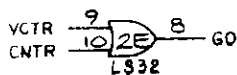
der Disable



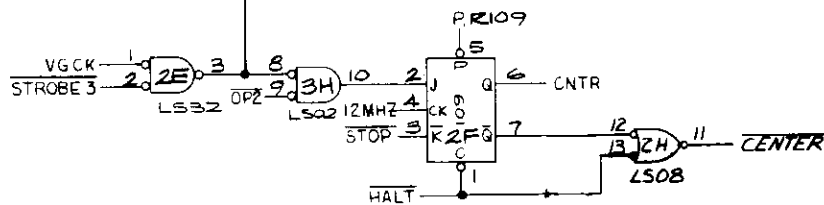
Vector Flag



Go Flag



Center Flag



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STAR WARS Analog Vector-Generator PCB

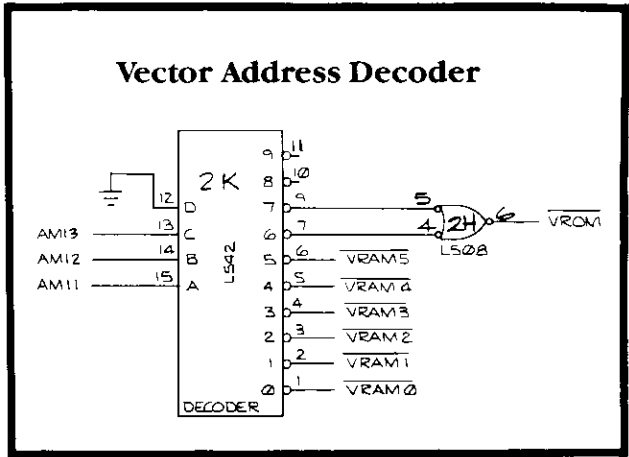


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SP-225 Sheet 13A
1st printing

The diagram shows a 74181 ALU Data Buffer. The chip is connected with pin 19 to GND, pin 16 to VCC, and pin 15 to A0. The output pins 2 through 9 are connected to a 10K pull-up network. The pull-up network consists of resistors R3 through R9 connected to +5V and R2 connected to pin 15. The output lines are labeled DVG7 through DVG0.



Vector ROM

The diagram shows a 2732 Vector ROM chip with the following connections:

- Address Bus (A0-A11):**
 - A11: AM11
 - A10: AM10
 - A9: AM9
 - A8: AM8
 - A7: AM7
 - A6: AM6
 - A5: AM5
 - A4: AM4
 - A3: AM3
 - A2: AM2
 - A1: AM1
 - A0: AM0
- Data Bus (D0-D7):**
 - D7: DVG 7
 - D6: DVG 6
 - D5: DVG 5
 - D4: DVG 4
 - D3: DVG 3
 - D2: DVG 2
 - D1: DVG 1
 - D0: DVG 0
- Control Signals:**
 - OE (Output Enable): Connected to ground (pin 20).
 - CE (Chip Enable): Connected to a bus labeled VROM (pin 18).

Vector RAM

	3L 137211-001	3M 137211-001	3P 137211-001	4L 137211-001	4M 137211-001	4P 137211-001
19						A10
22						A9
23						A8
1						A7
2						A6
3						A5
4						A4
5						A3
6						A2
7						A1
8						A0
21						CWE

D7						17	DVG7
D6						16	DVG6
D5						15	DVG5
D4						14	DVG4
D3						13	DVG3
D2						12	DVG2
D1						11	DVG1
D0						9	DVG0

CE	OE	CE	OE	CE	OE	CE	OE	CE	OE	CE	OE
10	20	10	20	10	20	10	20	10	20	10	20
VRAM0		VRAM1		VRAM2		VRAM3		VRAM4		VRAM5	

SP-225 Sheet 12A
1st printing

Vector Interface Buffer

The diagram illustrates the internal circuitry of a Vector Interface Buffer. It features an LS244 buffer with inputs connected to J17 pins and outputs connected to various system signals. The buffer is powered by 1G and 2G pins, with 1G connected to ground. Logic gates (504, 5P, 3A, LS00) are used to generate control signals like VMEM, BUFFER, 1.5 MHz, and VW from the buffer outputs.

Inputs (J17):

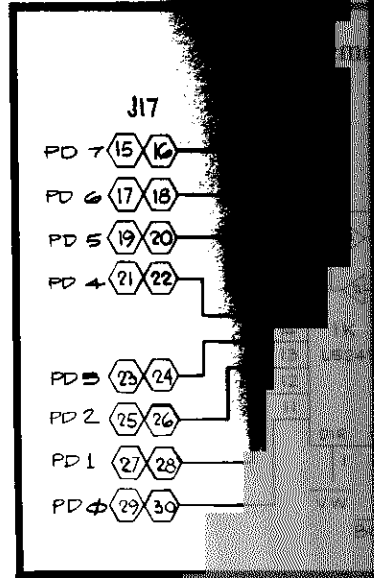
- EV MEM (pins 65, 66)
- EVGRST (pins 63, 64)
- EVGGO (pins 71, 72)
- E 12 MHz (pins 73, 74)
- E 6 MHz (pins 67, 68)
- E 3 MHz (pins 69, 70)
- E 1.5 MHz (pins 75, 76)

Outputs and Internal Connections:

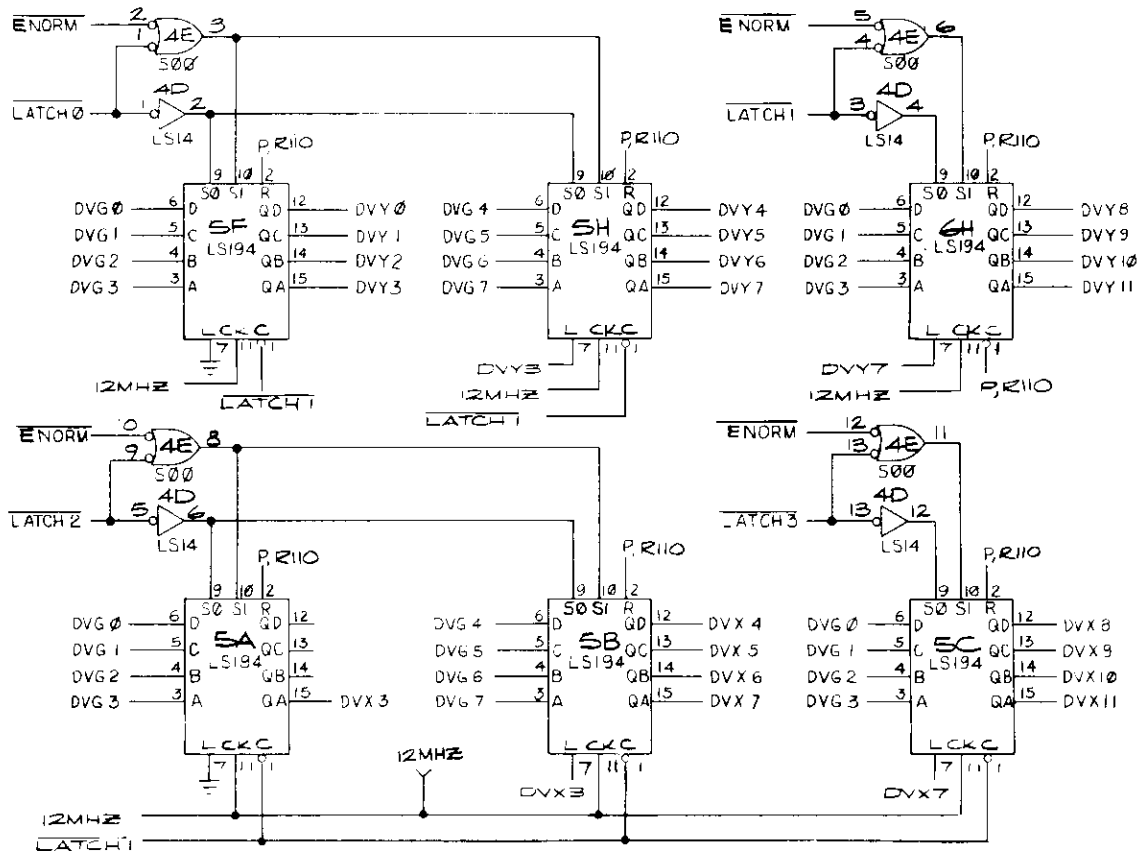
- Pin 2: Input to LS244 A
- Pin 15: Input to LS244 Y
- Pin 17: Input to LS244 Y
- Pin 4: Input to LS244 A
- Pin 6: Input to LS244 A
- Pin 13: Input to LS244 A
- Pin 11: Input to LS244 A
- Pin 8: Input to LS244 A
- Pin 1G: Ground
- Pin 2G: Ground
- Pin 19: Ground
- Pin 18: Output to VMEM
- Pin 5: Output to VGHALT
- Pin 3: Output to VGRST
- Pin 16: Output to VGGO
- Pin 14: Output to 12 MHz
- Pin 7: Output to 6 MHz
- Pin 9: Output to 3 MHz
- Pin 12: Output to SACLK
- Pin 12: Output to VGCK
- Pin 13: Output to VMEM
- Pin 12: Output to BUFFER
- Pin 11: Output to 1.5 MHz
- Pin 5: Output to VW

Logic Gates:

- 504: Inverter (5P)
- 3A: AND gate (5P)
- LS00: NAND gate (3A)



Vector Data Shifters



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STAR WARS Analog Vector-Generator PCB



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SP-225 Sheet 12B
1st printing

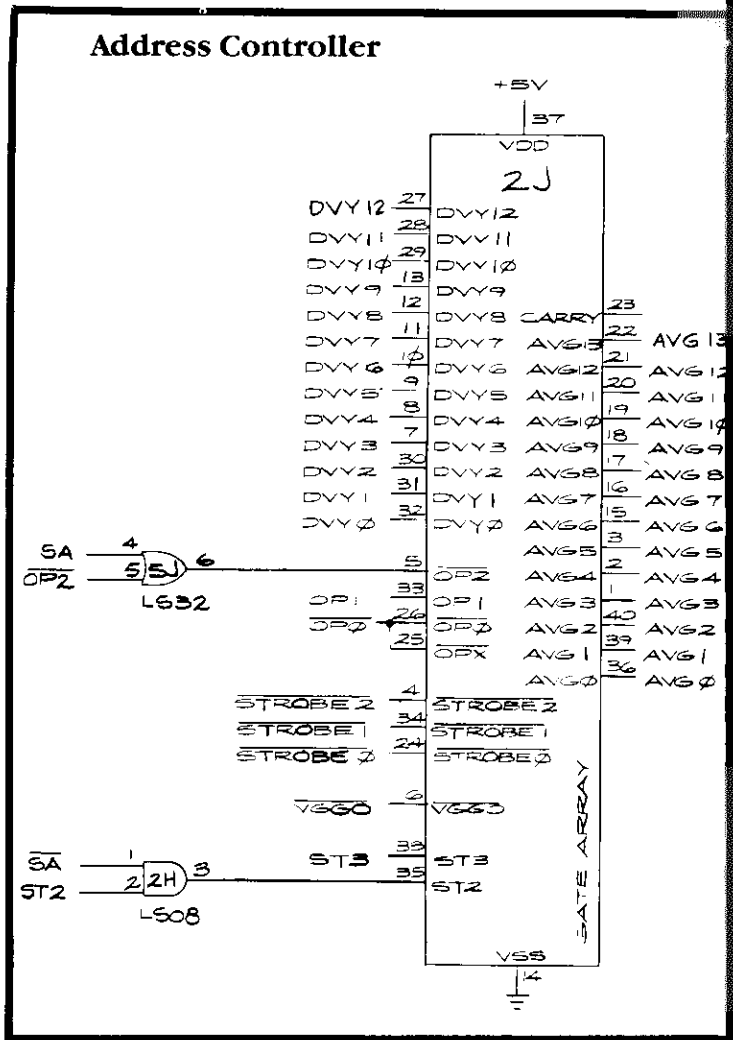
Op Code and Intensity Latches

LATCH 1

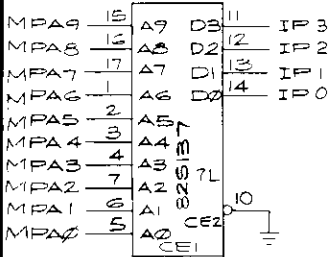
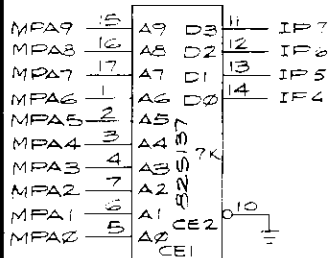
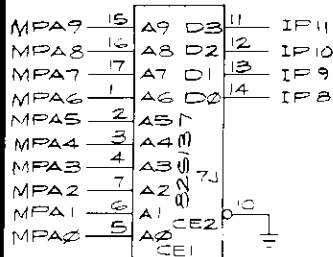
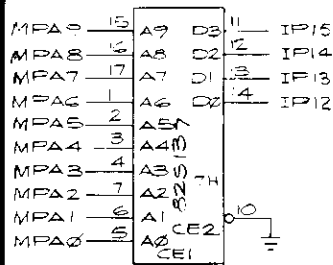
DVG 7 — 4 D Q 2 OP2
DVG 6 — 12 D Q̄ 3 OP2̄
DVG 5 — 5 D Q 10 OP1
DVG 4 — 13 D Q̄ 11 OP1̄
Q 7 OP0
Q̄ 6 OP0̄
Q 15 DYY12
Q̄ 14 DYY12̄
CS 1 P, R110

LATCH 3

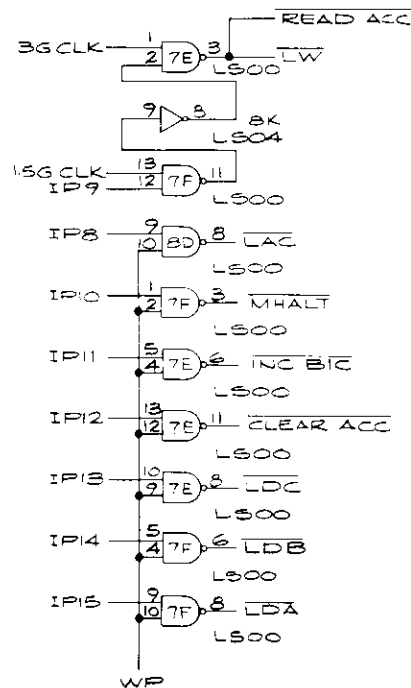
DVG 7 — 12 D Q 10 Z2
DVG 6 — 5 D Q̄ 11 Z2̄
DVG 5 — 13 D Q 7 Z1
DVG 4 — 4 D Q̄ 6 Z1̄
Q 15 Z0
Q̄ 14 Z0̄
Q 2 DVX 12
Q̄ 3 DVX 12̄
CS 1 LATCH 1



Instruction PROM



Instruction Strobe Gates



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STAR WARS Main PCB

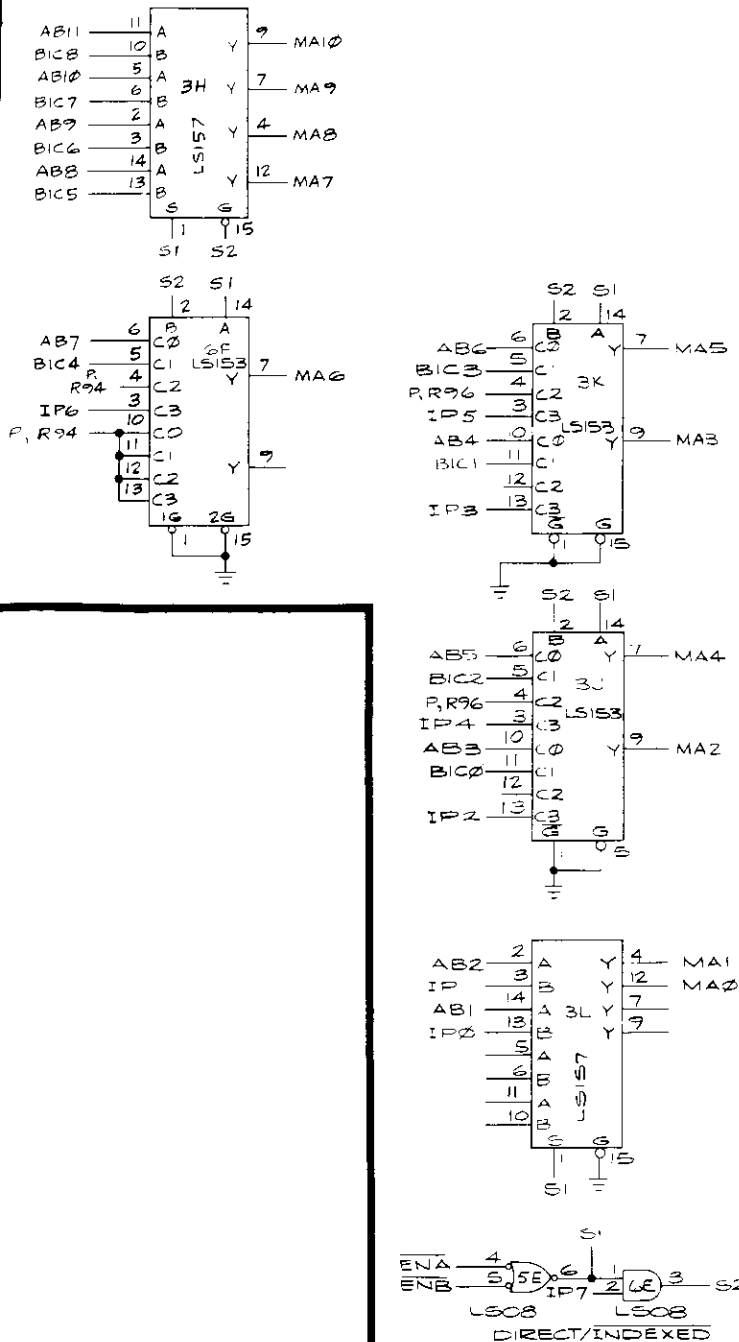


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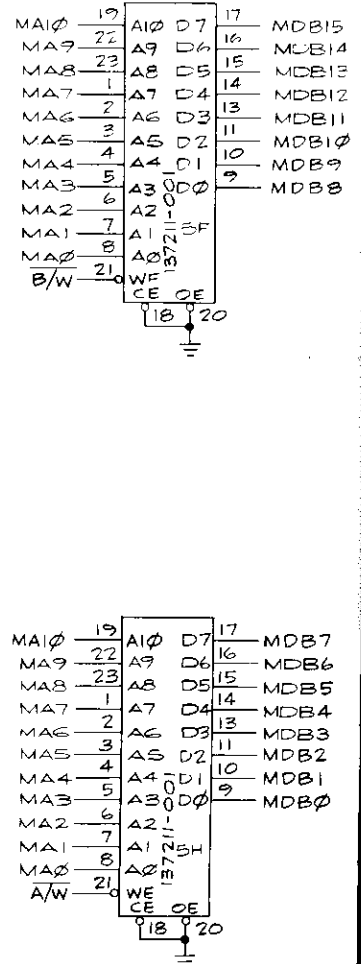
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SP-225 Sheet 11A
1st printing

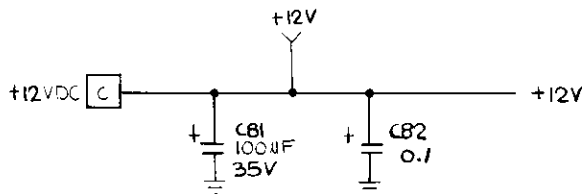
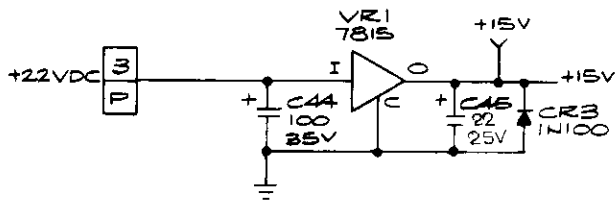
Matrix Processor Address Selector



Matrix Processor RAM



Power Input



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STAR WARS Analog Vector-Generator PCB

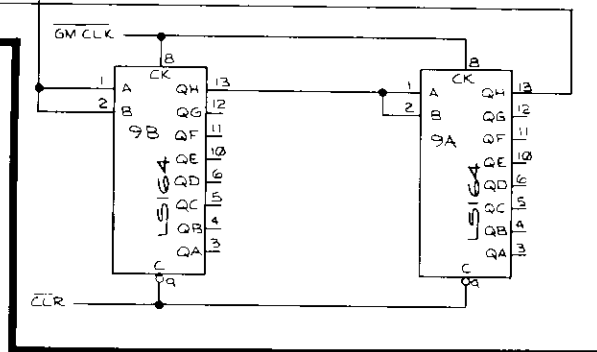
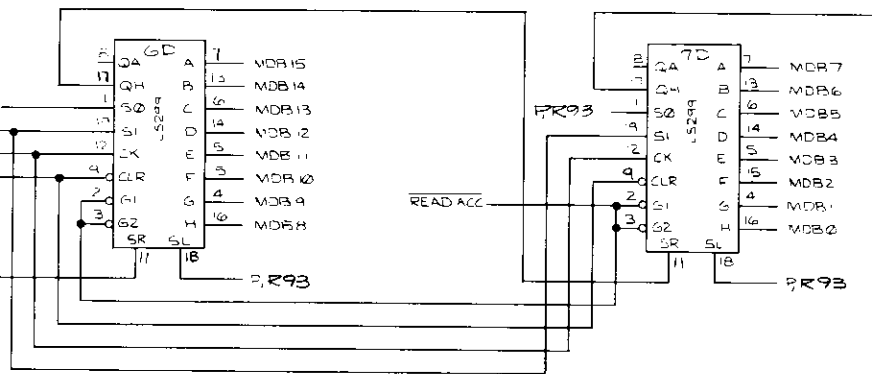


A Warner Communications Company

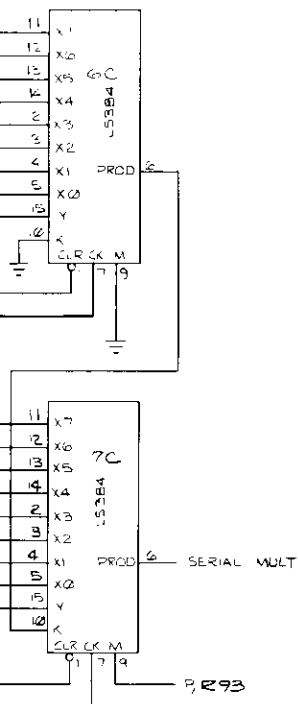
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SP-225 Sheet 11B
1st printing

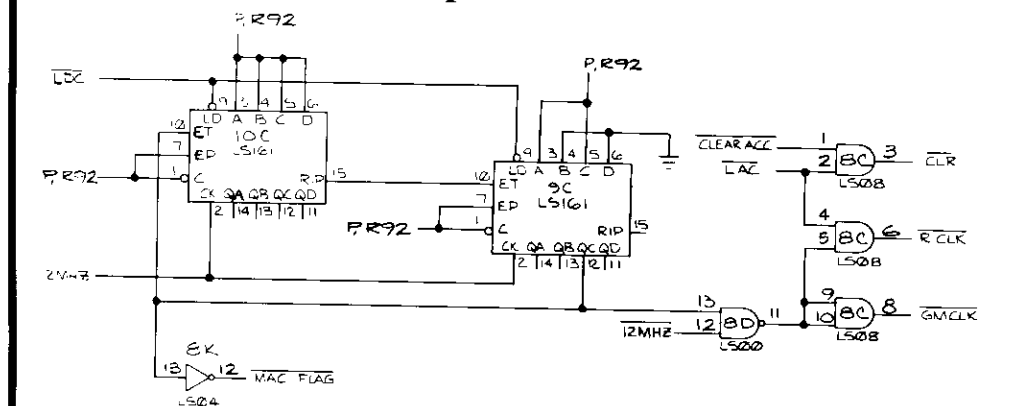
Accumulator



al Multiplier



Multiplier/Accumulator Clock



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STAR WARS Main PCB

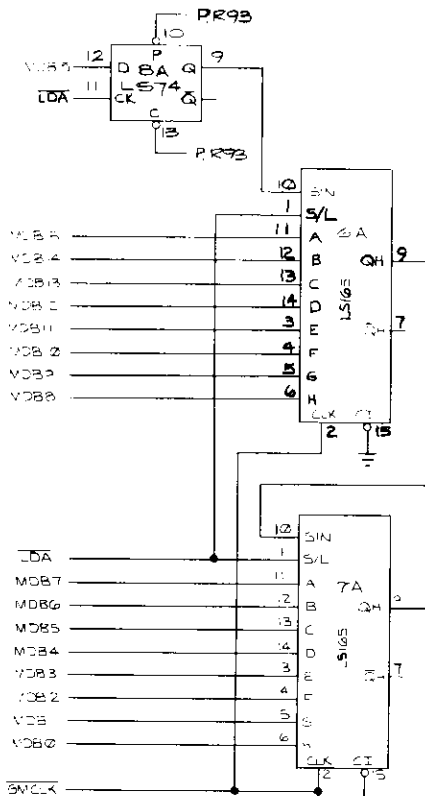


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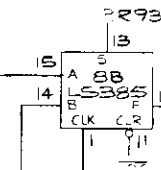
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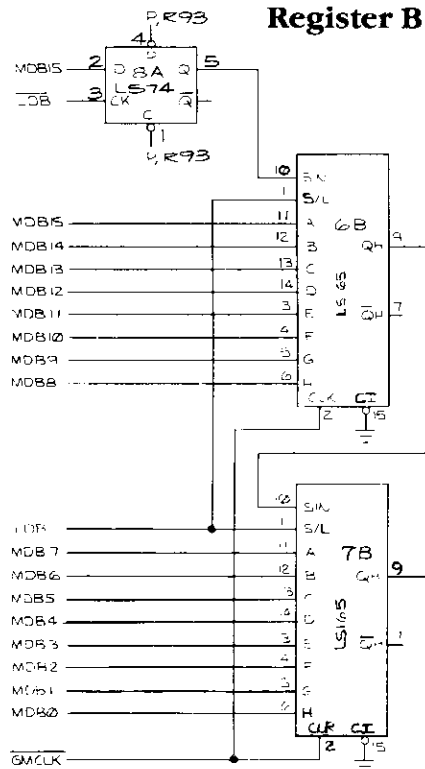
Register A



Serial Subtractor



Register B

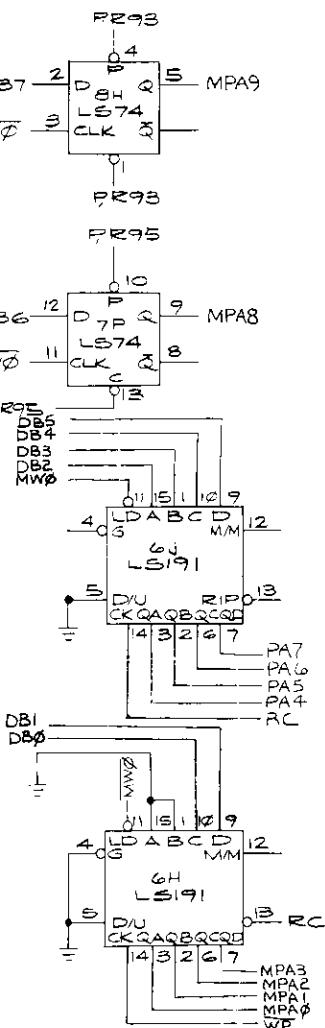


Serial

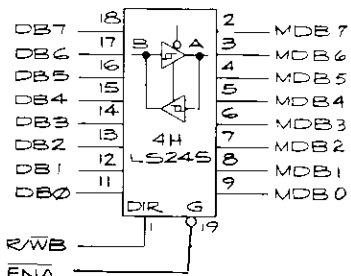
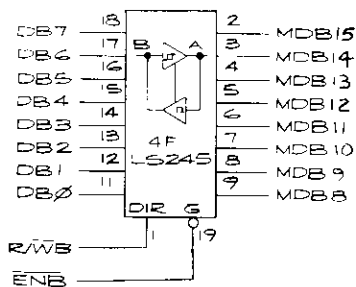
MDB15
MDB14
MDB13
MDB12
MDB11
MDB10
MDB9
MDB8

MDB7
MDB6
MDB5
MDB4
MDB3
MDB2
MDB1
MDB0

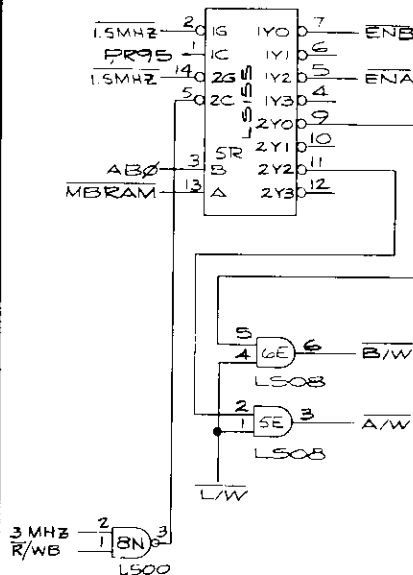
Matrix Processor Address Counter



Matrix Processor Data Selector



Matrix Processor Address and Data Selector Control



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STAR WARS Main PCB



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1st printing

Matrix Processor Clock

The diagram illustrates the clock logic for a Matrix Processor. It includes a 74LS161 counter and a 74LS74 flip-flop. The counter is clocked by a 2 MHz signal and a 1.5 GHz signal. Its outputs (QA-QD) are connected to various logic gates (AND, OR, XOR) to generate 1.2 MHz, WD, and WP signals. The flip-flop is clocked by MHALT and MATH RUN signals, and its outputs (Q, Q-bar) are connected to the counter and other logic gates.

Block Index Counter

The diagram illustrates a Block Index Counter circuit using two LS191 counters. The circuit is divided into two main sections, each handling a 4-bit binary input (DB7-DB4 and DB3-DB0) and producing a 4-bit binary output (BIC7-BIC4 and BIC3-BIC0).

Top Counter (LS191):

- Inputs:** DB7, DB6, DB5, DB4, and MW2. DB7, DB6, and DB5 are connected to inputs A, B, and C respectively. DB4 and MW2 are connected to input D. Input LD (pin 4) is connected to ground (pin 5).
- Outputs:** BIC7 (pin 12), BIC6 (pin 13), BIC5 (pin 7), and BIC4 (pin 6).
- Control:** The INCBIC signal is connected to the D/U pin (pin 14).

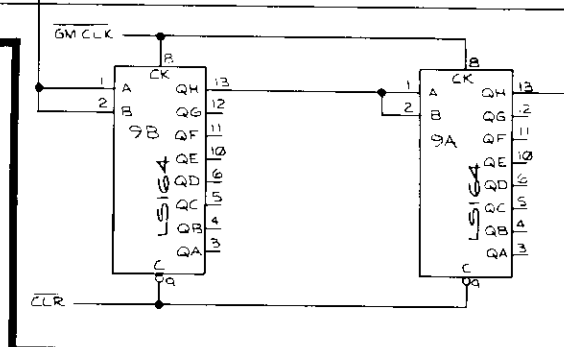
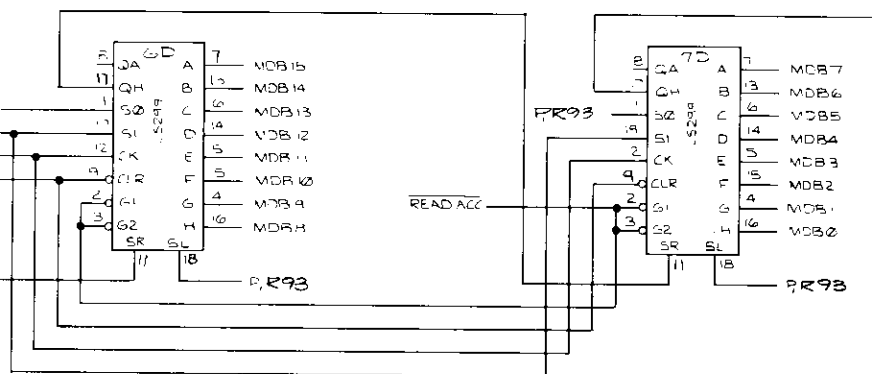
Bottom Counter (LS191):

- Inputs:** DB3, DB2, DB1, and DB0. DB3, DB2, and DB1 are connected to inputs A, B, and C respectively. DB0 is connected to input D. Input LD (pin 4) is connected to ground (pin 5).
- Outputs:** BIC3 (pin 12), BIC2 (pin 13), BIC1 (pin 7), and BIC0 (pin 6).
- Control:** The INCBIC signal is connected to the D/U pin (pin 14).

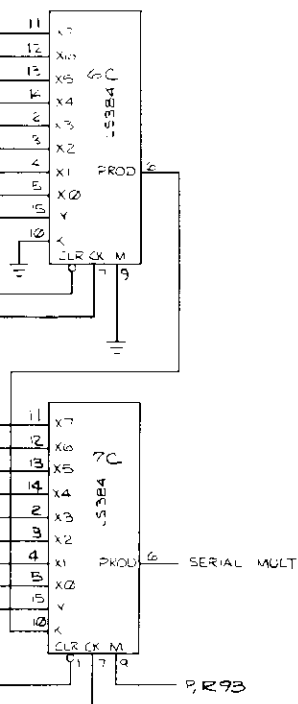
Additional Connections:

- The output of the top counter's pin 13 (BIC6) is connected to the input of the bottom counter's pin 14 (D/U).
- The output of the bottom counter's pin 13 (BIC2) is connected to the input of the top counter's pin 14 (D/U).

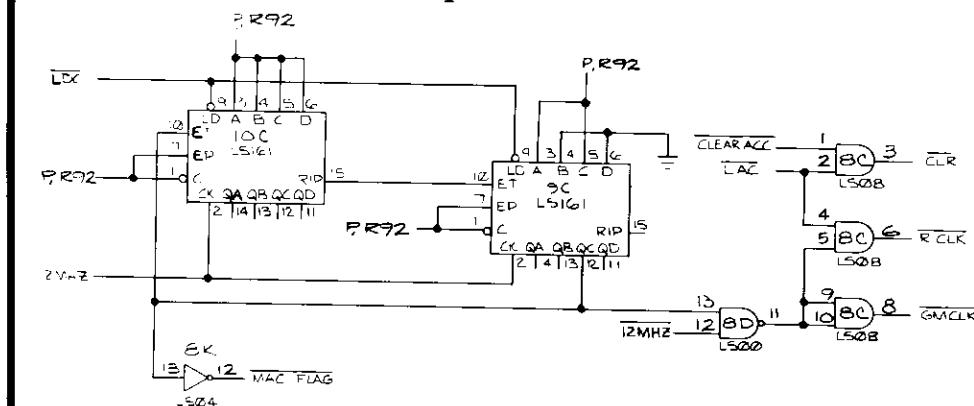
Accumulator



al Multiplier



Multiplier/Accumulator Clock



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STAR WARS Main PCB

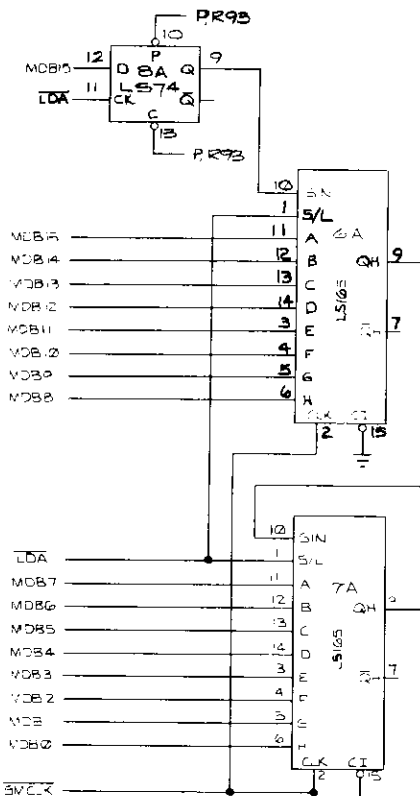


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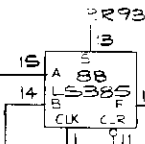
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SP-225 Sheet 10A
1st printing

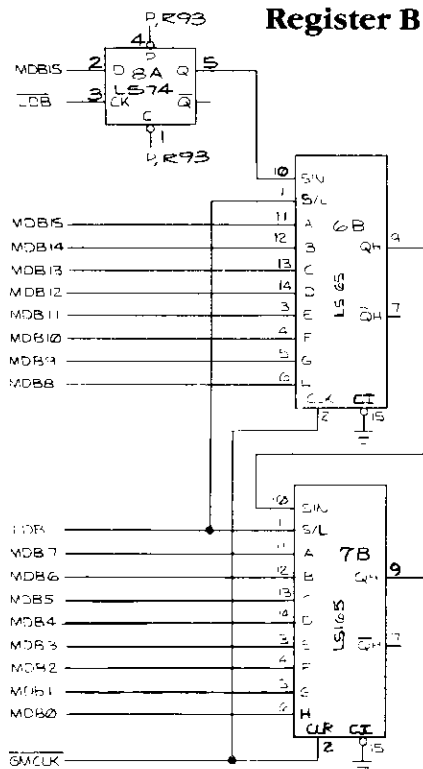
Register A



Serial Subtractor



Register B

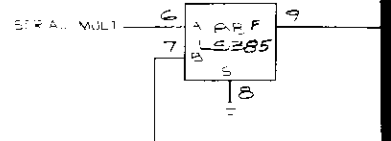


Serial

MCB15
MCB14
MCB13
MCB12
MCB11
MCB10
MCB9
MCB8

MCB7
MCB6
MCB5
MCB4
MCB3
MCB2
MCB1
MCB0

PR93
IPB
RCLK
CLEAR ACC



der

14

15

2

6

9

4

5

2

6

9

14

15

2

6

9

14

15

2

6

9

14

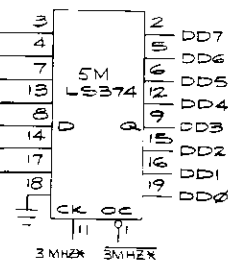
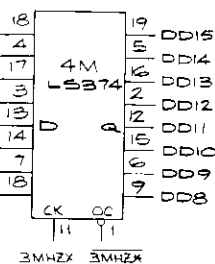
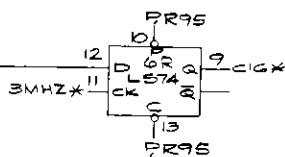
15

2

6

9

Difference Latch



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STAR WARS Main PCB

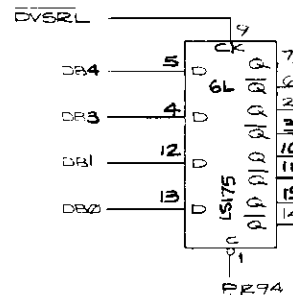
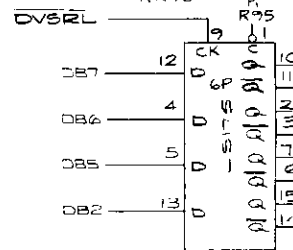
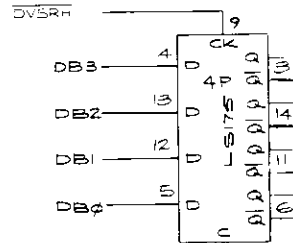
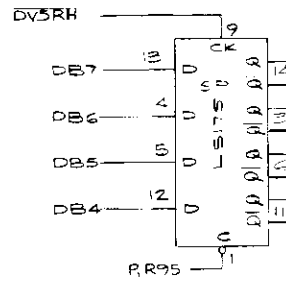


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SP-225 Sheet 9A
1st printing

Divisor Inverting Latch



DD15	16	B4	C4
1	A4	Z4	
DD14	4	B3	
3	A3	M	
DD13	7	B2	
8	A2	M	
DD12	11	B1	J
10	A1	M	
13	C0	SN	

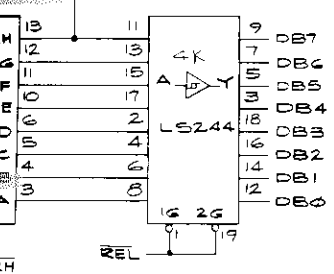
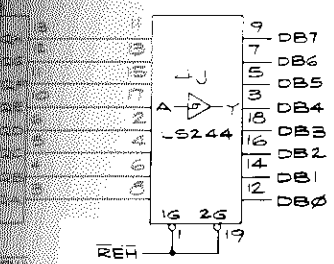
DD11	16	B4	C4
1	A4	Z4	
DD10	4	B3	
3	A3	M	
DD9	7	B2	
8	A2	J	
DD8	11	B1	
10	A1	M	
13	C0	4N	

DD7	16	B4	C4
1	A4	Z4	
DD6	4	B3	
3	A3	M	
DD5	7	B2	
8	A2	M	
DD4	11	B1	J
10	A1	M	
13	C0	6N	

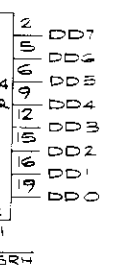
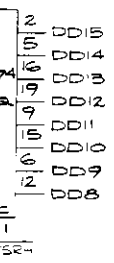
DD3	16	B4	C4
1	A4	Z4	
DD2	4	B3	
3	A3	M	
DD1	7	B2	
8	A2	J	
DD0	11	B1	
10	A1	M	
13	C0	6M	

PR94

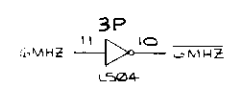
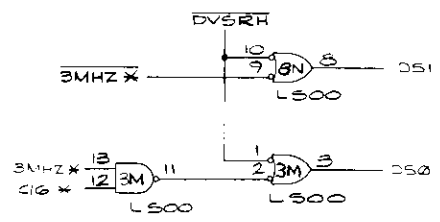
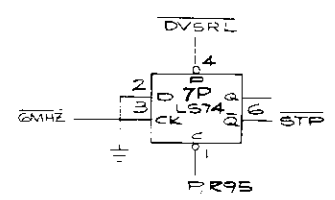
ient Shift Register



d Latch



Divider Control



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STAR WARS Main PCB

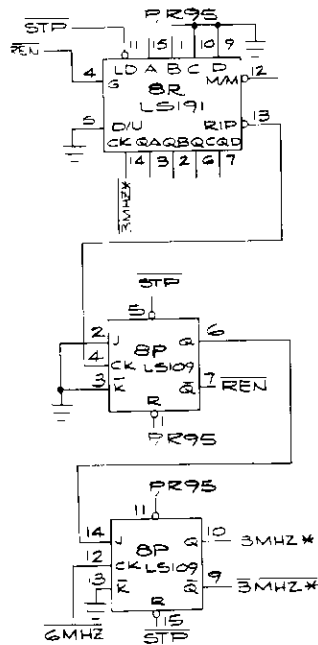


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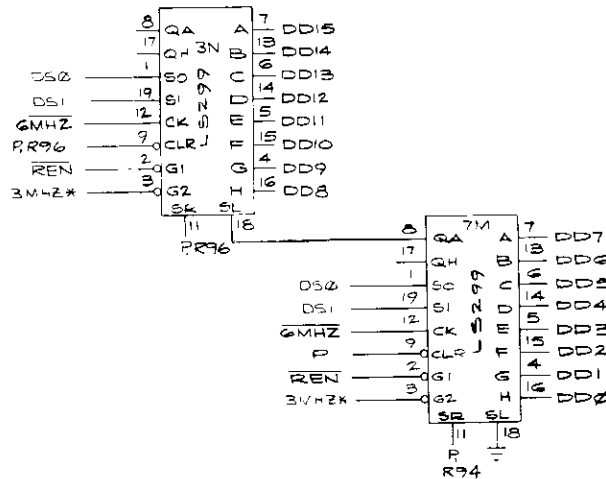
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SP-225 Sheet 1st page

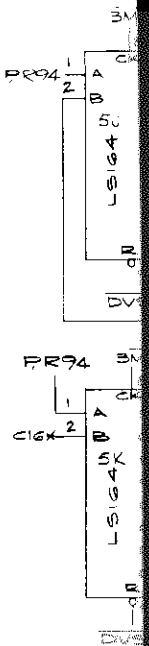
Divider Clock Generator



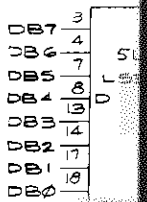
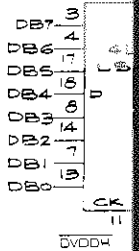
Dividend Shift Register



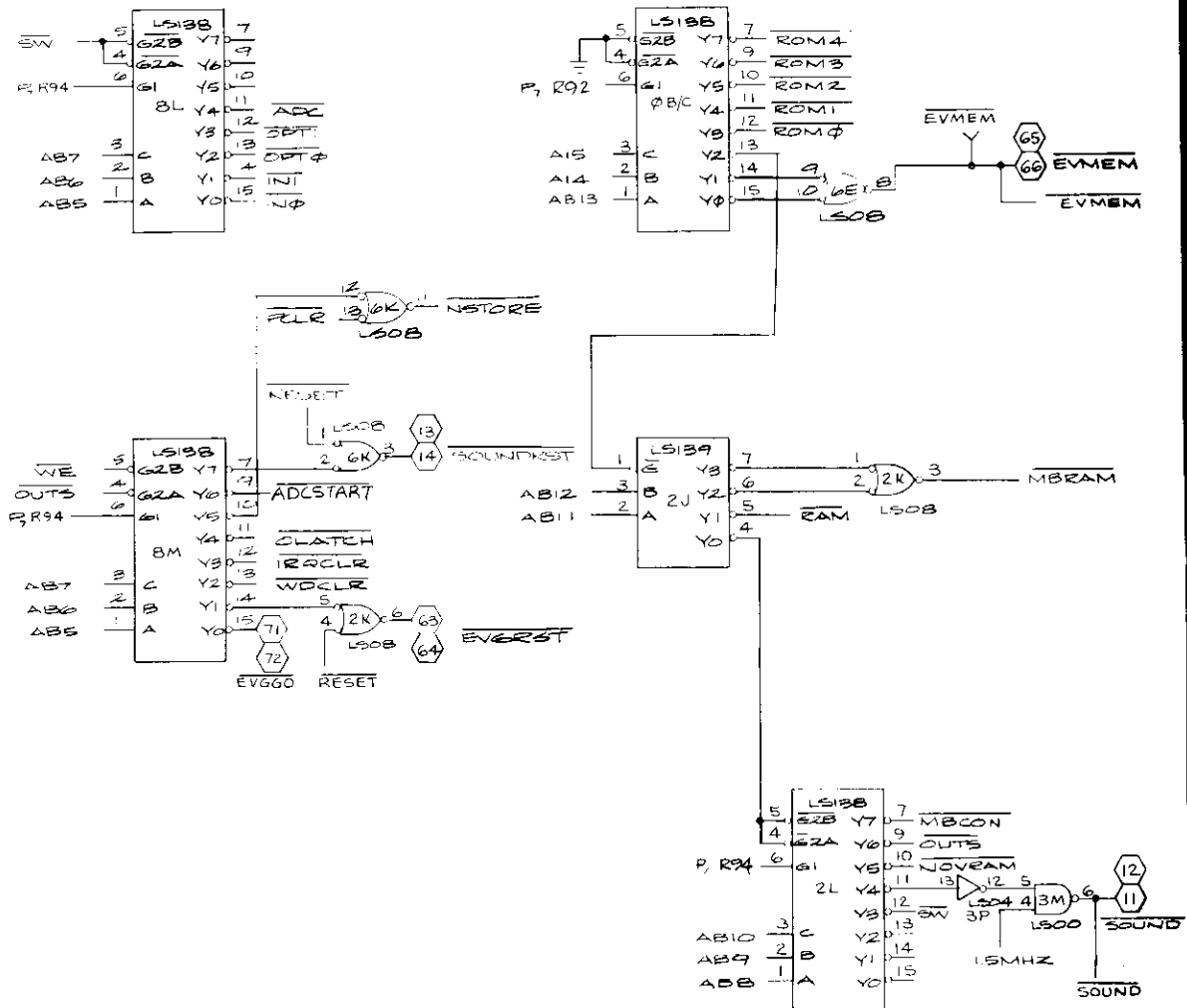
Quo



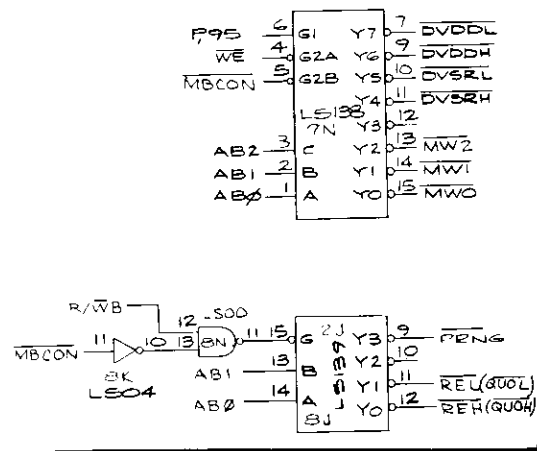
Dividen



Address Decoders



Math Address Decoders



[illegible]

The diagram illustrates the internal wiring of the Option Switches. It features two 8-bit switches, SW3 and SW2, each with pins 1 through 8. SW3 is labeled '10E/F' and SW2 is labeled '10D'. Both switches are connected to a +5V supply through resistors R50 through R57 (10K) and R43 through R49 (10K SPL). The outputs of the switches are connected to two 15244 comparators. The comparators are configured with pins 1 and 19 connected to GND, and pins 2 and 18 connected to +5V. The outputs of the comparators are connected to the D0-D7 and Dφ lines. The comparators are labeled '15244' and '9F'.

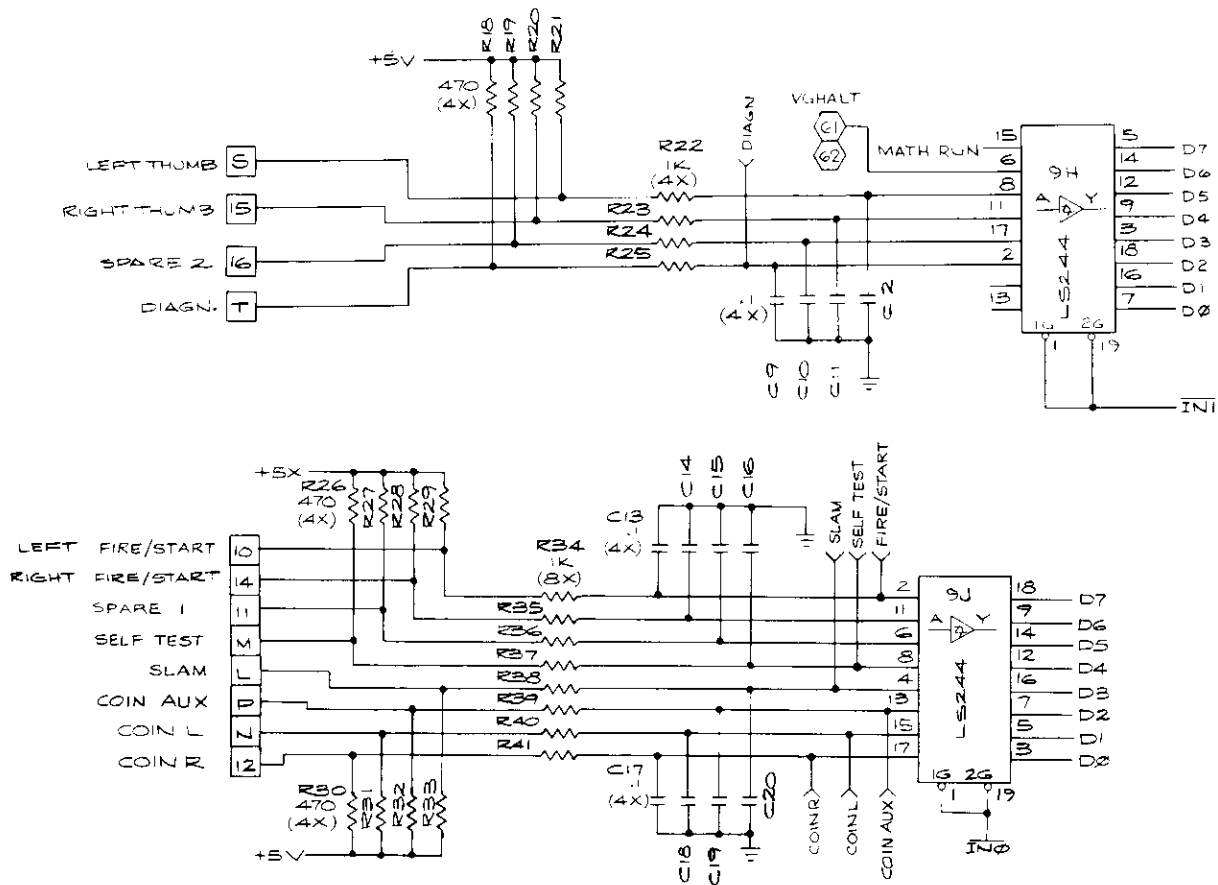
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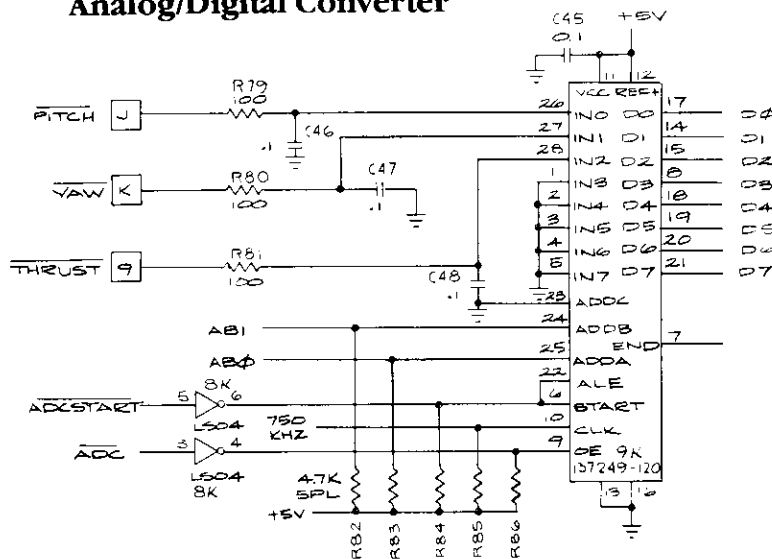
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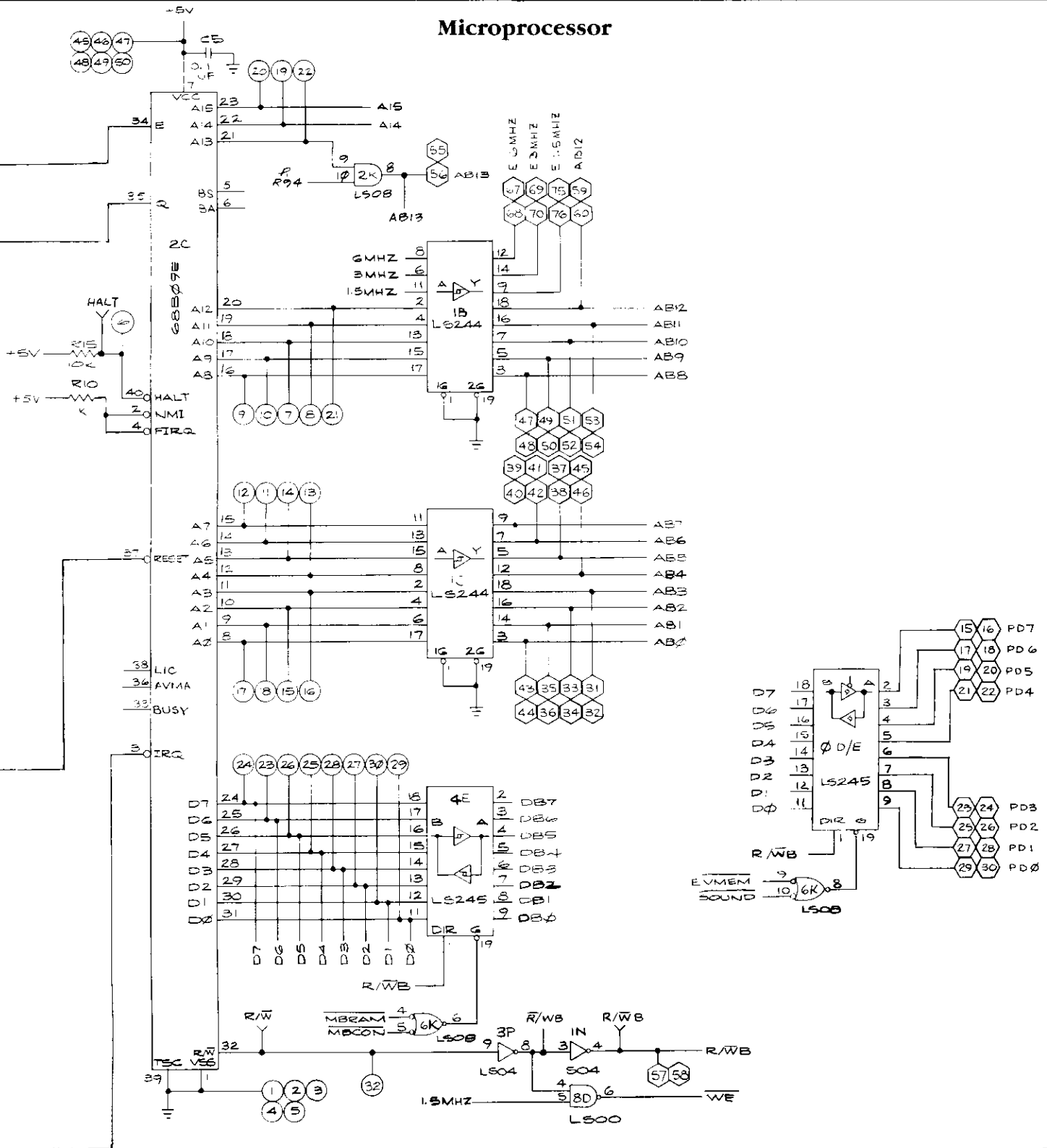
Coin Door and Control Panel Input



Analog/Digital Converter



Microprocessor



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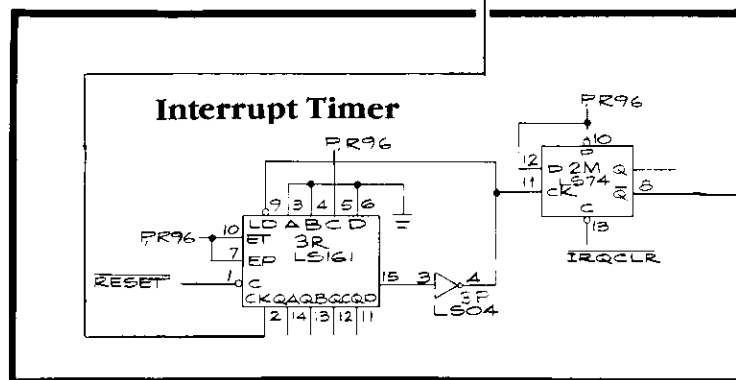
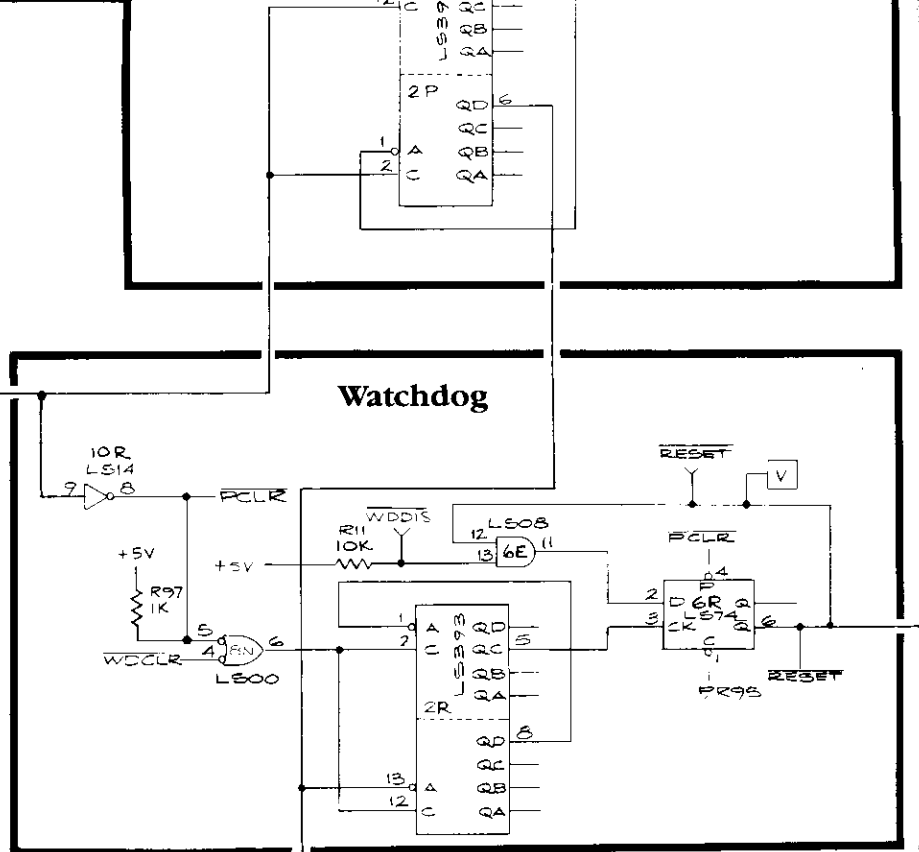
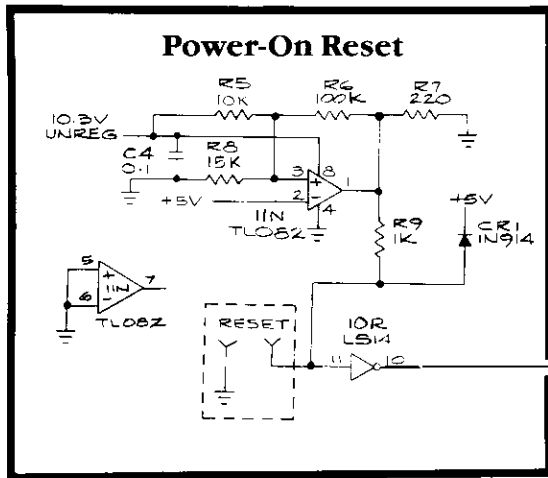
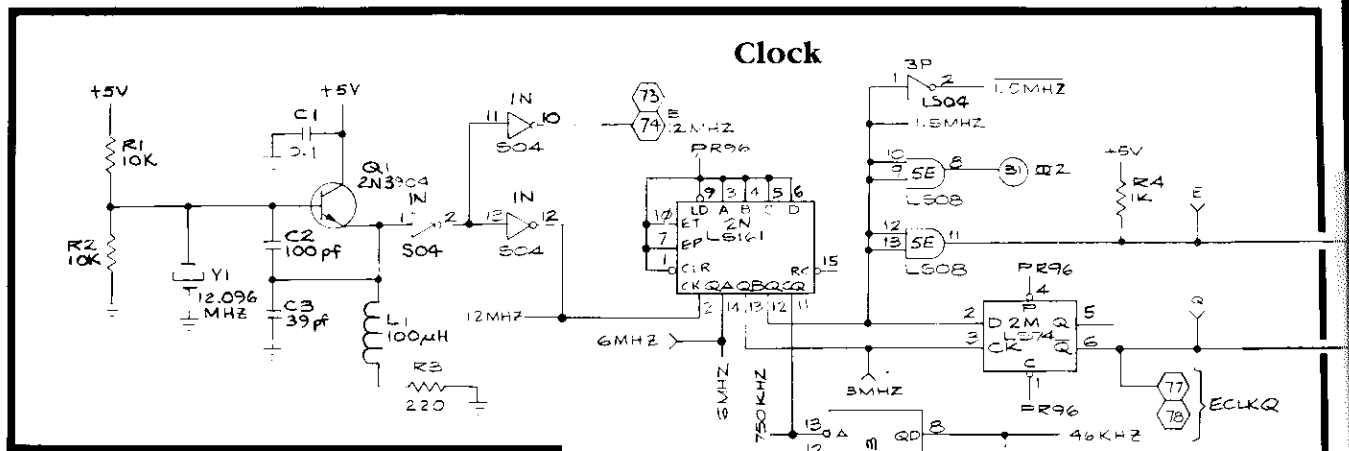
STAR WARS Main PCB



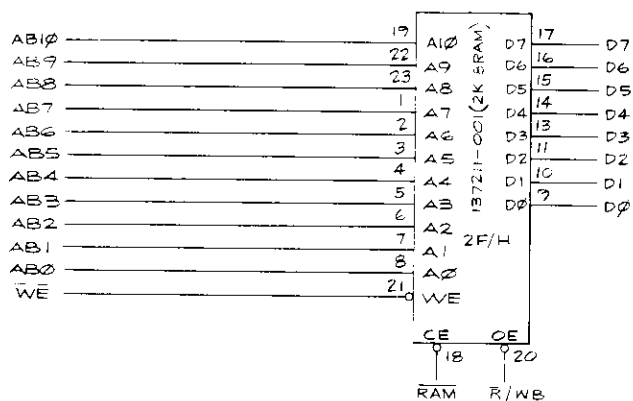
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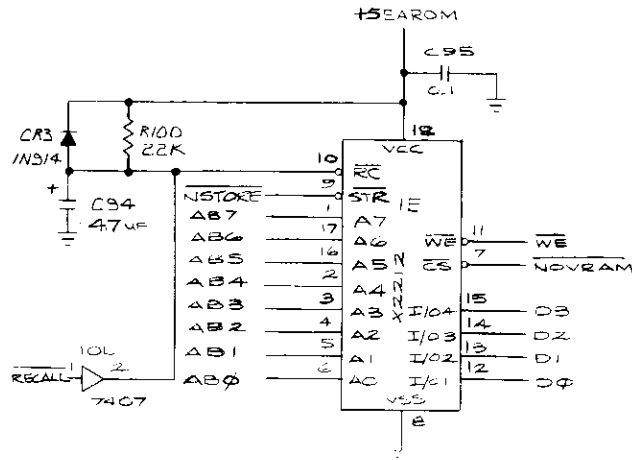
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RAM



High-Score and Bookkeeping Non-Volatile RAM



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STAR WARS Main PCB

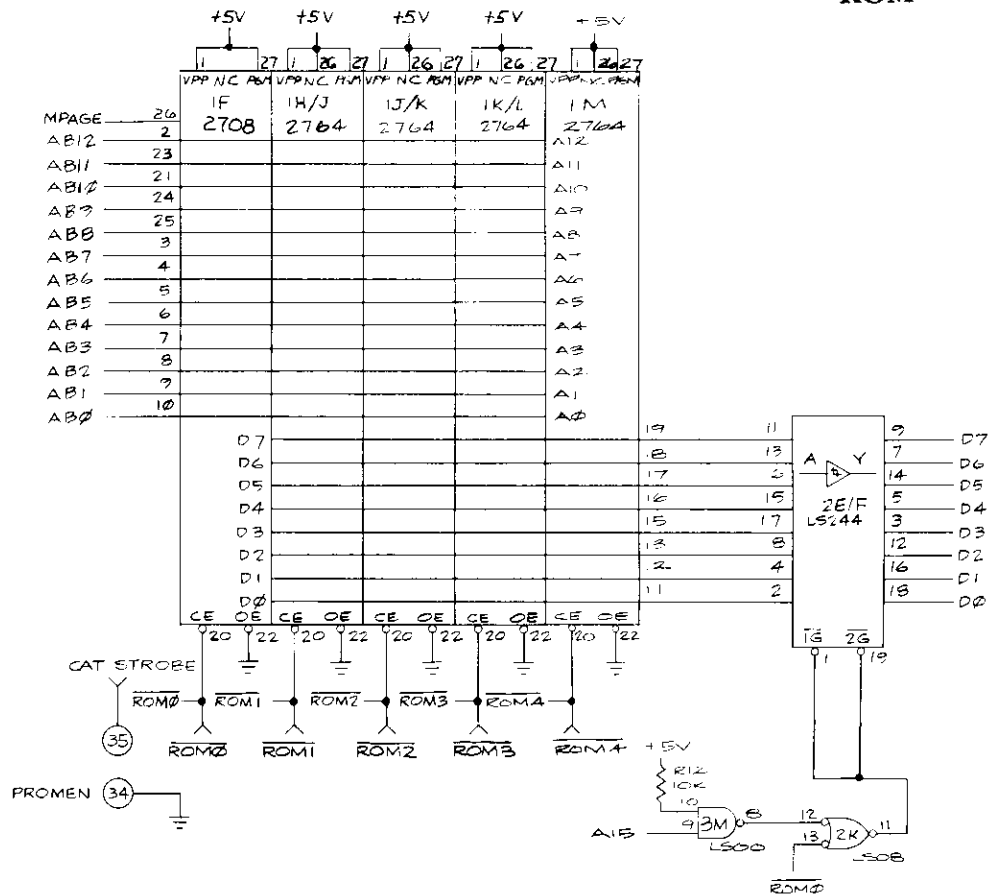


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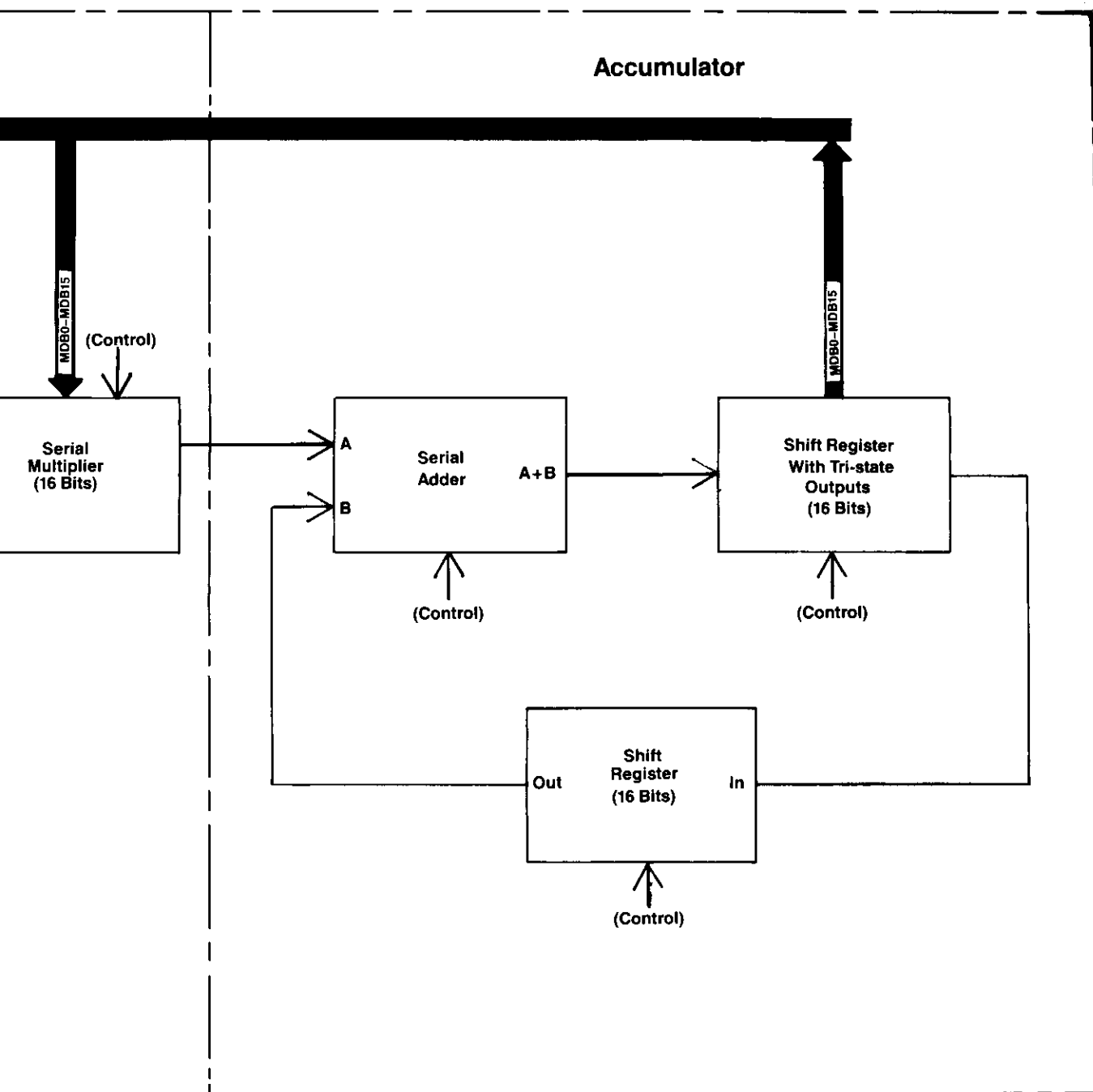
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ROM



ccumulator
+ (A-B) × C



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**STAR WARS Multiplier/Accumulator
Detailed Block Diagram**

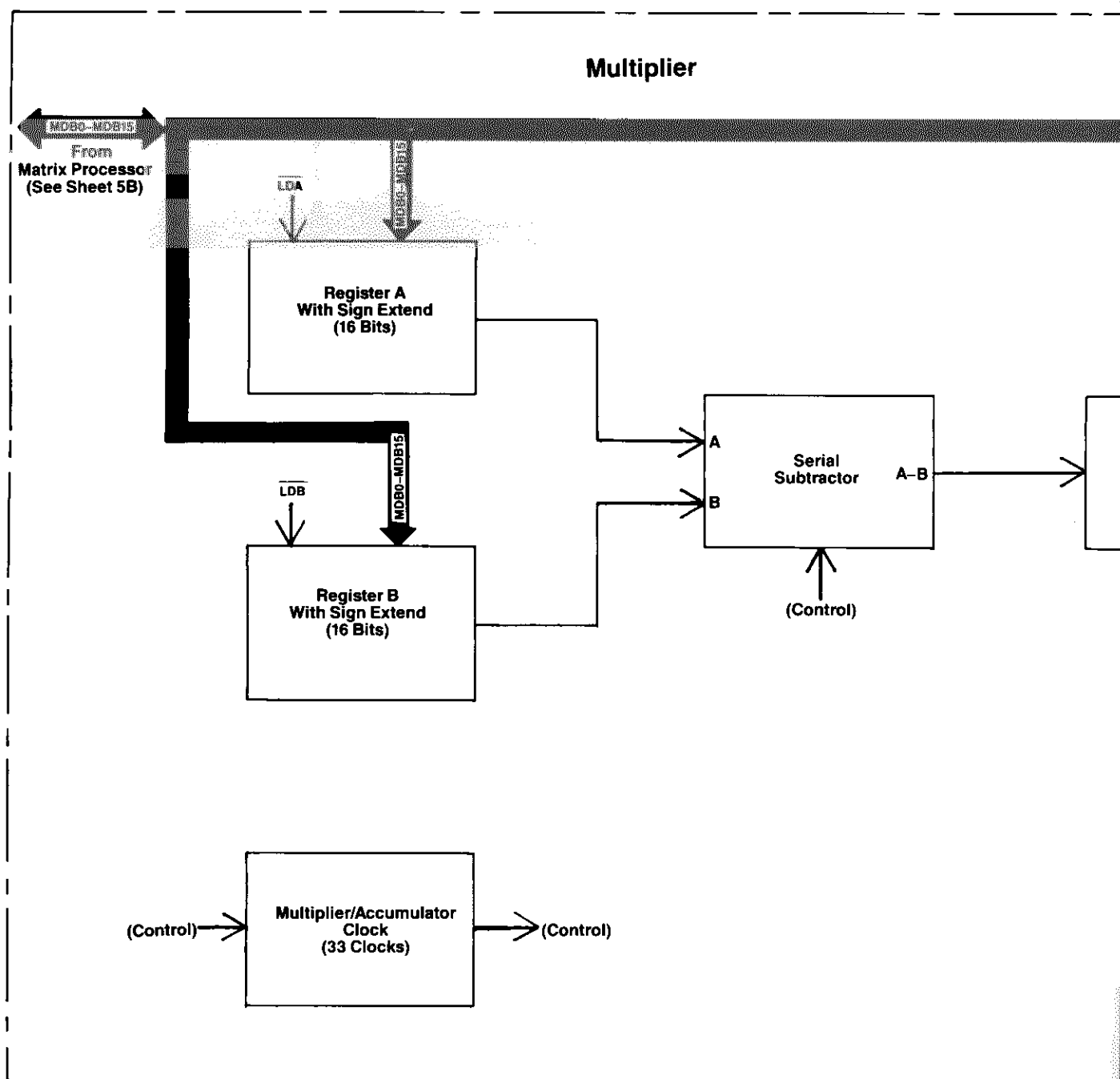


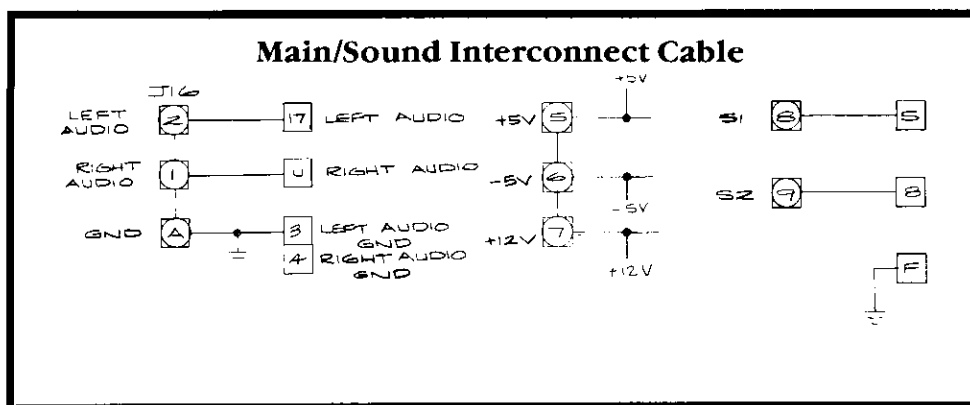
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Multiplier/
ACC = ACC





NOTE

- = J20 CONNECTOR
- = TEST CONNECTOR
- ◇ = J17 CONNECTOR
- ⊠ = J16 CONNECTOR

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STAR WARS Main PCB

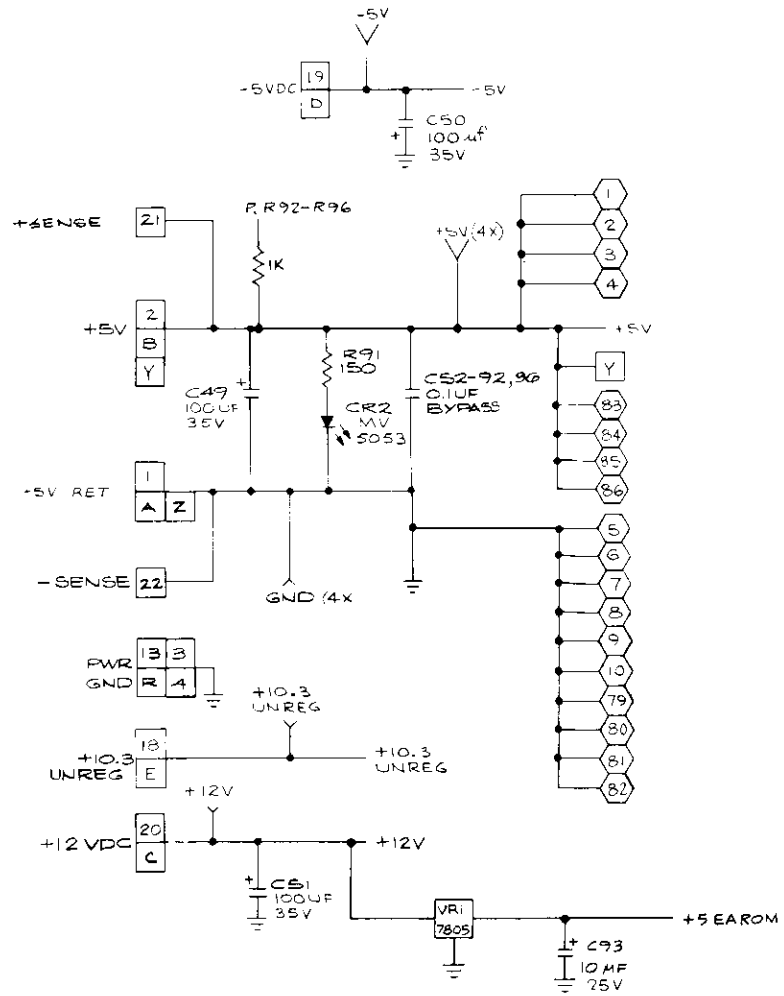


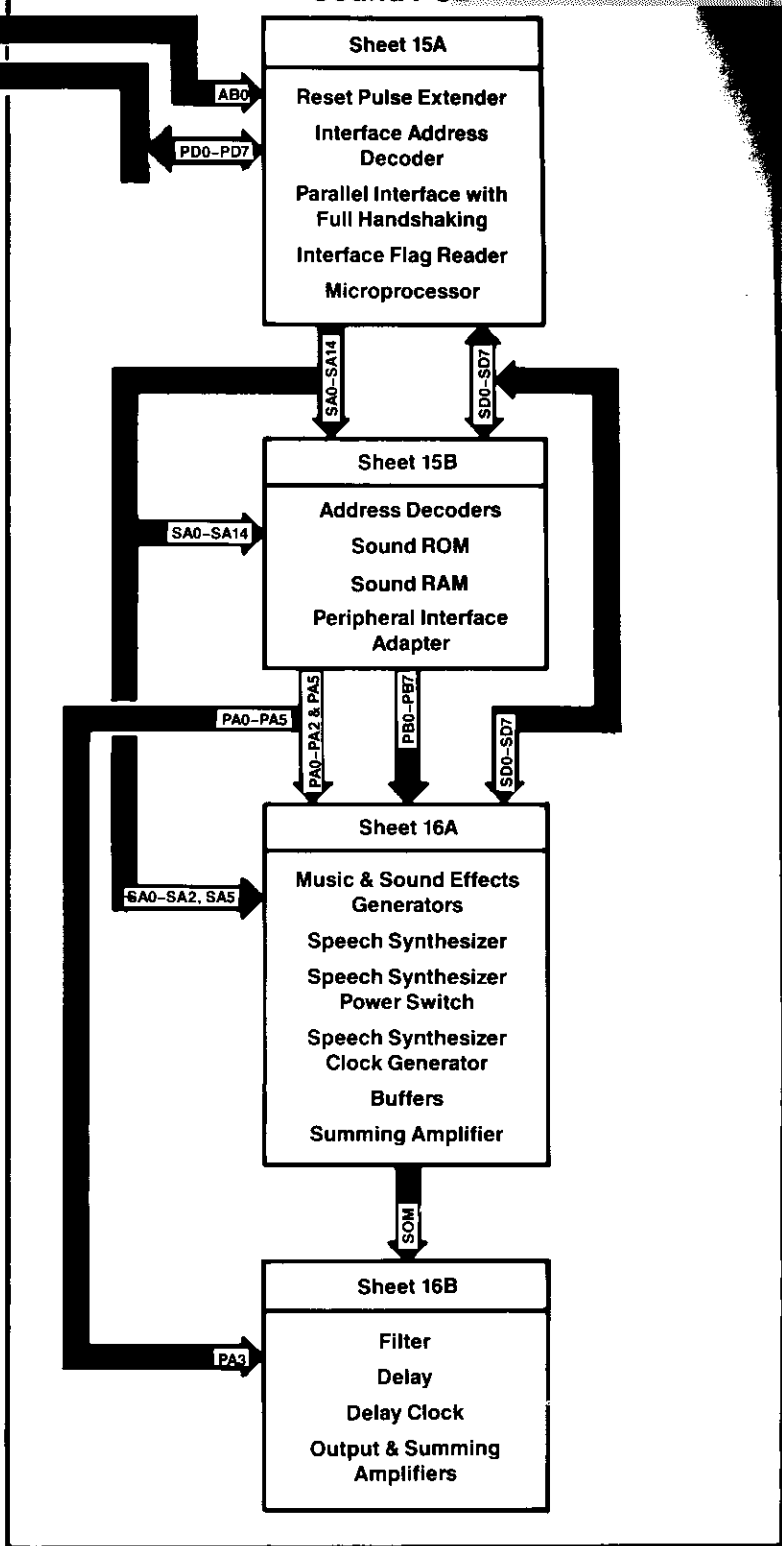
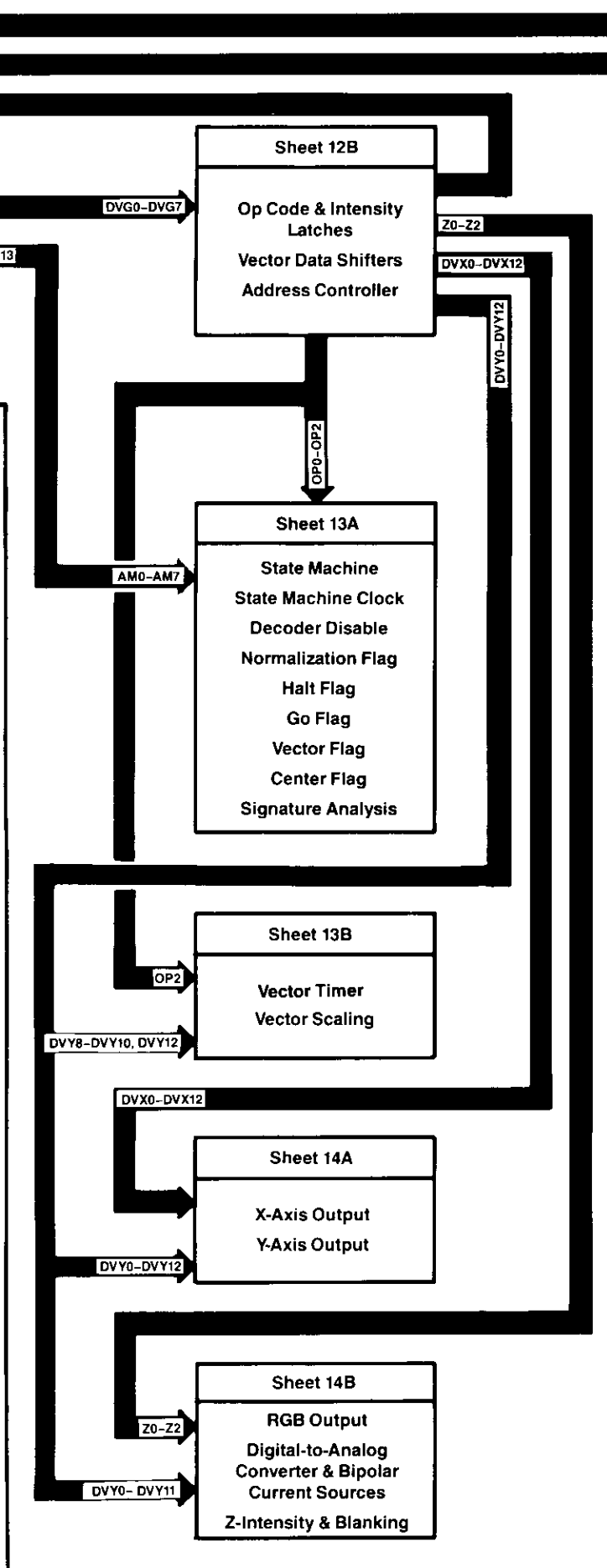
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Power Input





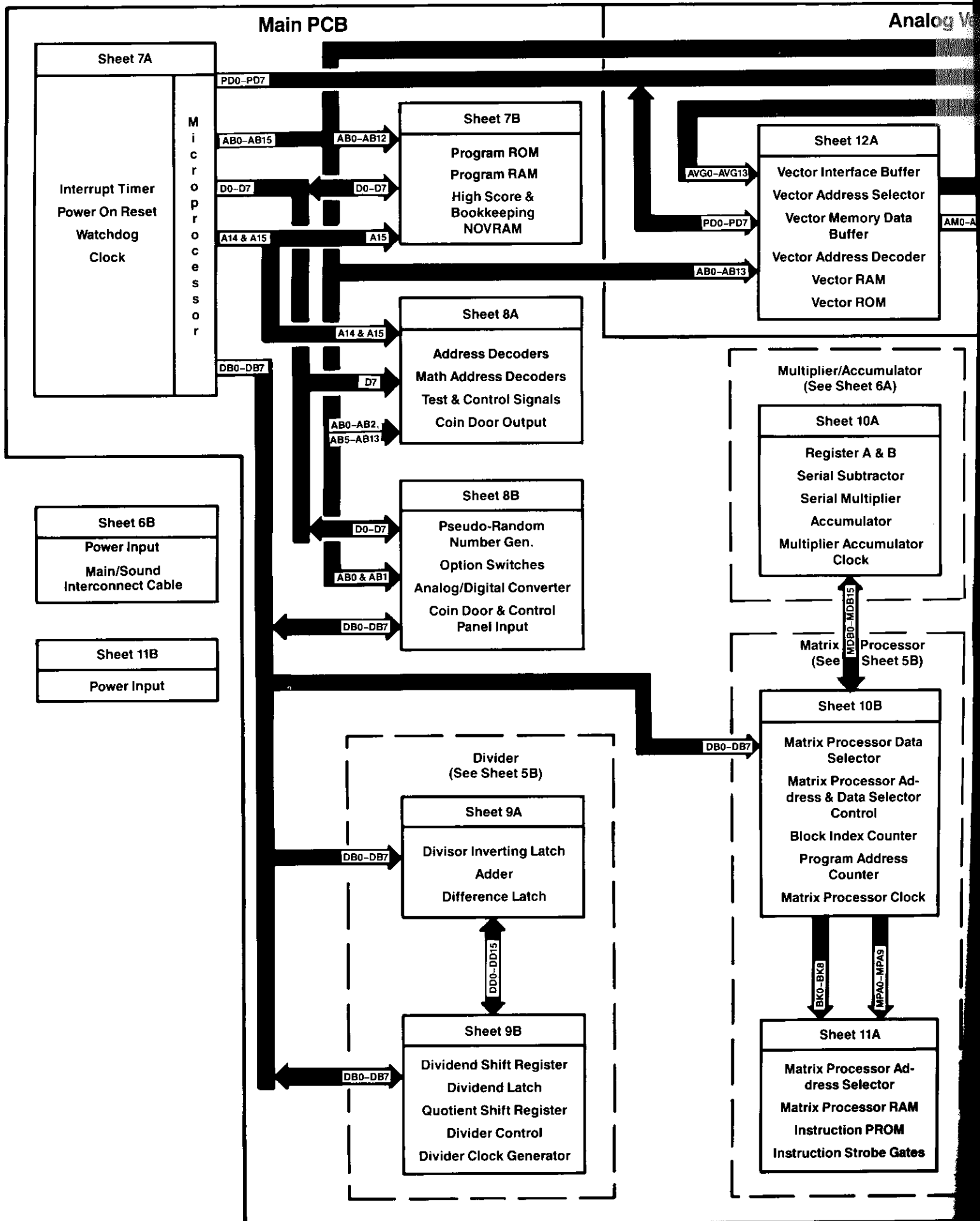
STAR WARS Functional Block Diagram and Guide to PCB Schematics

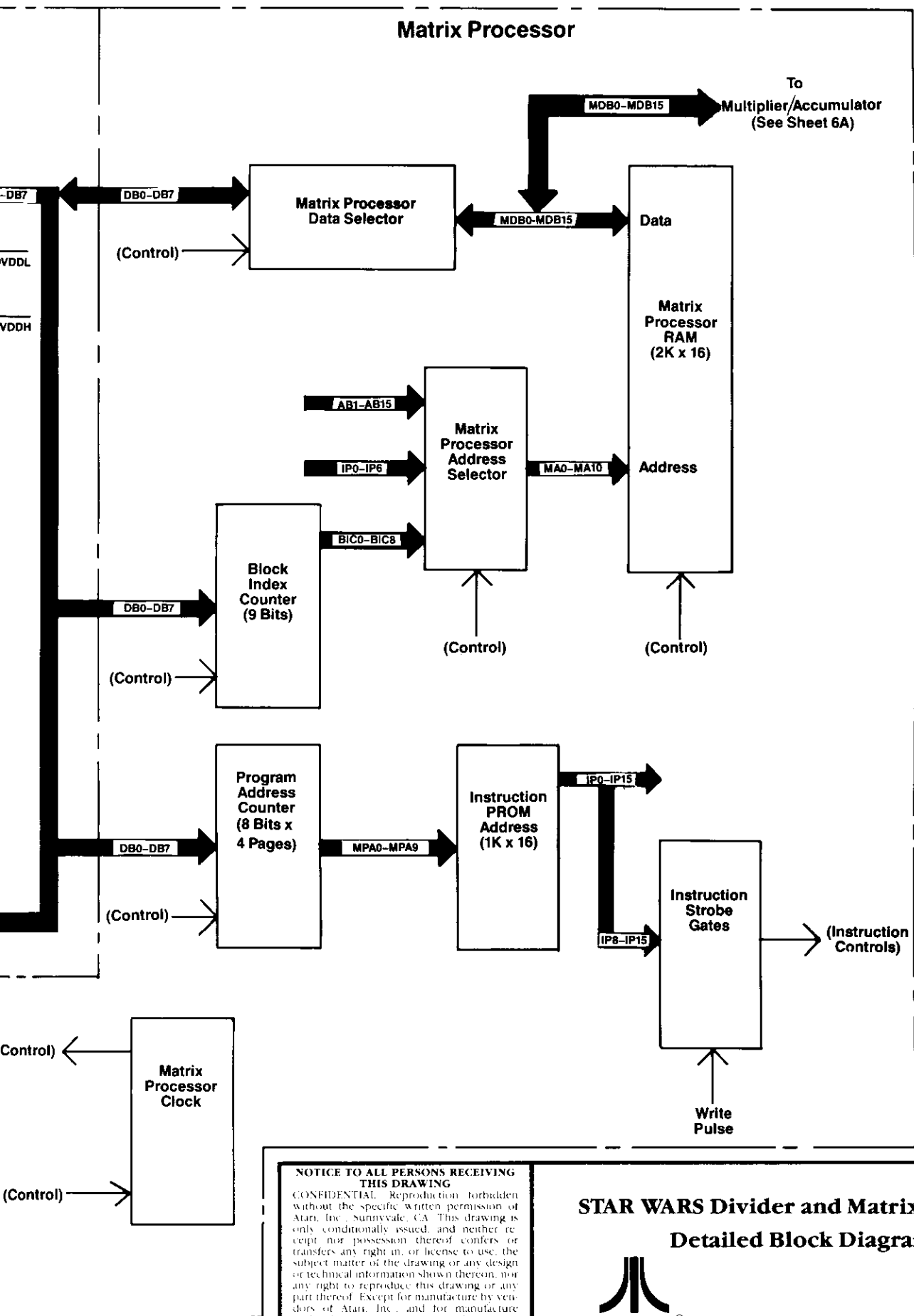


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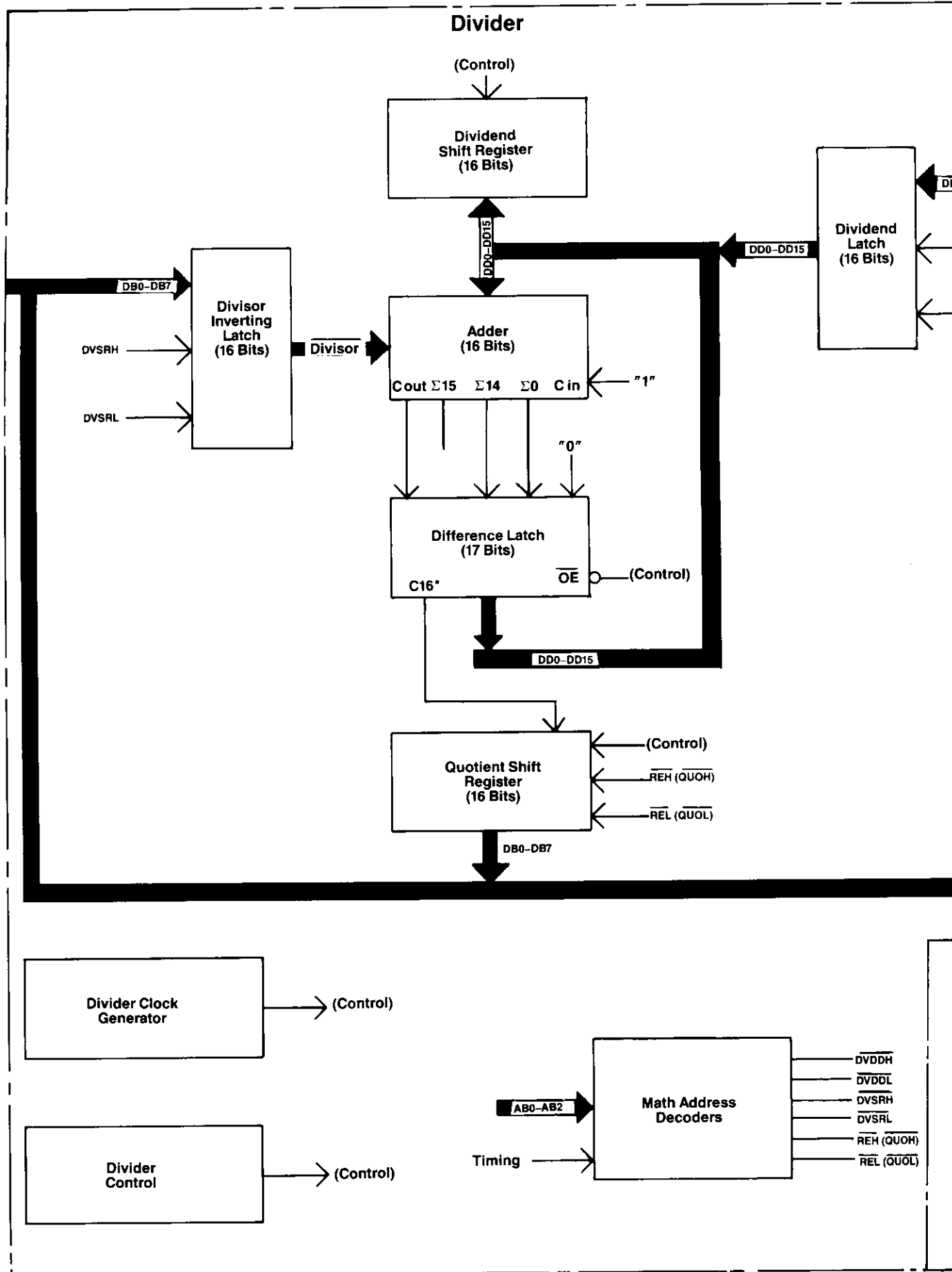
**STAR WARS Divider and Matrix Processor
Detailed Block Diagrams**



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READ/ WRITE	DATA BUS SIGNAL LINES D7 D6 D5 D4 D3 D2 D1 D0								FUNCTION
R/W	D	D	D	D	D	D	D	D	VRAM0
R/W	D	D	D	D	D	D	D	D	VRAM1
R/W	D	D	D	D	D	D	D	D	VRAM2
R/W	D	D	D	D	D	D	D	D	VRAM3
R/W	D	D	D	D	D	D	D	D	VRAM4
R/W	D	D	D	D	D	D	D	D	VRAM5
R	D	D	D	D	D	D	D	D	VROM
R	D								LEFT F/S
R		D							RIGHT F/S
R			D						SPARE 1
R				D					SELF-TEST
R					D				SLAM
R						D			COIN AUX
R							D		COIN L
R								D	COIN R
R	D								MATH RUN
R		D							VGHALT
R			D						LEFT THUMB
R				D					RIGHT THUMB
R					D				SPARE 2
R						D			DIAGN
R							D		Unused
R								D	Unused
R	D	D	D	D	D	D	D	D	OPT 0
R	D	D	D	D	D	D	D	D	OPT 1
R	D	D	D	D	D	D	D	D	ADC
R	D	D	D	D	D	D	D	D	MAINREAD
W	D	D	D	D	D	D	D	D	MAINWR
R	D								MAIN READY FLAG
R		D							SOUND READY FLAG
R/W					D	D	D	D	NOVRAM

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STAR WARS Memory Map -part 1



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HEXA- DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES															
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0000-07FF	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A
0800-0FFF	0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A
1000-17FF	0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	A
1800-1FFF	0	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A
2000-27FF	0	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A
2800-2FFF	0	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A
3000-3FFF	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A
4300	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
4320	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
4340	0	1	0	0	0	0	1	1	0	1	0					
4360	0	1	0	0	0	0	1	1	0	1	1					
4380	0	1	0	0	0	0	1	1	1	0	0					
4400	0	1	0	0	0	1	0	0								0
	0	1	0	0	0	1	0	0								0
4401	0	1	0	0	0	1	0	0								1
	0	1	0	0	0	1	0	0								1
4500-45FF	0	1	0	0	0	1	0	1	A	A	A	A	A	A	A	A

READ/ WRITE	DATA BUS SIGNAL LINES D7 D6 D5 D4 D3 D2 D1 D0								FUNCTION
W									$\overline{\text{EVGGO}}$
W									$\overline{\text{EVGRES}}$
W									$\overline{\text{WDCLR}}$
W									$\overline{\text{IRQCLR}}$
W	D								$\overline{\text{COIN CNTR 2}}$
W	D								$\overline{\text{COIN CNTR 1}}$
W	D								$\overline{\text{LED 3}}$
W	D								$\overline{\text{LED 2}}$
W	D								SASS
W	D								$\overline{\text{PRNGCLR}}$
W	D								$\overline{\text{LED 1}}$
W	D								$\overline{\text{RECALL}}$
W									$\overline{\text{NSTORE}}$
W									$\overline{\text{ADCSTART 0}}$
W									$\overline{\text{ADCSTART 1}}$
W									$\overline{\text{ADCSTART 2}}$
W									$\overline{\text{SOUNDRST}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{REH}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{MW0}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{REL}}$
W								D	$\overline{\text{MW1}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{MW2}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{PRNG}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{DVSRL}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{DVSRL}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{DVDDH}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{DVDDL}}$
R/W	D	D	D	D	D	D	D	D	$\overline{\text{RAM}}$
R/W	D	D	D	D	D	D	D	D	$\overline{\text{MBRAM}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 0}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 1}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 2}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 3}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 4}}$

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STAR WARS Memory Map -part 2



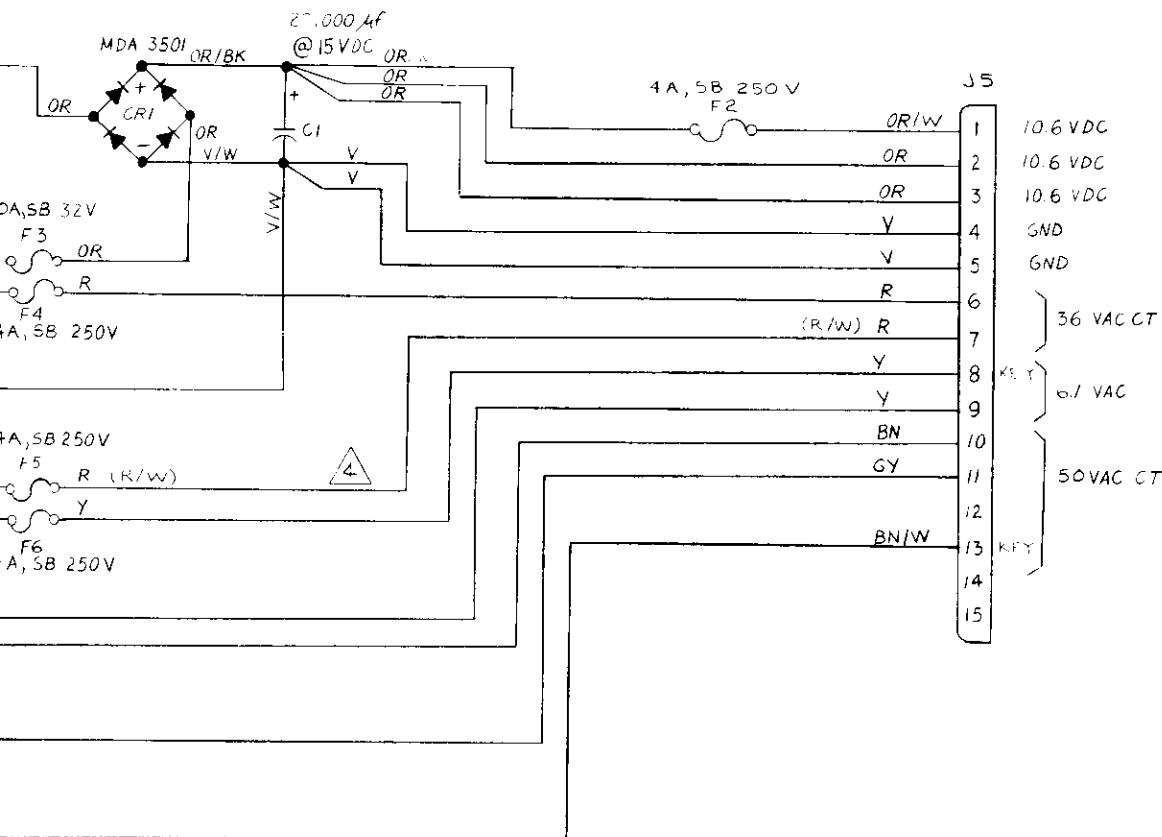
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1st printing

[illegible]

Color X-Y Power Supply Wiring Diagram



NOTES.

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND), & ONE WHITE WIRE (NEUTRAL).
2. USE 4 AMP 5B 250V FUSE AT F1 WITH 220 V & 240 V (EUROPEAN ONLY).
3. CONNECTOR J4B USED IN -04 THRU -06 VERSIONS OF A037396-XX ONLY.
4. ALTERNATE WIRE COLOR IS IN PARENTHESES.

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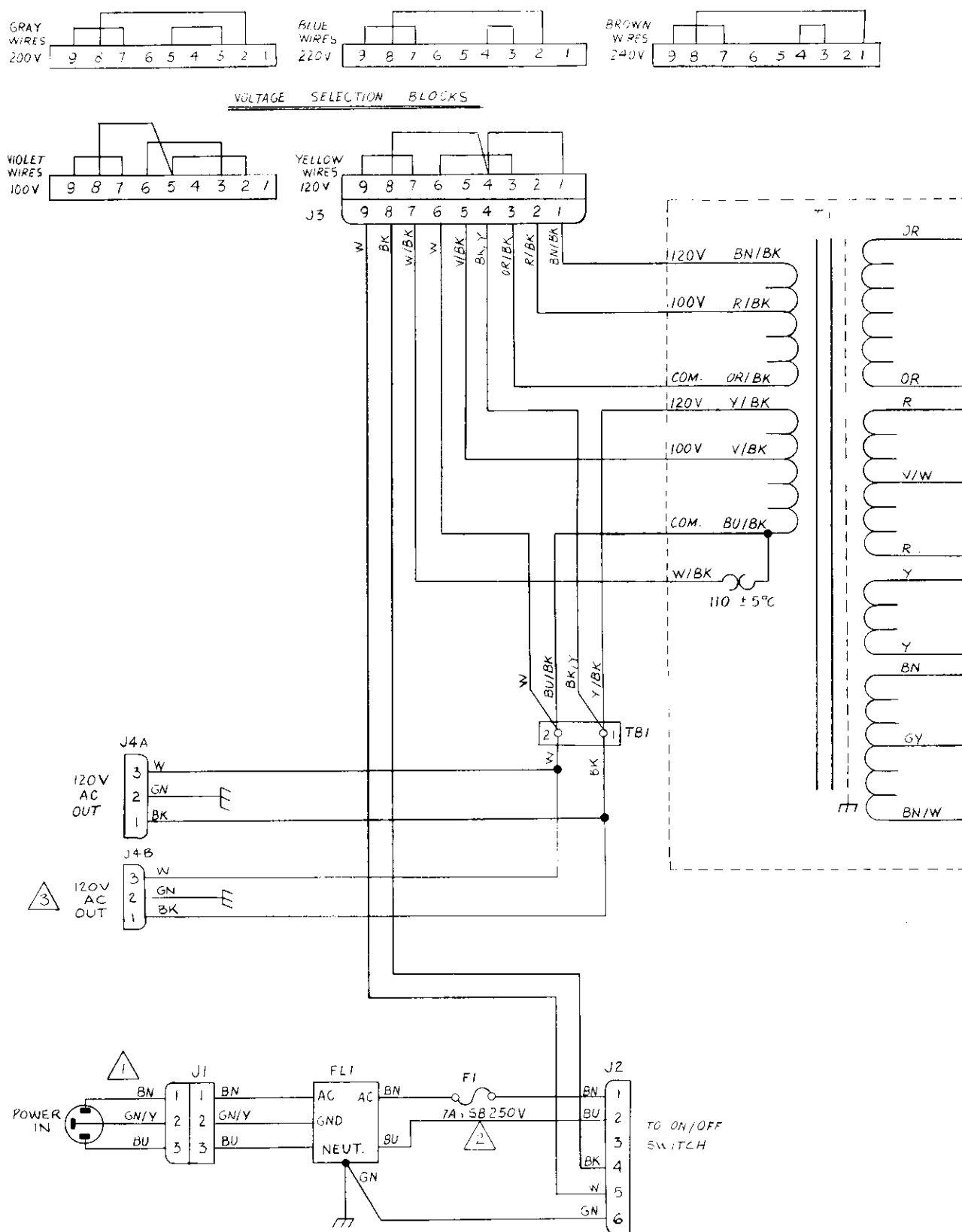
STAR WARS Color X-Y Power Supply Wiring Diagram



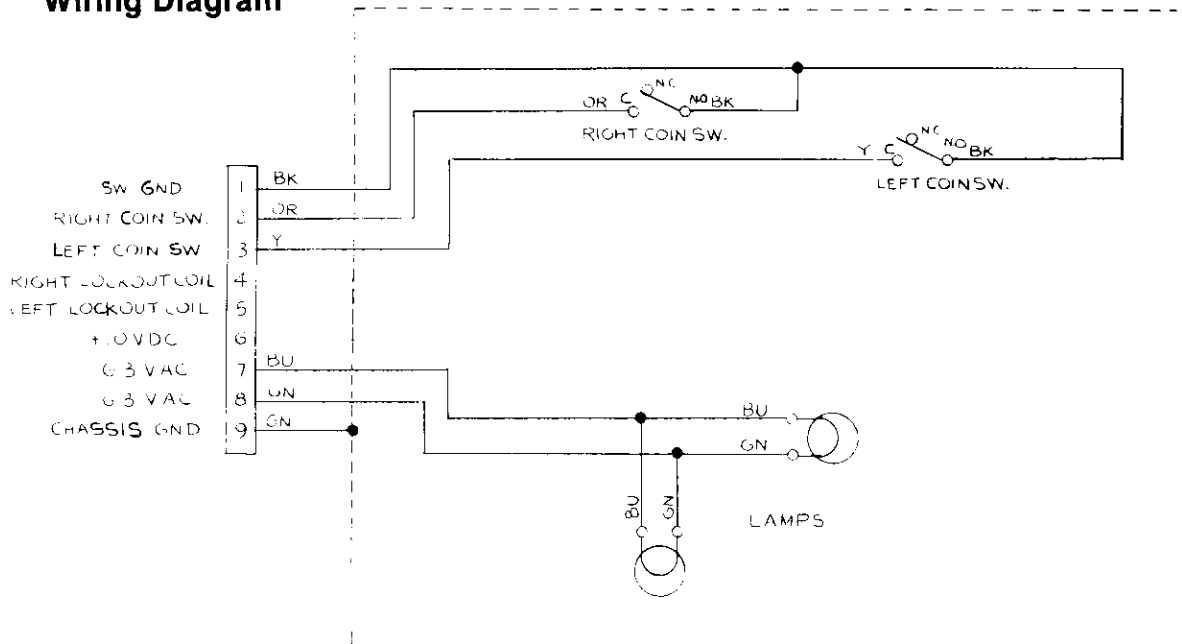
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Coin Door Wiring Diagram



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STAR WARS Game Interfaces

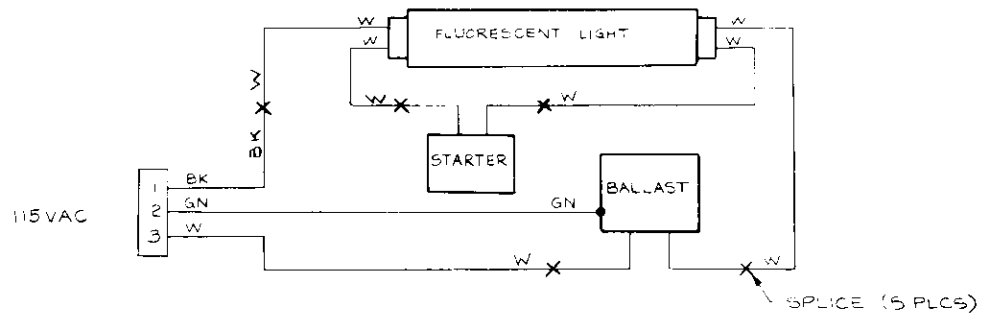


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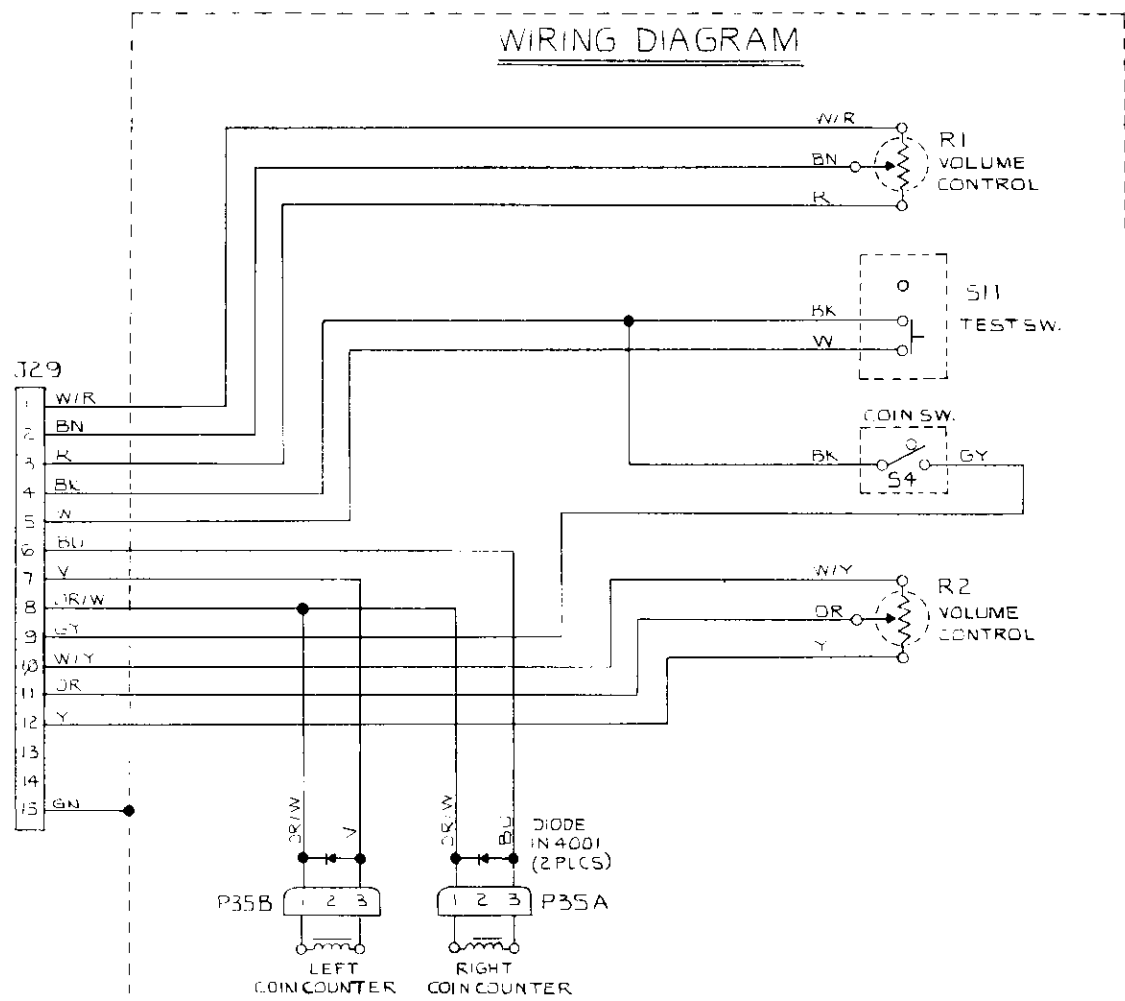
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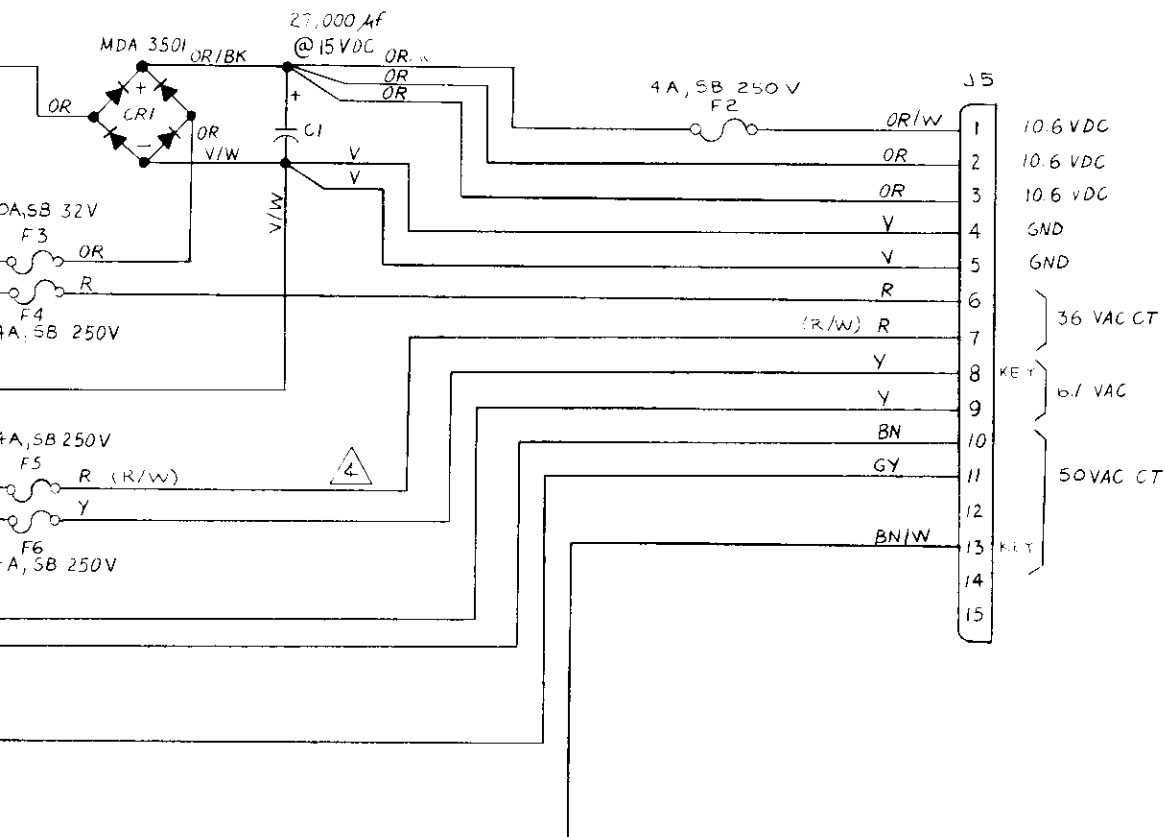
Fluorescent Light Wiring Diagram



Utility Panel Wiring Diagram



Color X-Y Power Supply Wiring Diagram



NOTES:

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND), & ONE WHITE WIRE (NEUTRAL).
2. USE 4 AMP SB 250V FUSE AT F1 WITH 220 V & 240 V (EUROPEAN ONLY).
3. CONNECTOR J48 USED IN -04 THRU -06 VERSIONS OF A037396-XX ONLY.
4. ALTERNATE WIRE COLOR IS IN PARENTHESES.

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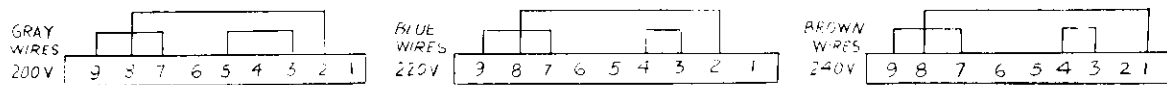
STAR WARS Color X-Y Power Supply Wiring Diagram



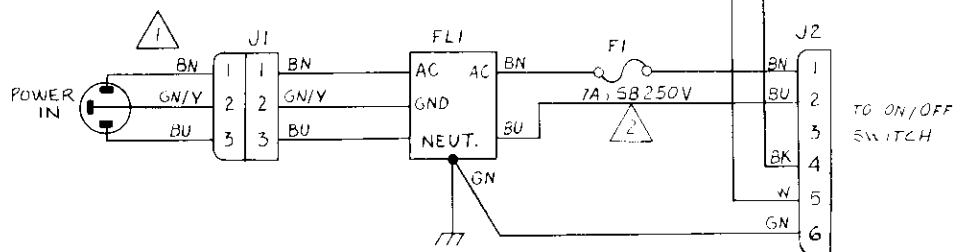
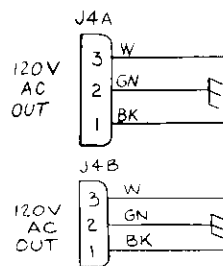
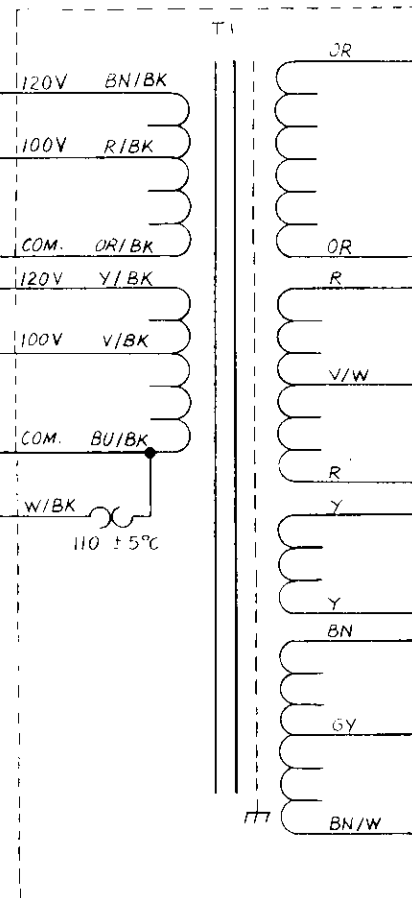
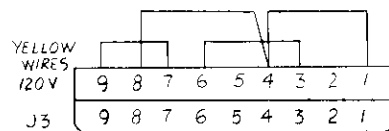
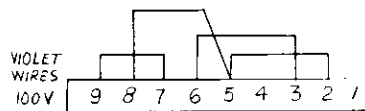
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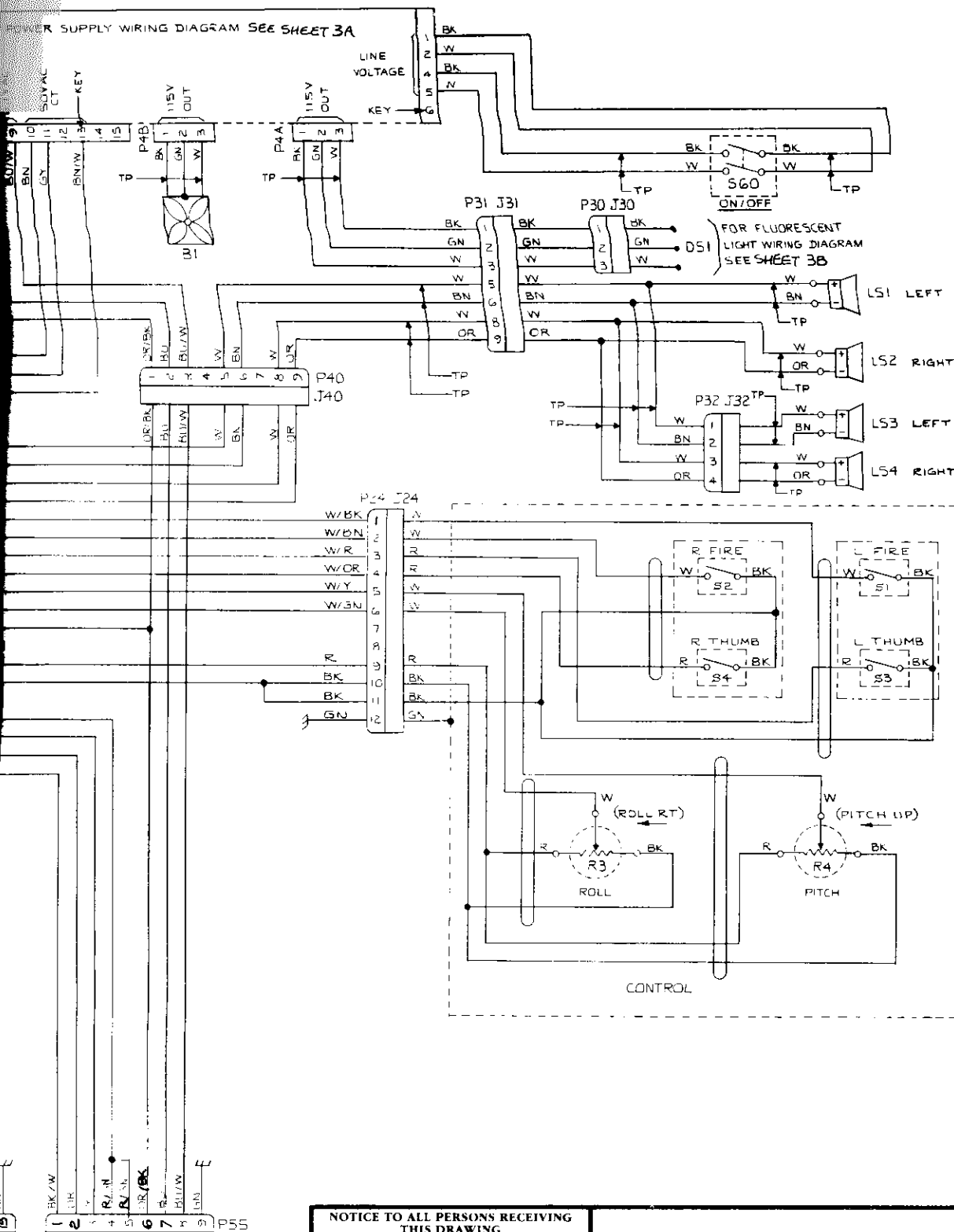
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VOLTAGE SELECTION BLOCKS



POWER SUPPLY WIRING DIAGRAM SEE SHEET 3A



FOR CON. DSR. WIRING DIAGRAM SEE SHEET 3B

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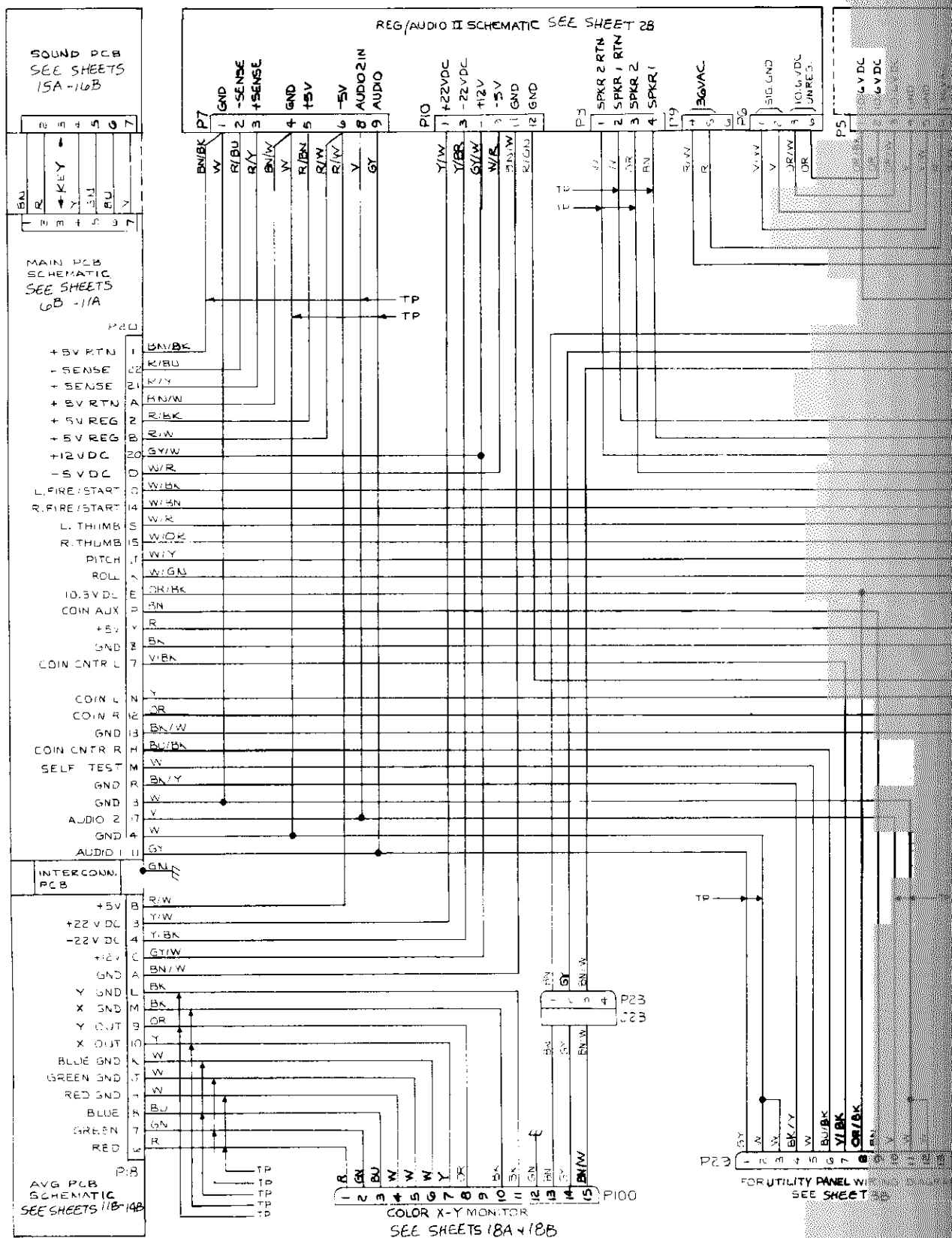
STAR WARS Cockpit Main Wiring Diagram



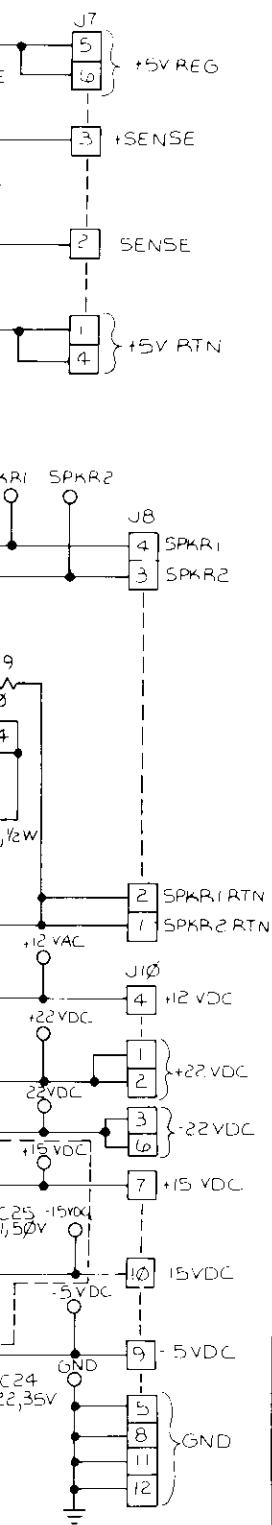
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Star Wars Regulator/Audio II PCB Schematic Diagram



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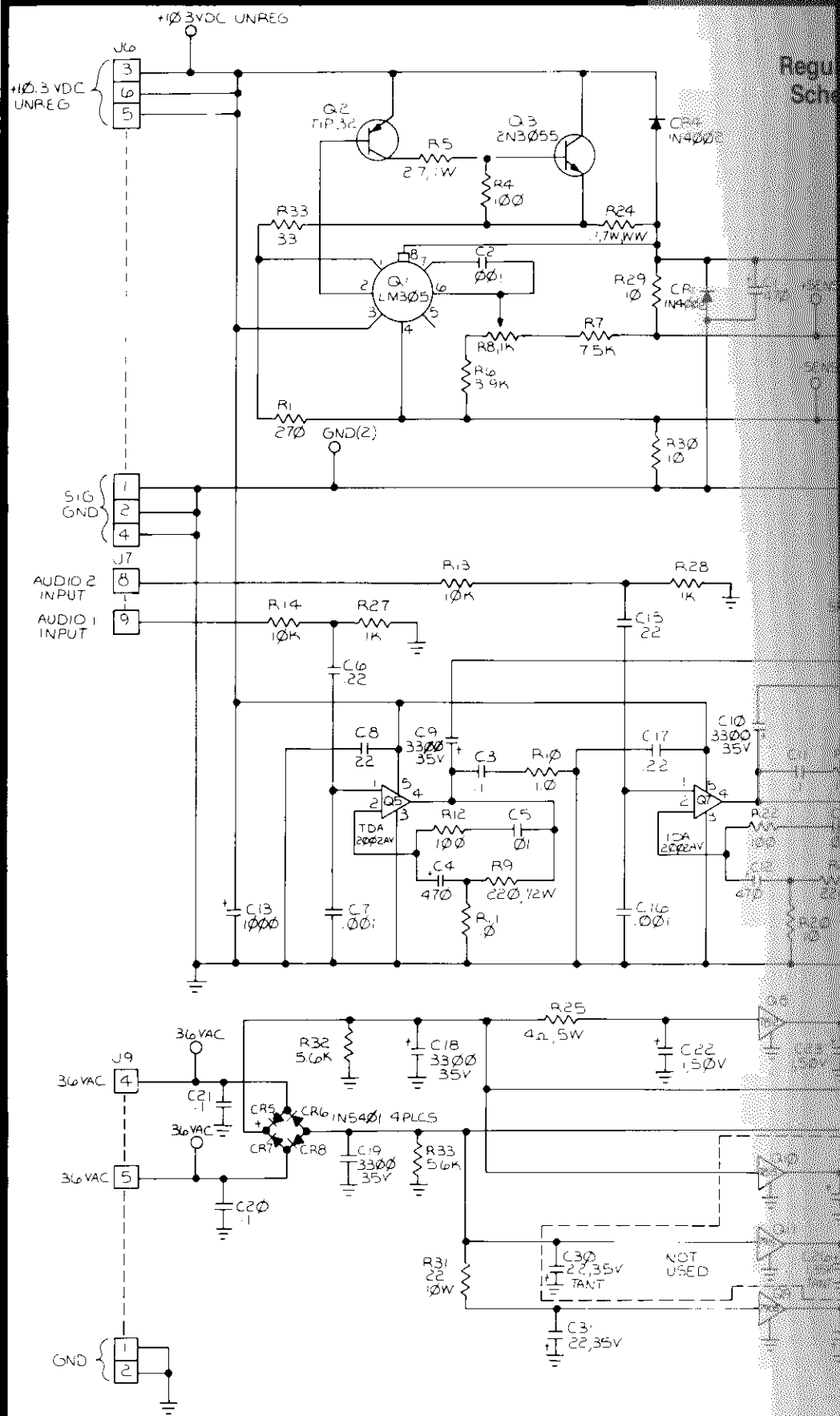
STAR WARS Regulator/Audio II PCB

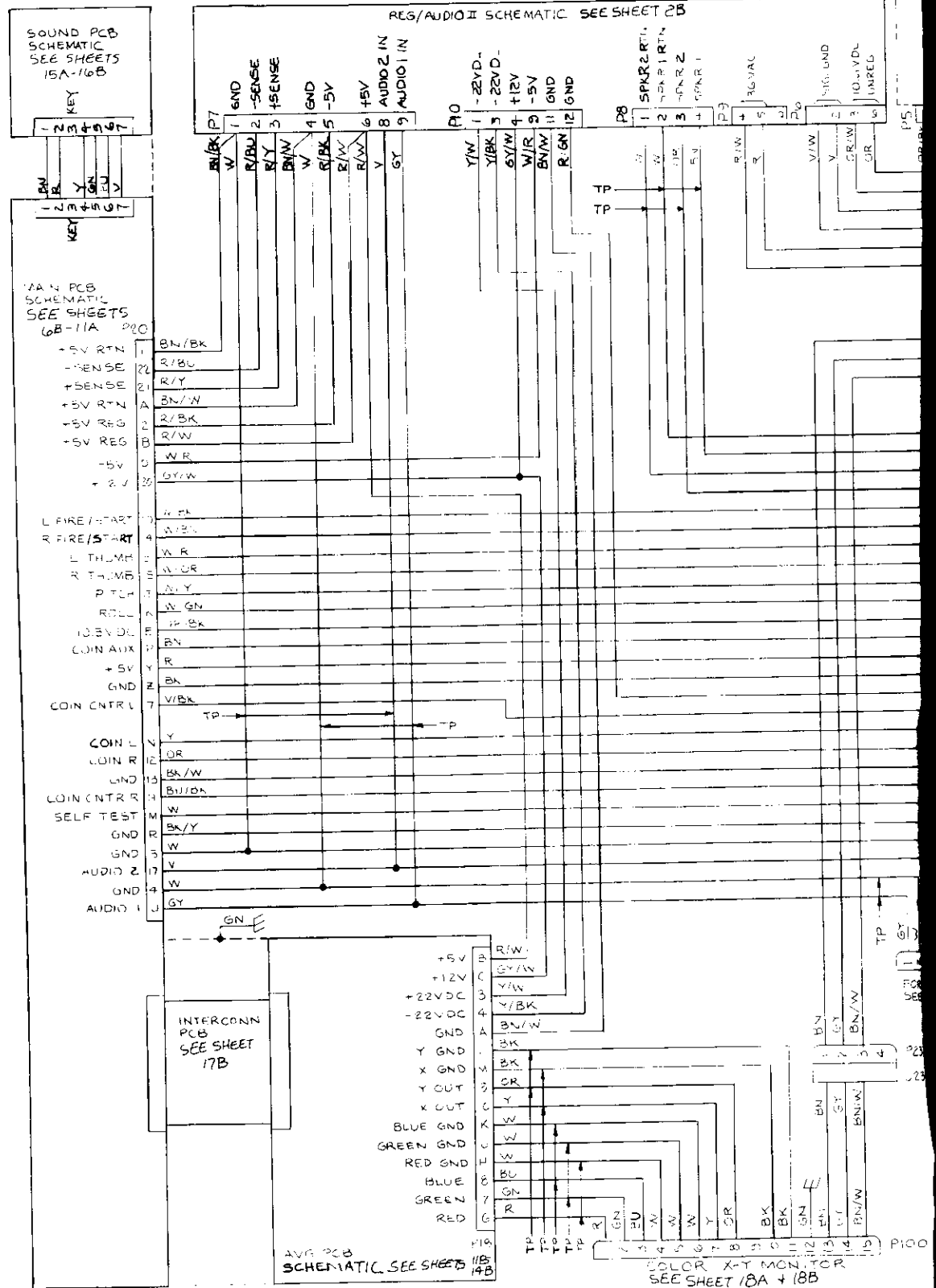


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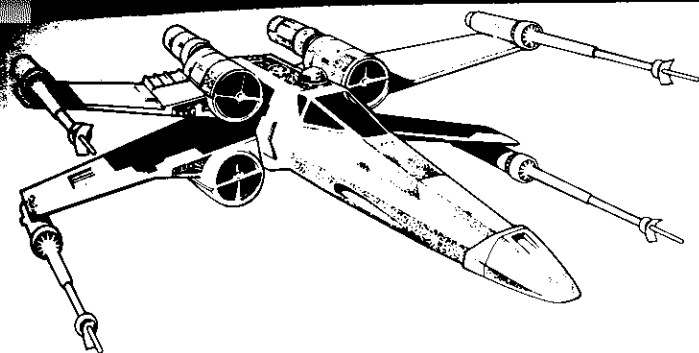


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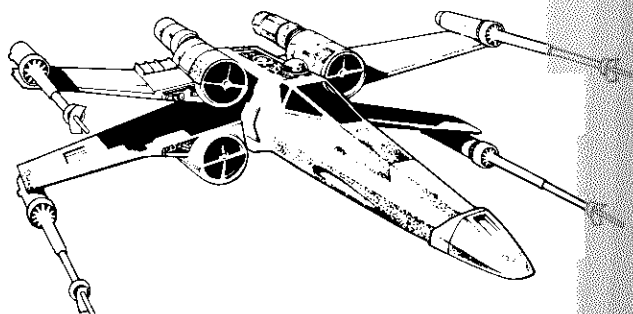
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Utility Panel Wiring Diagram (A039254-01 C)	
Fluorescent Light Wiring Diagram (035833-01 A)	
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STAR WARS Functional Block Diagram and Guide to PCB Schematics ..	Sheet 5A
STAR WARS Divider and Matrix Processor Detailed Block Diagram	Sheet 5B
STAR WARS Multiplier/Accumulator Detailed Block Diagram	Sheet 6A

Game PCB Schematics, Sheets 6B–17B

STAR WARS Main PCB	Sheet 6B–11A
STAR WARS Analog Vector-Generator PCB	Sheet 11B–14B
STAR WARS Sound PCB	Sheet 15A–16B
STAR WARS EMI Shield PCB	Sheet 17A
STAR WARS Interconnect PCB	Sheet 17B

Display Schematics, Sheets 18A–18B

STAR WARS Color X-Y High-Voltage PCB (201012-xx D)	Sheet 18A
STAR WARS Color X-Y Deflection PCB (201014-xx F)	Sheet 18B

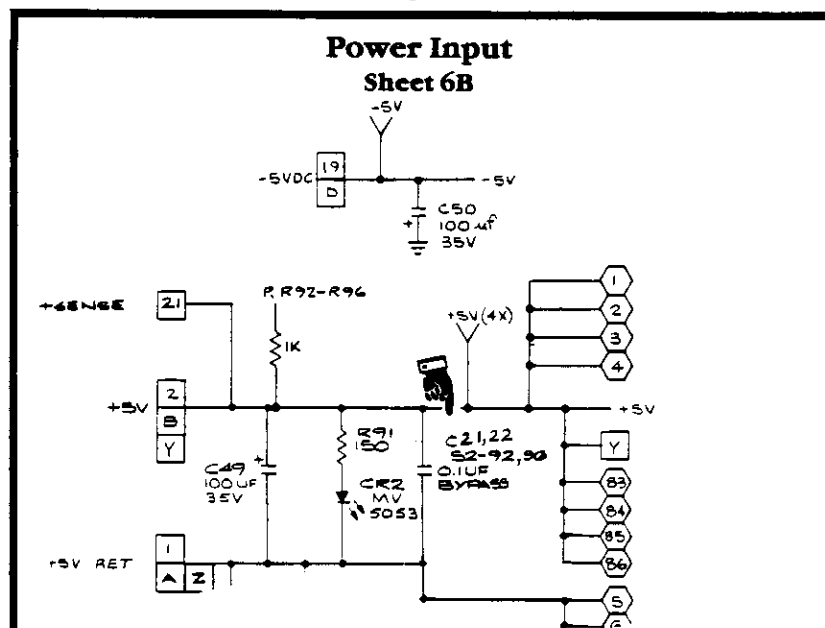


Supplement to

STAR WARS

STAR WARS Schematic Package (SP-225, 1st printing)
STAR WARS Operators Manual (TM-225, 1st printing)
STAR WARS Operators Manual (TM-245, 1st printing)

Please add the following correction to SP-225



Please make the following changes to the Main PCB parts list of TM-225 and/or TM-245:

STAR WARS Main PCB Parts List

Designator	Description	Part No.
Capacitors		
Add:		
C21, C22	0.1 µF, ±5%, 50 V Ceramic Capacitor	122002-104
Integrated Circuits		
1F	300 ns Tri-State EROM Integrated Circuit	136021-101
should be:		
1F	300 ns EPROM Integrated Circuit	136021-114

