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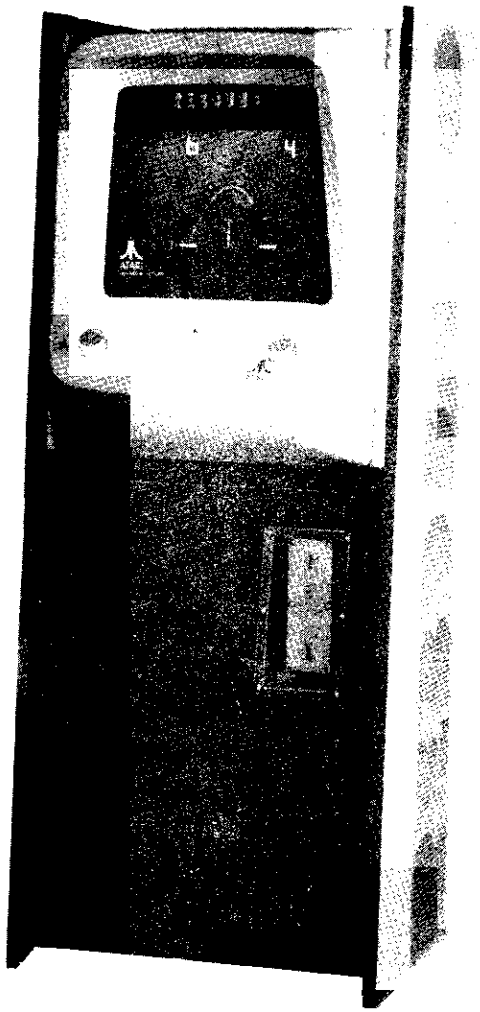
REBOUND



computer service manual

ATARI INC 14600 WINCHESTER BOULEVARD, LOS GATOS, CALIFORNIA 95030 • TELEPHONE (408) 374-2440 • TELEX 357-488

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1. GENERAL MAINTENANCE INFORMATION

1-1. INTRODUCTION

1-2. The Atari Rebound game consists of a cabinet, TV monitor, a printed circuit board (PCB) computer, interconnecting wiring, and various cabinet-mounted circuit components. Except for a schematic, no information about the TV monitor is presented in this manual. The TV monitor is a modified Motorola XM500 unit. TV circuit malfunctions can be solved using standard TV troubleshooting techniques. However, the PCB computer requires troubleshooting techniques that may be unfamiliar to the average technician. Therefore, the troubleshooting information in this manual is dedicated to the PCB computer and its associated cabinet circuitry.

1-3. TEST EQUIPMENT

1-4. In order to test any Atari PCB, some items such as the logic probe are absolutely essential. Others are desirable and will make the test procedure easier but are not absolutely essential. Some of these instruments are available from the Atari Customer Service Department and these are: the Atari Universal Test Fixture, the Kurz-Kasch 520 Logic Probe, the Atari Video Probe and the Hewlett-Packard 10529A Logic Comparator. Other instruments that are very useful are the HP 10526T Logic Pulser and the Tektronix 465 Oscilloscope. These items are available through your local electronics supply house.

1-5. **Required Minimum Equipment:** The following items are absolutely essential to perform the test procedures presented in this manual:

a. Atari Universal Test Fixture: The Atari Universal Test Fixture can be used to test the PCB computer assemblies for Pong, Pong Doubles, Super Pong, Rebound, Space Race, Gotcha, and Quadrapong. This test fixture is equipped with a 12 inch TV monitor, two 5 volt BNC connectors for use where a regulated 5 volt source is required, and all the controls necessary to operate the PCB computers. Connector cables must be ordered separately for each different type of PCB to be tested. The test fixture and cables are available only through the Atari Customer Service Department.

b. Logic Probe: The logic probe is an instrument designed for checking the outputs of integrated circuits. The Kurz-Kasch Logic Probe, Model No. LP-520, which is available through the Atari Customer Service Department or most large electronics supply houses, is recommended. This logic probe indicates if a signal is a logic high, logic low, or changing from one state to another. Consult the operating instructions included with the probe for further details about its operation. Logic probes received from the Atari Customer Service Department are specially modified to be compatible with the 5 volt BNC connector of the Atari Universal Test Fixture.

c. Video Probe: The video probe is a very simple but extremely useful device and consists of two test clips, a length of rubber-coated, test-lead wire, and a 4.7K, 1/4 watt carbon resistor. Video probes may be obtained free from the Atari Customer Service Department or, if necessary, they can be assembled from standard components available at all electronics supply houses. To use the video probe, attach one clip to the negative (-) side of the 10 uf video coupling capacitor found near position C9 on the PCB and clip the other end to the desired signal test points as indicated in the test procedures presented in this manual. The video probe allows the desired signal to be displayed on the TV monitor screen.

1-6. **Optional Equipment:** It is possible to find 90% of the possible PCB computer malfunctions without the following items. However, if a complete set of troubleshooting equipment is desired, Atari recommends:

a. Hewlett-Packard 10529A Logic Comparator: The Hewlett-Packard 10529A Logic Comparator is used to verify correct IC operation. This device simply clips onto in-circuit ICs and instantly displays any logic state difference between the in-circuit test IC and the reference IC in the comparator. Logic differences for each pin of a 14 or 16 dual in-line package are indicated by a lamp on the comparator. If the logic comparator is purchased from the Atari Customer Service Department, it is shipped with 20 preprogrammed reference PCBs. If the device is purchased elsewhere, these PCBs must be specially programmed.

b. Hewlett-Packard 10526T Logic Pulser: The Hewlett-Packard 10526T Logic Pulser is used to stimulate in-circuit ICs so that they are driven to

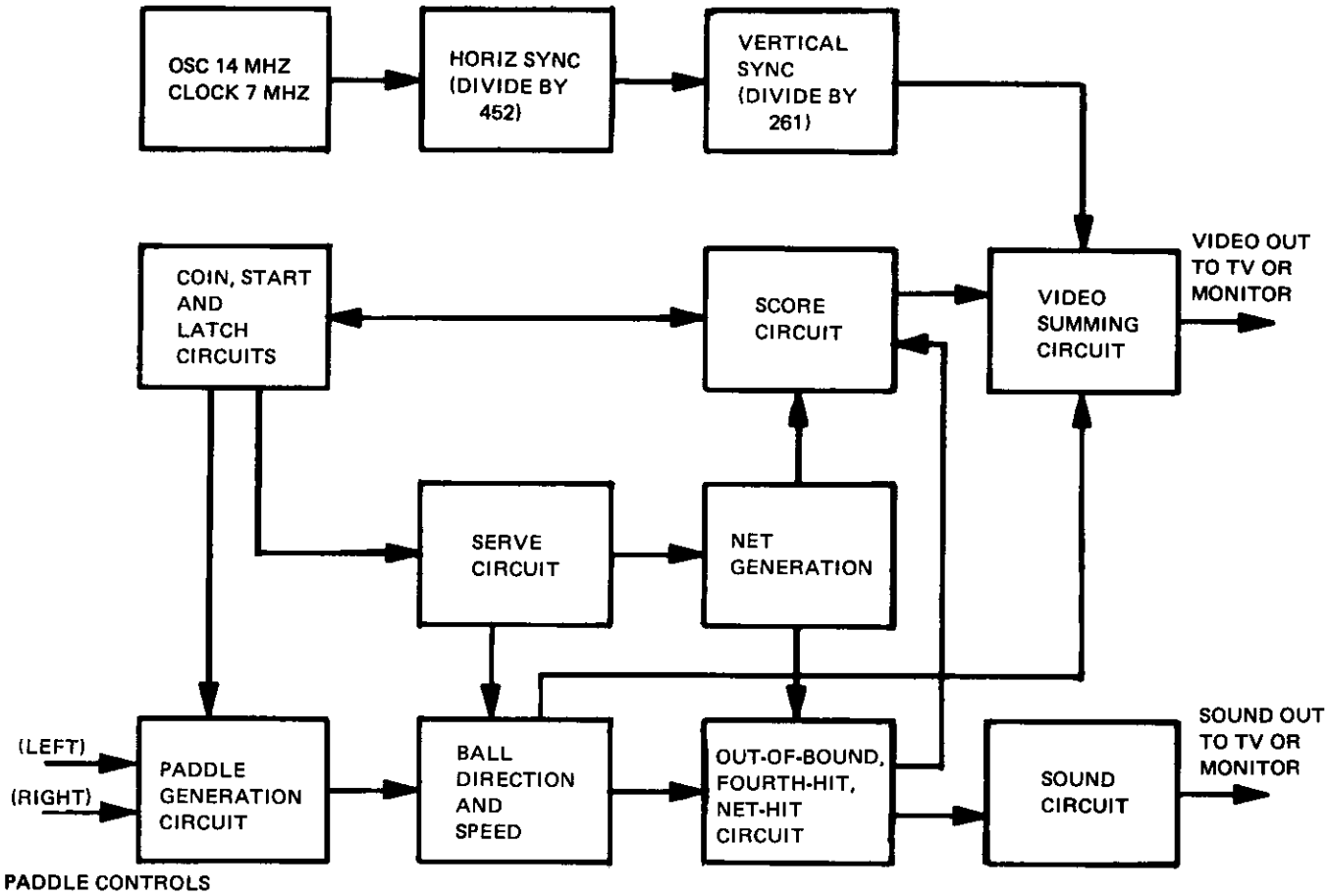


Figure 1-1. Rebound Block Diagram

their opposite states. This device is available from the Atari Customer Service Department or can be obtained from most large electronics supply houses.

c. Tektronix 465 Oscilloscope: The Tektronix 465 Oscilloscope is used for viewing various waveforms and should be ordered from Tektronix. Consult the manufacturer's operating instructions for details on oscilloscope operation.

1-7. GENERAL TROUBLESHOOTING APPROACH

1-8. The first step when troubleshooting malfunctions of the PCB computer is to relate the visible or audible malfunction to one or more circuits of the computer. For instance, if one of the paddle symbols is malfunctioning, study the text of the paddle circuit and then try to determine what might be causing the problem. Then, using schematics, the PCB component location diagram, and recommended test equipment, check out the paddle circuitry. Partial schematics of the computer are provided with each circuit description. Overall schematics of the computer and TV monitor, a cabinet wiring schematic, a component location diagram for the PCB computer, and a parts list are located at the rear of this manual.

1-9. BLOCK DIAGRAM DESCRIPTION

1-10. All circuitry of the computer is activated when the Rebound power cord is connected to a suitable source of ac power. Circuitry in the credit/start/electronic latch circuit automatically generates ATTRACT, $\overline{\text{ATTRACT}}$, START, and $\overline{\text{START}}$ signals. These signals are used by various cir-

cuits of the PCB computer to place the Rebound game in the attract mode.

1-11. Attract Mode: In the attract mode, the computer clock furnishes timing signals to various circuits of the computer. The horizontal sync and vertical sync circuits process a CLOCK signal, send timing signals to various circuits of the computer, and send horizontal sync and vertical sync signals to the TV monitor via the sync summing and video summing circuits. The paddle controls are defeated by the $\overline{\text{ATTRACT}}$ signal and the paddle circuit is forced to produce a horizontal bar across the bottom portion of the picture. Paddle data indicating what portion of the bar is being developed at any given time is continuously furnished to the ball direction and speed circuit.

1-12. The serve circuit is active during the attract mode and develops a ball symbol after the Rebound game is first energized. When the ball hits the horizontal bar at the bottom of the picture, the ball direction and speed circuit processes PADDLE DATA and BALL signals and develops HIT, $\overline{\text{HIT}}$, and motion data. The motion data is used by the horizontal and vertical ball motion circuits to develop ball velocity and direction signals. These signals are summed and furnished to various circuits of the computer. The BALL signal is also furnished to the TV monitor via the video summing circuit.

1-13. The net circuit is fully operative during the attract mode and produces a net symbol that increases in height after every second successful return of the ball across the net. However, due to the random movement of the ball during the attract mode, the ball is seldom returned more than twice before going out of bounds, hitting the net, or hitting the same point of the paddle bar four times in succession without being hit by the other paddle.

1-14. When the ball hits the net, goes out of bounds, or hits the left or right half of the paddle bar four times in succession, the out-of-bounds/fourth-hit/net-hit circuit sends a $\overline{\text{MISS}}$ signal to the sound circuit. The $\overline{\text{ATTRACT}}$ signal prevents the sound circuit from sending a SOUND OUT signal to the TV monitor when the ball hits the paddle bar or goes out of bounds, hits the net, or hits the left or right half of the paddle bar four times in succession. However, the sound circuit does send a $\overline{\text{SCORE SOUND}}$ signal to the serve circuit that causes another ball to be served.

1-15. The score circuit is partially inhibited by the START and $\overline{\text{START}}$ signals during the attract mode. Although the score of the last game is displayed on the TV screen, it is not changed when the ball goes out of bounds, hits the net, or hits the left or right half of the paddle bar four times in succession.

1-16. Play Mode: After a proper coin is inserted in the coin mechanism, the credit/start/electronic latch circuit lights the credit light and enables the start pushbutton. When ready, either player may press the start pushbutton, which causes the Rebound game to enter the play mode and a ball to be served.

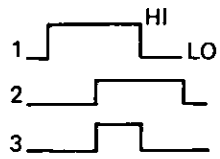
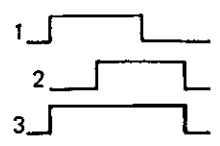
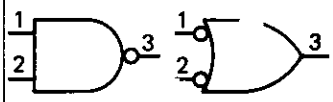
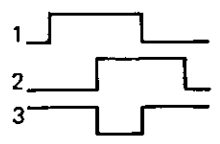
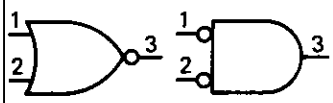
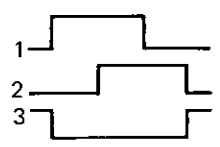
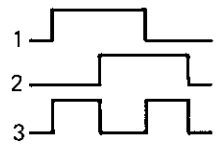
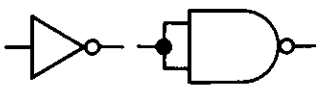
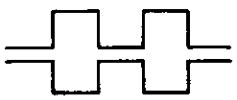
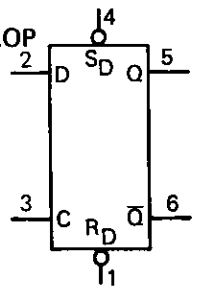
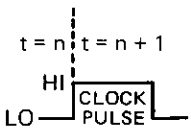
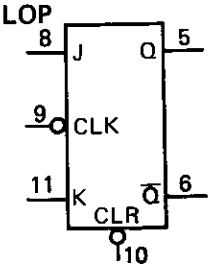
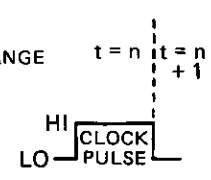
1-17. All circuits of the game are fully operational in the play mode. An ATTRACT signal causes the paddle circuit to enable the paddle controls and generate the left and right paddle symbols. Thus, the players can move the paddles horizontally to hit the ball. Each time the paddle hits the ball, a hit sound is generated. If the ball hits the left half of the left paddle or the right half of the right paddle, the ball rebounds to the left or right, respectively, at full speed. If the ball hits the center of either paddle, the ball is caused to move straight up and down. If the ball hits the right half of the left paddle or the left half of the right paddle, the ball is caused to be moved toward the opposite side of the net symbol at a speed and trajectory that is determined by where the ball hit the paddle.

1-18. If the ball hits the net, goes out of bounds, is missed by a paddle, or hits one paddle four times in succession, the score display is appropriately changed by the score circuit, a miss sound is generated, and another ball is served. Each time the ball is returned two times, the net is slightly increased in height. The net can be incremented ten times but is reduced to its minimum level each time the ball goes out of bounds, hits the net, is missed, or hits the same paddle four successive times. The game continues until one player accrues a score of 11 or 15, depending on how the game is programmed. At this point, the game reverts to the attract mode. If the game has been programmed for two plays per coin, a second game may be started by pressing the start pushbutton.

1-19. LOGIC SYMBOLOGY

1-20. Table 1-1 describes the operation of the most common logic circuits found on the computer board. Those not covered in the table are explained at their first appearance in the computer board circuit description in Section 2. Logic circuits are identified in the text and on the schematic by their actual grid location on the PCB and their output pin number, e.g., gate A6-3 would be the gate with output pin 3 in the logic package at location A6 on the PCB. The logic levels on the PCB are 0 to +0.4 volts for LO and +2.6 to +5 volts for HI. Signal names overscored (e.g., $\overline{\text{START}}$ and pronounced "start not") go LO to initiate events and those not overscored go HI when active. Overscored signals are always at the logic level opposite to that of their non-overscored counterparts, i.e., $\overline{\text{START}}$ is always at a logic level opposite to START.

Table 1-1. Logic Symbology

SYMBOL	TRUTH TABLE/TIMING	OPERATION
AND GATE 	1 2 | 3 LO LO | LO LO HI | LO HI LO | LO HI HI | HI 	Output is HI only when all inputs are HI, otherwise output is LO. Rule applies for any number of inputs.
OR GATE 	1 2 | 3 LO LO | LO LO HI | HI HI LO | HI HI HI | HI 	Output is HI when any input is HI. Output is LO only when all inputs are LO.
NAND GATE 	1 2 | 3 LO LO | HI LO HI | HI HI LO | HI HI HI | LO 	Output is LO only when all inputs are HI, otherwise output is HI.
NOR GATE 	1 2 | 3 LO LO | HI LO HI | LO HI LO | LO HI HI | LO 	Output is LO when any input is HI. Output is HI only when all inputs are LO.
EXCLUSIVE OR GATE 	1 2 | 3 LO LO | LO LO HI | HI HI LO | HI HI HI | LO 	Output is HI when either but not both inputs are HI, otherwise output is LO.
INVERTERS 	IN OUT 	The 2-input NAND or NOR gate can be used as inverters by tying one input to a fixed level or tying both inputs together.
D-TYPE FLIP-FLOP 	t = n t = n + 1 D Q | Q LO LO | LO LO HI | LO HI LO | HI HI HI | HI  Truth Table valid only when S_D and R_D are both HI	When both S_D (direct set) and R_D (direct reset) are HI, level at input D is transferred to output Q when input C (clock) goes HI. A LO on S_D forces $\overline{Q}$ HI and Q LO. A LO on R_D forces $\overline{Q}$ HI and Q LO. S_D and R_D predominate over all other inputs.
J-K MASTER SLAVE FLIP-FLOP 	t = n t = n + 1 J K CLK | Q $\overline{Q}$ LO LO – | NO CHANGE LO HI – | LO HI HI LO – | HI LO HI HI LO | HI LO HI HI HI | LO HI  Truth Table valid only when CLR is HI	When CLR is HI and: 1. J and K are both LO, clock pulse has no effect on outputs Q and $\overline{Q}$. 2. J and K are at opposite logic levels, negative-going clock edge transfers J level to Q and K level to $\overline{Q}$. 3. J and K are both HI, each negative-going clock edge alternates outputs Q and $\overline{Q}$. 4. LO on CLR forces and holds Q LO and $\overline{Q}$ HI

2. CIRCUIT DESCRIPTION

2-1. POWER SUPPLY

2-2. The power supply circuitry for the Rebound computer is shown in Figure 2-1. Input single-phase, 60 Hz, 115 vac power is routed through the front and rear interlocks, an ac line filter, and a 1A fuse to the primary of transformer T1. This transformer steps the input voltage down to 16.5 vac (under load), which is then applied to the rectifying, filtering, and regulating circuits of the computer.

2-3. The 16.5 vac output of T1 is full-wave rectified by diodes CR1 and CR2, and the pulsating dc output of these diodes is filtered by capacitor C28. A voltage regulator composed of integrated circuit LM309 or LM309K and resistor R4 receives the filtered dc voltage and provides a highly regulated +5 vdc output to the circuits of the computer. Resistor R4 increases the current capacity of the power supply. Capacitors C1 and C6 through C14 provide filtering for the +5 vdc bus.

2-4. COMPUTER CLOCK

2-5. Figure 2-2 shows the circuitry of the computer clock. Inverting amplifiers F9-12 and F9-2, resistors R5 and R6, capacitors C4 and C5, and crystal X1 form the oscillator portion of the clock circuit. Crystal X1 is in the feedback circuit of the oscillator and functions as a 14.3181 MHz narrow-band filter. Thus, the oscillator circuit is forced to oscillate at a frequency of 14.3181 MHz. The 14.3181 MHz signal taken from the output of amplifier F9-12 is routed through inverter F9-10 to the input of flip-flop J4-5/6. This flip-flop divides the input signal by 2 and delivers 7.159 MHz CLOCK and $\overline{\text{CLOCK}}$ signals to the logic circuits of the computer.

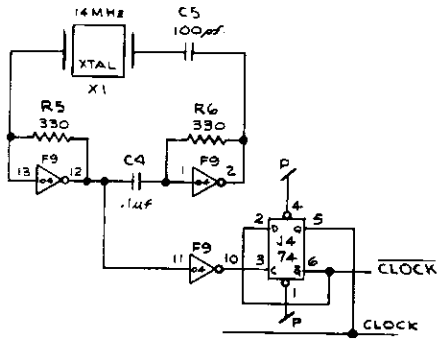


Figure 2-2. Computer Clock

2-6. HORIZONTAL SYNC CIRCUITRY

2-7. Horizontal sync for the TV monitor and timing signals for various circuits of the computer are supplied by the circuitry shown in Figure 2-3. This circuitry is composed of a counter circuit (H5, F5, and H4); NAND gates F4-6, K4-3, and K4-11; AND gate F7-3; inverter D4-4; and flip-flops J4-9/8, K5-5/6, and K5-9/8. The counter receives the 7.159 MHz CLOCK signal from the computer clock and produces numerous submultiples of the CLOCK signal that are designated 1H, 2H, 4H, 8H, 16H, 32H, 64H, 128H, 256H, and $\overline{256H}$. These submultiples are distributed to various logic circuits of the computer for timing and signal development purposes. The development of the H SYNC, $\overline{\text{H SYNC}}$, H BLANK, $\overline{\text{H BLANK}}$, H RESET, and $\overline{\text{H RESET}}$ signals is discussed in the following paragraphs. Development and timing of other signals related to the submultiples of the CLOCK signal are discussed in other portions of this manual.

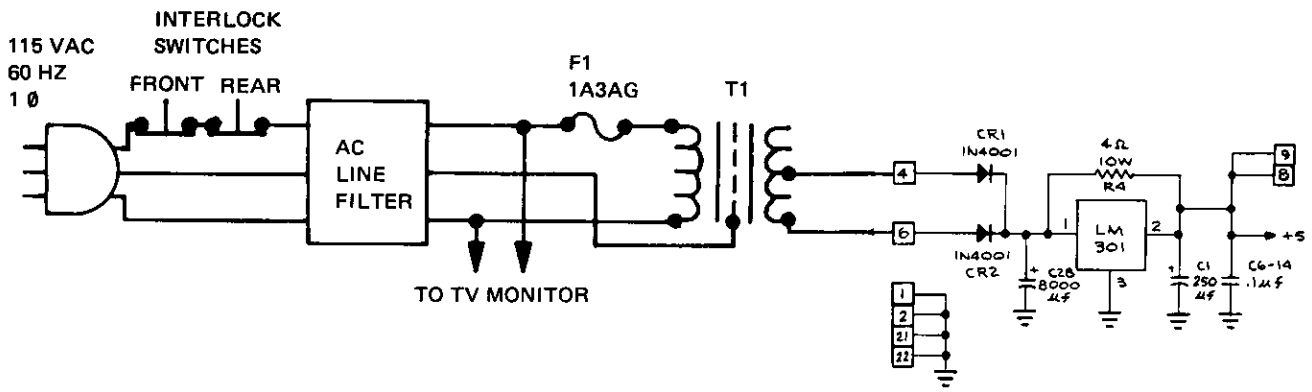


Figure 2-1. Power Supply

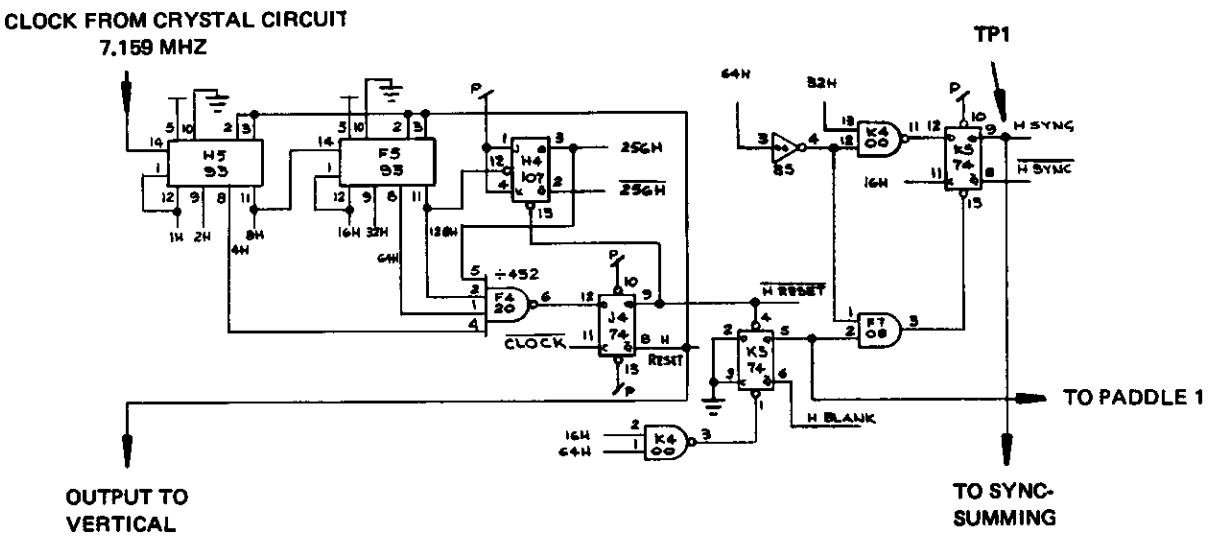


Figure 2-3. Horizontal Sync and Blanking Circuitry

2-8. Each TV line of the Rebound game is approximately 63 usec long, which is equivalent to the time it takes the counter to count 453 CLOCK pulses after being reset. At the count of 452, the 256H, 128H, and 4H signals are all high. As a result, the output of NAND gate F4-6 goes low. When the next $\overline{\text{CLOCK}}$ pulse occurs, the Q output of flip-flop J4-9/8 goes low and the $\overline{Q}$ output goes high. The Q output is used to reset flip-flop H4-3/2 of the counter, to set flip-flop K5-5/6, and for other signal development purposes on the computer. The $\overline{Q}$ output of J4-9/8 is used to reset counters H5 and F5 and is also sent to the vertical sync circuitry.

2-9. Setting flip-flop K5-5/6 causes the $\overline{Q}$ output to go low, which establishes the leading edge of the $\overline{\text{H BLANK}}$ pulse, and the Q output to go high, which establishes the leading edge of the H BLANK pulse. The H BLANK pulse is sent to the paddle logic and to AND gate F7-3. Before the count 64H is reached, the output of inverter B5-4 is high. Therefore, the output of AND gate F7-3 is high. Signals 16H and 32H are both high at the count of 48. Consequently, the output of NAND gate K4-11 goes low, and the clock input (pin 11) of flip-flop K5-9/8 is enabled. With a low applied to pin K5-12 and highs applied to pins K5-10, K5-11, and K5-13 of flip-flop K5-9/8, the Q output of the flip-flop goes low, which forms the leading edge of the H SYNC pulse, and the $\overline{Q}$ output goes high, which forms the leading edge of the $\overline{\text{H SYNC}}$ pulse. At the count of 64, the 64H signal goes high, causing flip-flop K5-9/8 to change states and form the trailing edge of the H SYNC and $\overline{\text{H SYNC}}$ pulses. At the count of 80, the 16H and 64H signals are high, causing a low to be applied to the clear input (pin 1) of flip-flop K5-5/6. As a result, the flip-flop changes state and thereby forms the trailing edges of the H BLANK and $\overline{\text{H BLANK}}$ signals. The $\overline{\text{H SYNC}}$ and $\overline{\text{H BLANK}}$ are both used by other circuits of the computer, and the H SYNC signal is used by circuits of the computer and is sent to the TV monitor via the sync summing and video summing circuits.

2-10. VERTICAL SYNC CIRCUITRY

2-11. Vertical sync for the TV monitor and signal development and timing signals for various circuits of the computer are supplied by the vertical sync circuitry, which is shown in Figure 2-4. The vertical sync circuitry is composed of a counter circuit (J3, H3, and H4), NAND gates H2-12 and H2-6, and flip-flops J2-9/8 and H1-3/11. During operation, the counter receives the H RESET signal from the horizontal sync circuitry and produces numerous submultiples of the H RESET signal that are designated 1V, 2V, 4V, 8V, 16V, 32V, 64V, 128V, 256V, and $\overline{\text{256V}}$. These submultiples are distributed to various logic circuits of the computer for timing and signal development purposes. The development of the $\overline{\text{V RESET}}$, V RESET, and $\overline{\text{V SYNC}}$ signals is discussed in the following paragraphs. Development and timing of other signals related to the submultiples of the H RESET signal are discussed in other portions of the manual.

2-12. It requires 1/60.08 second to develop one field of the TV picture for the Rebound game, which is the time it takes the counter to count 262 H RESET pulses after being reset. At the count of 261, the 256V, 4V, and 1V signals are all high. As a result, the output of NAND gate H2-12 goes low. When the next H RESET pulse occurs, the Q output ($\overline{\text{V RESET}}$) of flip-flop J2-9/8 goes low and the $\overline{Q}$ out-

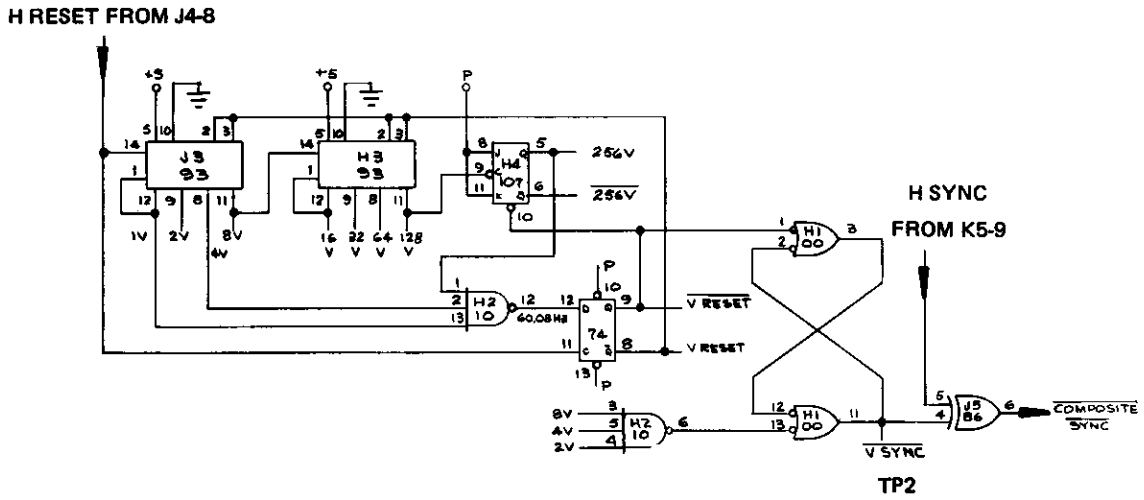


Figure 2-4. Vertical Sync and Sync Summing Circuitry

put (V RESET) goes high. The Q output is used to reset flip-flop H4 of the counter, to set flip-flop H1-3/11, and for other timing and signal development purposes on the computer. The $\overline{Q}$ output is used to reset counters J3 and H3 and is also used for other timing and signal development purposes on the computer.

2-13. Setting flip-flop H1-3/11 causes the output at pin H1-11 to go low, which forms the leading edge of the $\overline{\text{V SYNC}}$ pulse. Fourteen H RESET pulses later, signals 8V, 4V, and 2V are all high. Consequently, the output of NAND gate H2-6 goes low, which resets flip-flop H1-3/11. Resetting flip-flop H1-3/11 forms the trailing edge of the $\overline{\text{V SYNC}}$ pulse, which is sent to sync summing gate J5-6 and to other circuits of the computer for signal timing and developmental purposes.

2-14. SYNC SUMMING

2-15. Exclusive OR gate J5-6 (shown in Figure 2-4) is used for sync summing. H SYNC pulses are applied to pin 5 of this gate, and $\overline{\text{V SYNC}}$ pulses are applied to pin 4. The logic of the exclusive OR gate causes the $\overline{\text{V SYNC}}$ pulse to be serrated by the H SYNC pulses. Serrating the $\overline{\text{V SYNC}}$ pulse keeps the horizontal oscillator of the TV monitor synchronized during vertical retrace. The output of the exclusive OR gate is sent to the video summing circuit and consists of a serrated vertical sync pulse (containing 14 serrations) followed by 248 horizontal sync pulses. Therefore, one field of the TV picture consists of 248 viewable lines. Since no interlace provisions are incorporated into the circuitry of the computer, successive fields are laid approximately on top of one another, resulting in a picture frame that contains approximately 248 lines. This frame is repeated 30.04 times per second.

2-16. ELECTRONIC LATCH CIRCUIT

2-17. The electronic latch circuit is shown in Figure 2-5 and consists of transistors Q1, Q2, and Q3 and associated circuitry, inverter E9-4, and an antenna. The antenna is mounted within the Rebound cabinet; all other components of the electronic latch circuit are mounted on the computer board. The latch circuit has four functions, which are described in the following paragraphs.

2-18. The first function of the latch circuit is to initialize (Q high) flip-flop D8-9/8 of the one/two-play circuit and flip-flop E8-5/6 of the start circuit when power is first turned on. This function results from the fact that the latch circuit stabilizes with the collector of transistor Q3 at a high state after power is turned on. This high is inverted by E9-4 and used to preset the Q outputs of flip-flops D8-9/8 and E8-5/6 to a high level. Presetting these two flip-flops disables the start circuitry and places the Rebound game in the attract mode. which is discussed in another section of this manual.

2-19. The second function of the latch circuit is to furnish enabling levels to the preset inputs of flip-flops D8-9/8 and E8-5/6 when the credit circuit has determined that a proper coin has been deposited. As described in the text of the credit circuitry, flip-flop E8-8 produces a negative-going pulse when a proper coin is deposited. This pulse is routed through diode CR8 and resistor R14 to the base of transistor Q2, turning on the transistor. Providing transistor Q1 is

not turned on by the antenna circuit (discussed in the next paragraph), the high developed at the collector of Q2 turns on transistor Q3. Turning on Q3 latches transistors Q2 and Q3 in the on state, which perpetuates the high levels applied to the preset inputs of flip-flops D8-9/8 and E8-5/6.

2-20. The credit and start circuitry is sensitive to any accidental or player-produced static charges. If not offset, these charges can enable the start circuitry. To offset static charges, a static suppression circuit is incorporated into the circuitry of the Rebound game. This circuit consists of an antenna within the Rebound cabinet, and diode CR7 and transistor Q1 on the computer board. When static charges are sensed by the antenna, a positive level is impressed at the base of transistor Q1, turning on Q1. Turning on Q1 turns off transistor Q3, which causes the start circuit to be inhibited and the attract mode to be enabled as previously described.

2-21. The fourth function of the electronic latch circuit is to furnish a low preset level to flip-flops D8-9/8 and E8-5/6 at the end of one or two games, as determined by the two-play/one-play circuit. When the two-play/one-play circuit senses that game credit has expired, the output of NAND gate D7-3 is forced low. This low is routed through diode CR6 to the base of transistor Q3, turning it off. Turning off Q3 unlatches the electronic latch circuit, causing a low to be furnished to flip-flops D8-9/8 and E8-5/6 via inverter E9-4. This low is used to place the Rebound game in the attract mode and inhibit the start circuitry.

2-22. CREDIT CIRCUIT

2-23. The credit circuit is shown in Figure 2-5. This circuit consists of the coin deposit mechanism; diodes CR3 and CR4; capacitors C17, C18, C19, and C20; resistors R7, R12, and R13; timer D9; inverters E9-8 and E9-6; flip-flops E9-10/12, E8-8, D8-5, and D8-9/8; NAND gate D7-3; NOR gate C8-1; a light emitting diode (LED); and the 2P/1P switch. Except for the LED and coin mechanism, all of the foregoing components are located on the computer board. The LED (credit light) and coin mechanism are located on the front panels of the Rebound cabinet.

2-24. During the time a proper coin is being deposited, a microswitch in the coin deposit mechanism is actuated. Actuating the microswitch produces a negative-going pulse that is applied to a coil of a coin counter and, via diode CR3, to pin 13 of flip-flop E9-10/12, setting the flip-flop. This flip-flop is used to prevent transients produced by bouncing contacts of the microswitch from disturbing the circuits of the computer. The low produced at pin 10 of this flip-flop inhibits part of the start circuit and triggers timer D9. At the same time, the high output at pin 12 of the flip-flop is applied to pin 2 of NOR gate C8-1 and to pins 12 and 13 of flip-flop E8-8. The timer delays the pulse from flip-flop E9-10/12 by 10 milliseconds and then applies it, via inverter E9-8, to flip-flop E8-8, triggering it. Delaying the triggering of flip-flop E8-8 by 10 milliseconds prevents the accidental or player-induced vibrations that might actuate the coin microswitch from triggering flip-flop E8-8 and eventually enabling the Rebound game.

2-25. The negative-going output of flip-flop E8-8 is sent to the electronic latch circuit and is also applied to the clear inputs of flip-flops D8-5 and D8-9/8. The resulting high from the electronic latch circuit and the low from flip-flop E8-8 cause the Q output of flip-flop D8-9/8 to go low. Flip-flop D8-5 is part of a two-play/one-play circuit and is discussed further in subsequent text. The low output of flip-flop D8-9/8 furnishes one enabling input to NOR gate C8-1 and disables NAND gate D7-3. An enabling high level for the start circuitry is taken from the $\overline{Q}$ output of flip-flop D8-9/8. This $\overline{Q}$ output is also inverted and used to forward bias the LED of the front panel credit indicator, which informs the game player that his coin has been accepted and he may start the game when ready.

2-26. After the coin has passed the microswitch, the switch returns to its normally closed position, which resets flip-flop E9-10/12. Resetting this flip-flop clears flip-flop E8-8, sends a high enabling level to the start circuitry, and enables NOR gate C8-1. Enabling NOR gate C8-1 causes another high enabling level to be sent to the start circuitry. Diode CR4 damps the inductive transient produced when the ground is removed from the coil of the coin counter. In addition, diode CR3 protects integrated circuit E9 from the positive-going inductive transients from the coin counter coil.

2-27. The two-play/one-play circuit is part of the credit circuit and consists of flip-flops D8-5 and D8-9/8, NAND gate D7-3, and the 2P/1P switch. This circuit allows the Rebound game to be set up to provide one game or two games for each coin accepted by the credit circuitry.

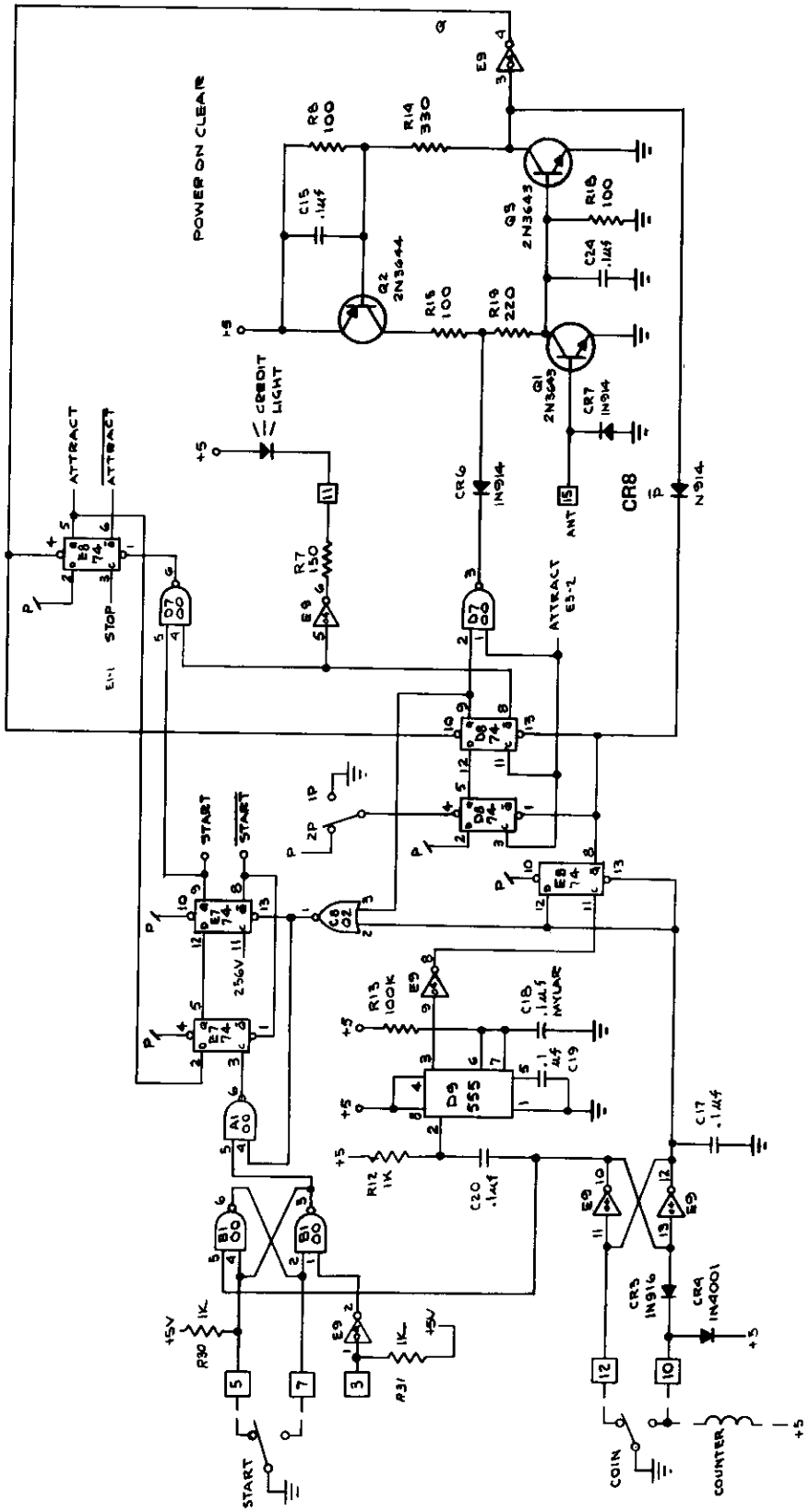


Figure 2-5. Credit, Start, and Electronic Latch Circuitry

2-28. For example, if the 2P/1P switch is set to 1P, a high is produced at the Q output of flip-flop D8-5. Therefore, when the game is over and the ATTRACT signal from flip-flop E8-5/6 goes high, the high output of flip-flop D8-5 is clocked to the Q output of flip-flop D8-9/8. This high Q output forces the output of NOR gate C8-1 to go low, which inhibits the start circuitry. In addition, the high Q output in combination with the high ATTRACT signal forces the output of NAND gate D7-3 low, which unlatches the electronic latch circuitry as described in the electronic latch text. The low $\overline{Q}$ output of flip-flop D8-9/8 turns off the credit light and also inhibits the start circuitry via NAND gate D7-6.

2-29. If the 2P/1P switch is set to 2P, a low is produced at the Q output of flip-flop D8-5 when the negative-going pulse from flip-flop E8-8 occurs. Consequently, when the game is over, the fixed high at the D input of flip-flop D8-5 is clocked to the Q output of this flip-flop, but no change occurs at the Q output of flip-flop D8-9/8. Therefore, the outputs of NOR gate C8-1 and NAND gate D7-3 remain high, allowing the start circuitry to remain enabled. When ready, the game player may press the start pushbutton to begin the second game. At the end of the second game, the high output of flip-flop D8-5 is clocked to the Q output of flip-flop D8-9/8 by the high ATTRACT signal. This high Q output, in combination with the low $\overline{Q}$ output and the high ATTRACT signal, inhibits the start circuitry as previously described.

2-30. START CIRCUIT

2-31. The start circuit is shown in Figure 2-5 and consists of inverter E9-2; flip-flops B1-6/3, E7-5, E7-9/8, E8-5/6; AND gate A1-6; NAND gate D7-6; and the start switch. The start pushbutton switch is located on the front panel of the Rebound game; all other components of the start circuit are located on the computer board.

2-32. Once the credit light is lit, the Rebound game is started by pressing the start pushbutton. Pressing and releasing the pushbutton sets and resets flip-flop B1-6/3, causing a positive-going pulse to be applied to pin 5 of NAND gate A1-6. Pin 4 of NAND gate A1-6 is high whenever game credit has been established by the credit circuit. Consequently, the high ATTRACT signal present at pin 2 of flip-flop E7-5 is clocked by the positive-going trailing edge of the pulse produced at the output of NAND gate A1-6, causing the Q output of flip-flop E7-5 to go high. When the start pushbutton is released, flip-flop B1-6/3 is reset. This flip-flop is used to prevent transients that are produced by the contacts of the start pushbutton from disturbing the circuits of the computer.

2-33. Just before vertical sync, the 256V signal clocks the high output of flip-flop E7-5 through to the Q output of flip-flop E7-9/8. This high output is the START signal, which is applied to NAND gate D7-6 and various other circuits of the computer. The $\overline{\text{START}}$ signal is used to clear flip-flop E7-5 and is also used by other circuits of the computer to start the Rebound game.

2-34. Pin 4 of NAND gate D7-6 is high whenever game credit has been established by the credit circuit. As a result, the high output of flip-flop E7-9/8 forces the output of NAND gate D7-6 low. This low causes flip-flop E8-5/6 to change states, resulting in a low ATTRACT signal and a high $\overline{\text{ATTRACT}}$ signal. The $\overline{\text{ATTRACT}}$ signal is sent to various circuits of the computer, and the ATTRACT signal is sent to flip-flops D8-5 and D8-9/8, to NAND gate D7-3, and to various other circuits of the computer. These attract signals cancel the attract mode and permit the play mode to proceed. When the game is over, a high STOP signal clocks the fixed high level at pin 2 of flip-flop E8-5/6 through to the Q output (ATTRACT signal). The ATTRACT signal is sent to the two-play/one-play circuit and to various other circuits of the computer. The two-play/one-play circuit is discussed in the text pertaining to the credit circuitry.

2-35. WINDOWS

2-36. The term window is one that has been coined to explain the process of gating the TV lines so that they can only appear within certain limits. The most confusing thing about the window concept is that it takes information from the vertical sync circuit to produce a horizontal window and vice versa. For example, Figure 2-6 correlates the vertical signals required to produce a horizontal window between vertical positions 64V and 128V with the window produced on the TV screen. Thus, if the 64V and $\overline{128V}$ signals from the vertical sync circuits are ANDed, a signal develops that can be used to blank the electron beam of the picture for all TV lines except those occurring between vertical positions 64V and 128V. As a result, a bright band between positions 64V and 128V appears on the screen of the picture tube. The remainder of the screen remains dark.

2-37. SCORE CIRCUIT

2-38. Figure 2-7 shows the circuitry of the score circuit. This circuitry consists of the score window circuitry, left and right score counter circuits, multiplexers, a BCD-to-seven segment decoder, a score segment window circuit, and a stop circuit. Each of these circuits is discussed in the following text.

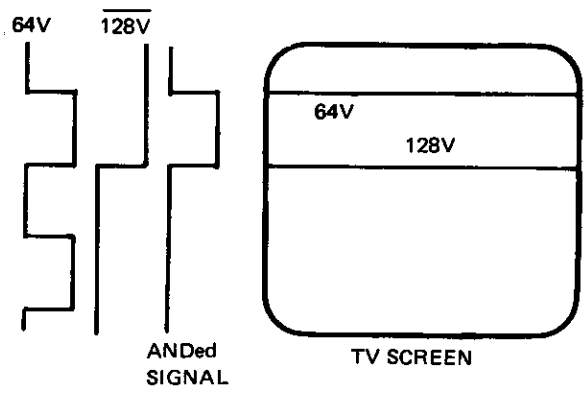


Figure 2-6. Development of a Typical Horizontal Window

2-39. Score Window Circuitry: The score window circuitry consists of NOR gate C8-13, AND gate F7-11, exclusive OR gates J5-8 and J5-11, NAND gates J6-3 and J6-6, negative-true AND gate K6-4, and inverter D4-6. Horizontal timing signals $\overline{256H}$, 64H, 256H, and 128H and vertical timing signals 64V, 32V, and 128V are matrixed to define the two score display areas. The left score display area begins at horizontal position 128H and ends at 192H, and the right score display area begins at horizontal position 320H and ends at 394H. Both score windows are located between vertical positions 32V and 64V. When the electron beam of the picture tube is within either of the two score display areas, the output of gate K6-4 is high. This high level is used to enable BCD-to-seven segment decoder/driver K7, which is discussed in subsequent text.

2-40. Score Counter Circuits: The left score counter circuit consists of decade counter K9 and J-K flip-flop H9-5/6, and the right score counter circuit consists of decade counter J9 and J-K flip-flop H9-3/2. These two counters are identical, therefore, only the left counter is described in the following text.

2-41. Decade counter K9 is reset to zero at the beginning of the game when the START signal goes high. At the same time, the Q output of flip-flop H9-5/6 is cleared to a low state and the $\overline{Q}$ output is cleared to a high state by a low $\overline{START}$ signal. During the game, high level inputs from the out-of-bounds/fourth-hit/miss circuitry for the right player are accumulated by the left score counter. The accumulated score is read out of K9 at pins 1, 9, 8, and 11 in BCD format. BCD output 1 from pin 1 is sent to the ball direction and speed circuitry, to NAND gate F8-6 of the stop circuit, and to multiplexer K8, BCD output 2 from pin 9 is sent to multiplexer K9, and BCD output 4 from pin 8 is sent to multiplexer J8 and the 11/15 score switch of the stop circuit. BCD output 8 from pin 11 is sent to J-K flip-flop H9-5/6 and multiplexer J8. Each time the BCD count changes from 1001 (decimal 9) to 0000 (decimal 10), flip-flop H9-5/6 is toggled, causing the Q output to go low. This low output of flip-flop H9-5/6 is used along with a fixed high input to pin 6 of multiplexer K8 to form BCD 0001, which is used to cause a 1 to appear in the tens position of the score. During the time the score is nine or less, the $\overline{Q}$ output of flip-flop H9-5/6 is high. This high output is used with the fixed high input to pin 6 of multiplexer K8 to form BCD 1111, which is used to cause no number to be generated for the tens position of the score.

2-42. Multiplexers and BCD-to-Seven Segment Decoder/Driver: The BCD score inputs to multiplexers K8 and J8 are sequentially gated to a BCD-to-seven segment decoder/driver by the 32H and 64H signals from the horizontal sync circuit. These gating signals are sequenced such that the tens information for the left score is gated first and is followed by the units information for the left score, the tens information for the right score, and finally the units information for the right score. When allowed by a high SCORE WINDOW signal, decoder/driver K7 sends a seven-bit code (signals a through g) to a score segment window circuit.

2-43. Score Segment Window Circuit: The score segment window circuit consists of NAND gates J7-12, J7-8, H7-6, J7-6, F8-8, H7-12, H7-8, J6-11, and F6-12; NOR gate K6-1 used as an inverter; negative-true AND gates H6-6, K6-13, and H6-12; negative-true OR gate H8-8; and inverters F9-4 and F9-8. Timing signals 4H, 8H, 4V, 8V, 16H, and 16V from the horizontal sync and vertical sync circuits are logically processed and used to enable the appropriate combination of NAND gates J7-12, J7-8, H7-6, J7-6, F8-8, H7-12, and H7-8 to allow various combinations of score segment signals (a through g) to reach negative-true OR gate H8-8. These sequenced score segment signals are ORed along with a $\overline{NET}$ signal from the net circuit to form the SCORE signal which is sent to the video summing circuit.

2-44. Stop Circuit: NAND gates F8-6 and F8-12 and negative-true OR gate J6-8 form a stop circuit. NAND gate F8-6 receives tens information from flip-flop H9-5/6 and units information from counter K9. When the 11/15 score switch is open, NAND gate F8-6 is enabled when the left score reaches 11. Alternately, when the 11/15 score switch is closed, NAND gate F8-6 is enabled when the left score reaches 15. NAND gate F8-12 receives inputs from the right score counter circuitry and operates exactly like NAND gate F8-6. When the output of either NAND gate goes low, it signifies that one player has accumulated a score of 11 or 15. This low causes the STOP signal to go high, and this high is sent to the start circuitry to switch the Rebound game from the play mode to the attract mode.

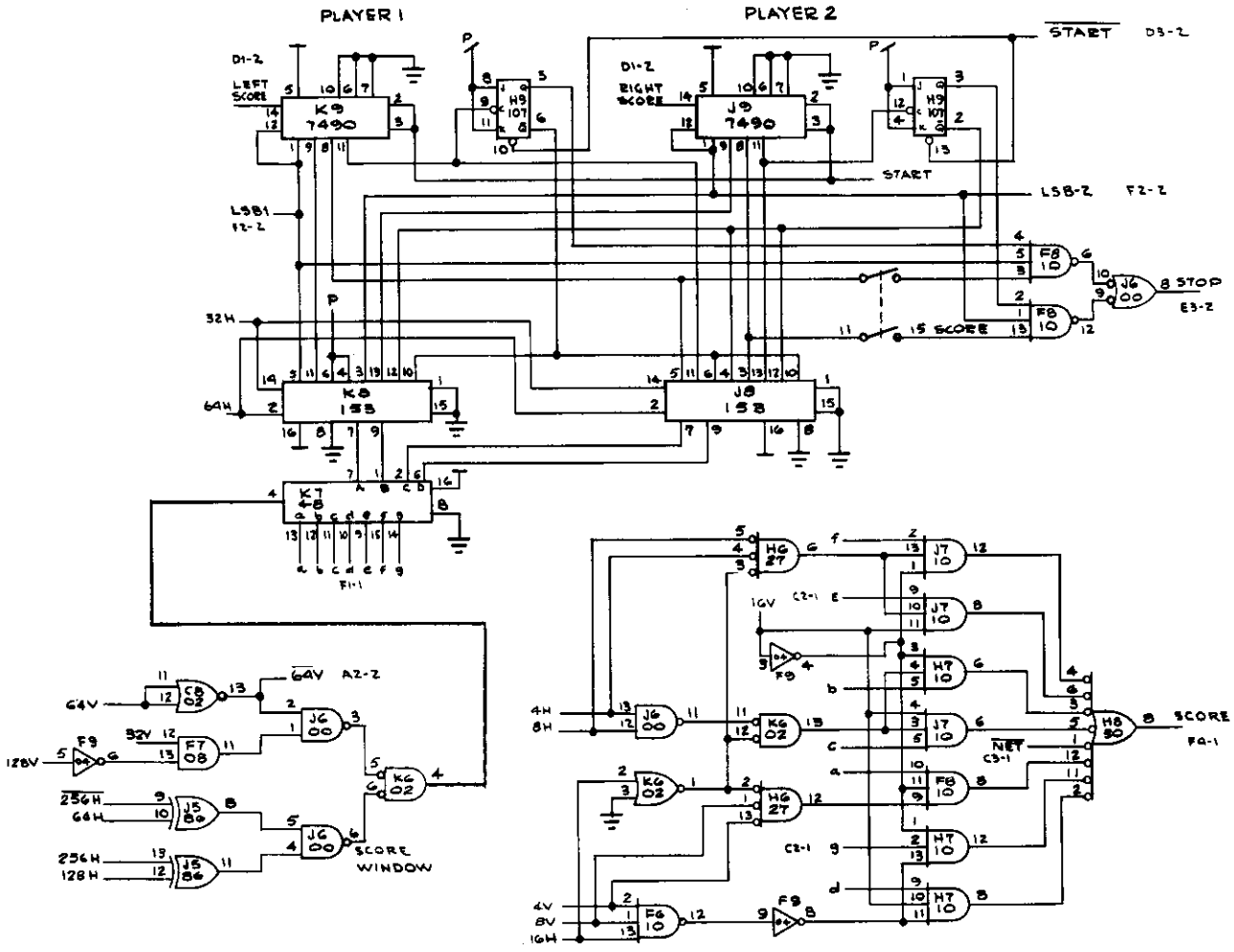


Figure 2-7. Score Circuit

2-45. PADDLE CIRCUIT

2-46. The paddle circuit (Figure 2-8) consists of two rotary potentiometers (not shown); timers C9 and B9 and associated circuitry; NOR gates C8-4 and C8-10; NAND gates D7-11, B8-6, D7-8, B8-8, H2-8, B1-11, F6-6, and F6-8; inverter B5-2; negative-true AND gate K6-10; AND gate E5-8; negative-true OR gates F7-6 and F7-8; counters C7 and B7; and multiplexer B6. Both rotary potentiometers are mounted on the front panel and are used by the players to position the paddle symbols shown on the picture tube. All other components of the paddle circuitry are located on the computer board. The paddle circuitry is subdivided into five circuits: the paddle 1 circuit, the paddle 2 circuit, the multiplexer, the paddle window circuit, and the stop circuit. Each of these circuits is described in the following text.

2-47. **Paddle Window Circuit:** The paddle window circuit consists of NAND gates H2-8 and B1-11, negative-true AND gate K6-10, and AND gate E5-8. Vertical timing signals 64V, 32V, 128V, 16V, and 8V are logically combined to develop a horizontal window for the paddle 1 and paddle 2 circuits. The window is located between vertical positions 248V and 256V. In addition, a 4V signal is used to gate the DISP PAD COMP (display paddle composite) signal through AND gate E5-8. Consequently, the final paddle signal is confined between vertical positions 252V and 256V.

2-48. **Multiplexer:** Multiplexer B6 is controlled by the 256H signal from the horizontal sync circuit. Between the leading edge of horizontal blanking and horizontal position 256H (essentially the left half of the picture), the multiplexer passes information from the paddle 1 circuit. From

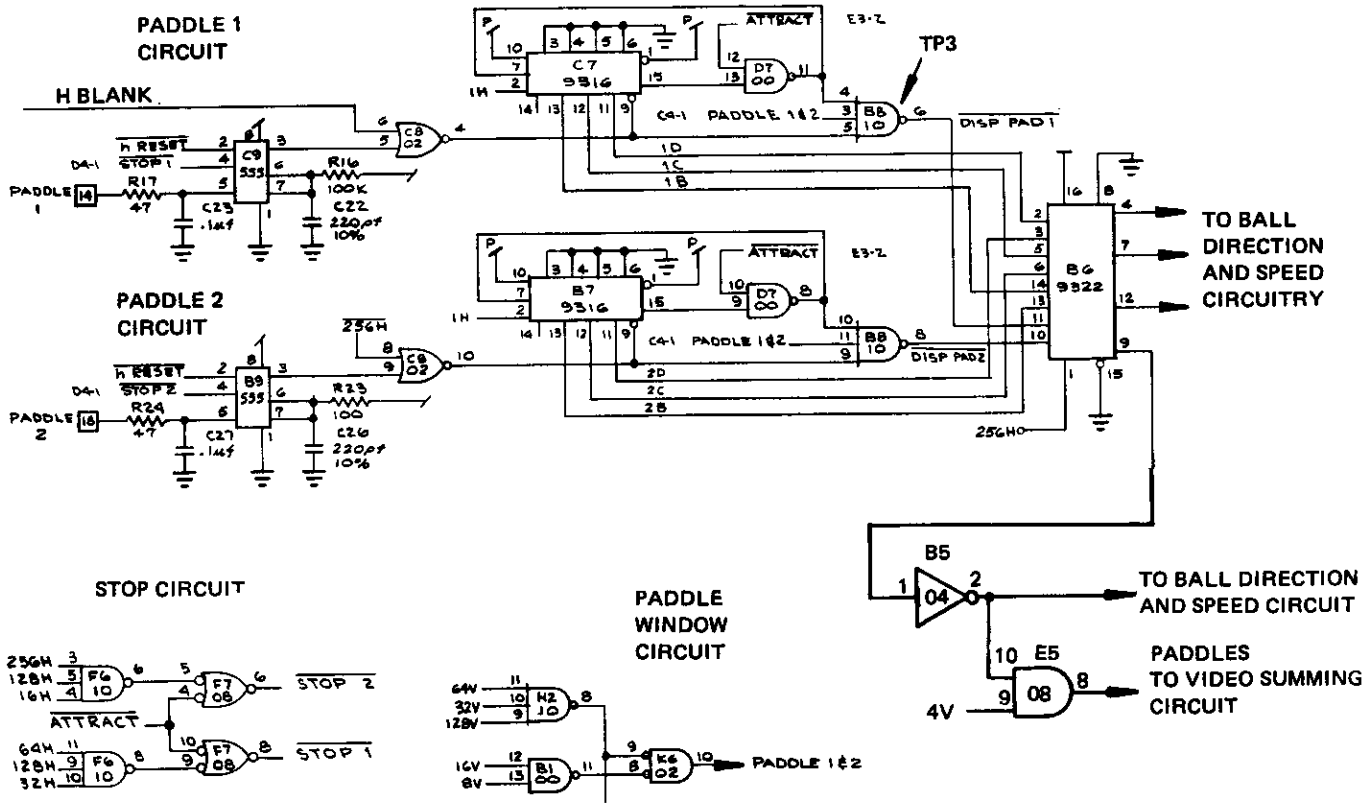


Figure 2-8. Paddle Circuit

horizontal position 256H to 453H (right half of picture), the multiplexer passes information from the paddle 2 circuit.

2-49. Paddle 1 and 2 Circuits During Attract Mode: The paddle 1 circuit consists of the front panel player 1 potentiometer; timer C9 and associated circuitry, NOR gate C8-4; counter C7; and NAND gates D7-11 and B8-6. The paddle 2 circuit consists of timer B9; NOR gate C8-10; counter B7; and NAND gates D7-8 and B8-8. Although controlled differently, these two paddle circuits operate identically.

2-50. During the attract mode, a low $\overline{\text{STOP 1}}$ signal from the stop circuit turns off timer C9 (pin C9-3 low) and a low $\overline{\text{ATTRACT}}$ signal from the start circuit inhibits NAND gate D7-11. As a result, the outputs of NOR gate C8-4 and NAND gate D7-11 are forced high during the active portion of the picture. With pins 10, 7, and 9 of counter C7 held high, it continuously counts 1H pulses and furnishes count information to multiplexer B6. When the PADDLE 1 & 2 signal is high, NAND gate B8-6 furnishes a low $\overline{\text{DISP PAD 1}}$ (display paddle 1) signal to the multiplexer. During horizontal blanking, the output of NOR gate C8-4 is forced low by the H BLANK signal. This low initializes counter C7 (zero output) and inhibits the $\overline{\text{DISP PAD 1}}$ signal. Between horizontal positions 256H and 400H the paddle 2 circuit furnishes count information and a $\overline{\text{DISP PAD 2}}$ signal to the multiplexer. Counter B7 is initialized and the $\overline{\text{DISP PAD 2}}$ signal is inhibited when the 256H signal goes high. Thus, the paddle 2 circuit does not furnish any useful information to the multiplexer for the left side of the picture.

2-51. Multiplexer B6 continuously passes first the paddle 1 information and then the paddle 2 information to the ball direction and speed circuitry and to inverter B5-2. The ball direction and speed circuitry (discussed elsewhere in this manual) receives information from counters C7 and B7, and inverter B5-2 alternately receives the low $\overline{\text{DISP PAD 1}}$ and $\overline{\text{DISP PAD 2}}$ signals. Consequently, during the active picture time, the output of inverter B5-2 is held high. When the 4V signal and the PADDLE 1 & 2 signals coincide, the DISP PAD COMP (display paddle composite) signal is passed through AND gate E5-8 to the video summing circuit. Thus, during the attract mode, a white bar, which is positioned between vertical positions 252V and 256V, is displayed from the left to right side of the picture.

2-52. Paddle 1 and 2 Circuits During Play Mode: During the play mode, a high $\overline{\text{STOP 1}}$ signal from the stop circuit enables timer C9 and a high $\overline{\text{ATTRACT}}$ signal from the start circuit enables NAND gate D7-11. Timer C9 is triggered by a negative-going $\overline{\text{H RESET}}$ pulse at the beginning

of horizontal blanking, forcing pin 3 of the timer high. This high, in conjunction with a high H BLANK signal, forces the output of NOR gate C8-4 low, which initializes counter C7 and inhibits NAND gate B8-6. When horizontal blanking is ended, pin 6 of NOR gate C8-4 goes low allowing timer C9 to control the gate for the remainder of the horizontal line.

2-53. The time constant of timer C9 is controlled by the front panel paddle position potentiometer. When C9 times out, as determined by the setting of the potentiometer, pin 3 of the timer goes low forcing the output of NOR gate C8-4 high. As a result, counter C7 begins counting 1H pulses and furnishes the resulting count information to the multiplexer. In addition, the high output of NOR gate C8-4 enables pin 5 of NAND gate B8-6. Thus, when the PADDLE 1 & 2 signal goes high, a low $\overline{\text{DISP PAD 1}}$ signal is sent to the multiplexer.

2-54. Multiplexer B6 passes the output of counter C7 to the ball direction and speed circuitry and the $\overline{\text{DISP PAD 1}}$ signal to inverter B5-2. When allowed by the 4V signal, the high output of inverter B5-2 is sent to the television monitor via AND gate E5-8 to cause the paddle 1 symbol to appear on the picture tube. When counter C7 reaches the count of BCD 1111 (decimal 15), pin 15 of the counter goes high and forces the output of NAND gate D7-11 low. This low stops the counter and inhibits NAND gate B8-6, causing the right edge of the paddle 1 symbol to be formed. Thus, the paddle 1 circuit determines where the left edge of paddle 1 starts on the TV screen and terminates the paddle symbol 15 1H pulses later. Using the front panel paddle 1 potentiometer in the play mode, the paddle 1 symbol can be moved back and forth horizontally between the left side and approximately the vertical center of the TV picture. The paddle 2 circuitry operates approximately the same as the paddle 1 circuit. However, the paddle 2 symbol cannot begin until the $\overline{\text{256H}}$ signal applied to NOR gate C8-10 goes low and the 256H signal applied to multiplexer B6 goes high. The right travel of both paddle symbols is limited by the stop circuit.

2-55. **Stop Circuit:** The stop circuit is composed of NAND gates F6-6 and F6-8 and negative-true OR gates F7-6 and F7-8. When the electron beam of the picture tube reaches horizontal position 224H during the play mode, the output of NAND gate F6-8 goes low. This low is passed through gate F7-8 to timer C9, causing pin 3 of the timer to go high and forcing the output of NOR gate C8-4 low. Consequently, counter C7 is reset to zero and NAND gate B8-6 is inhibited and paddle 1 symbol information is prevented from being displayed after horizontal position 224H. In a similar manner, paddle 2 information from the paddle 2 circuit is suppressed after horizontal position 400H.

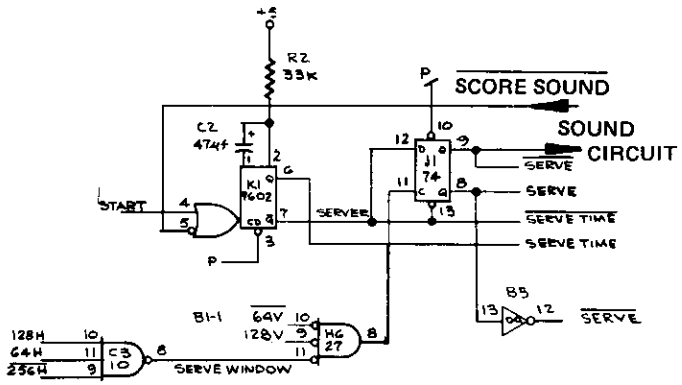


Figure 2-9. Serve Circuit

2-56. SERVE CIRCUIT

2-57. As shown in Figure 2-9, the serve circuit consists of NAND gate C3-8; negative-true AND gate H6-8; one-shot K1-6/7; flip-flop J1-9/8; and inverter B5-12. This circuit is used to generate the SERVE, $\overline{\text{SERVE}}$, SERVE TIME, and $\overline{\text{SERVE TIME}}$ signals that cause the horizontal and vertical ball motion circuits to initiate a serve after the front panel start pushbutton is pressed to start a new game, after each time the ball symbol goes out of bounds, or after the ball symbol hits a paddle four times without crossing the net. The serve circuit consists of a serve window circuit and a timing circuit, which are discussed in the following paragraphs.

2-58. **Serve Window Circuit:** NAND gate C3-8 and negative-true AND gate H6-8 form the serve window circuit. This circuit logically combines the 128H, 64H, $\overline{\text{256H}}$, $\overline{\text{64V}}$, and 128V signals from the horizontal sync and vertical sync circuits to develop a serve window that is located between vertical positions 64V and 128V and between horizontal positions 196H and 256H. The positive-going window pulse developed at the output of gate H6-8 is used to clock flip-flop J1-9/8 of the timing circuit.

2-59. **Timing Circuit:** The timing circuit consists of one-shot K1-6/7, flip-flop J1-9/8, and inverter B5-12. When the front panel start pushbutton is pressed after game credit has been established, the START signal goes high. This high START signal triggers one-shot K1-6/7, causing it to develop a nominal 0.5 second positive-going pulse at pin 6 (SERVE TIME) and a 0.5 second negative-going pulse at pin 7 ($\overline{\text{SERVE TIME}}$). One-shot K1-6/7 is also triggered whenever the ball goes out of bounds or after the ball hits a

paddle four times without crossing the net by a negative-going pulse from the sound circuit. In either case, the SERVE TIME pulse is sent to various circuits of the computer, and the $\overline{\text{SERVE TIME}}$ pulse is sent to the D and clear inputs of flip-flop J1-9/8 and to the ball direction and speed circuit. Flip-flop J1-9/8 is cleared by the negative-going $\overline{\text{SERVE TIME}}$ pulse, causing its Q output ($\overline{\text{SERVE}}$) to go low and its $\overline{Q}$ output (SERVE) to go high. After one-shot K1-6/7 times out, pin 6 of K1 goes low and pin 7 goes high. When the next positive-going serve window signal appears at the output of gate H6-8, the high $\overline{Q}$ output of one-shot K1-6/7 causes the Q output of flip-flop J1-9/8 to go high and the $\overline{Q}$ output to go low. The high $\overline{\text{SERVE}}$ signal from the Q output is sent to the sound circuit, net circuit, and to the ball direction and speed circuit. The low SERVE output is sent to the out-of-bounds/fourth-hit circuit and to inverter B5-12. The high $\overline{\text{SERVE}}$ output of inverter B5-12 is sent to the horizontal ball motion circuit.

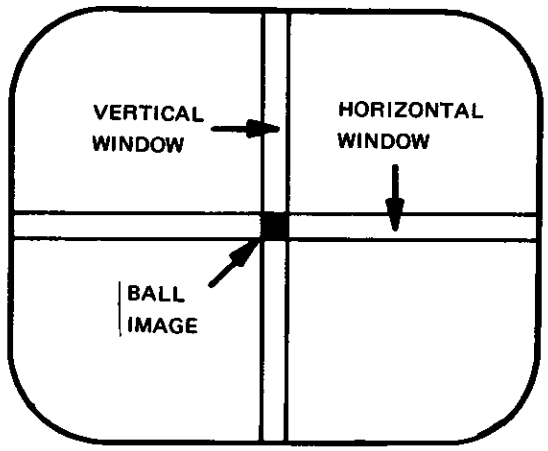
2-60. BALL MOTION

2-61. The ball image is created by intensifying the TV display at the intersection of narrow horizontal and vertical windows (Figure 2-10a). The two windows are moved independent of each other by the ball direction and speed circuits. When the horizontal and vertical windows move at the same speed (Figure 2-10b), the ball will appear to travel across the display at a 45^{o} angle. A faster vertical window speed (Figure 2-10c) will cause the ball to move faster in the horizontal direction and vice versa.

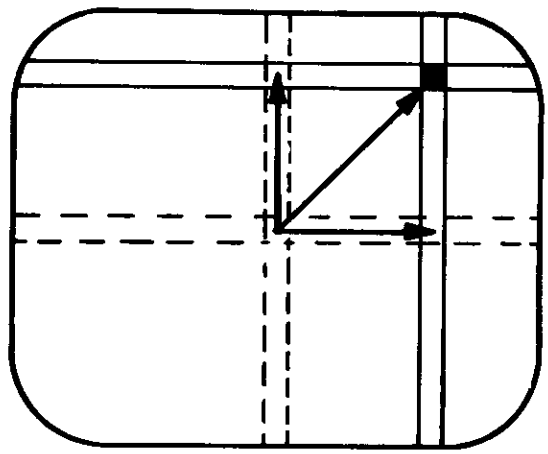
2-62. HORIZONTAL BALL MOTION

2-63. The horizontal ball motion circuit is almost identical in construction to the horizontal synchronization circuit. The major difference between the two circuits is that the counting process of the horizontal ball motion circuit can be controlled and it is this fact that is used to produce a counting differential between the sync circuit counting and the counting of the horizontal motion window.

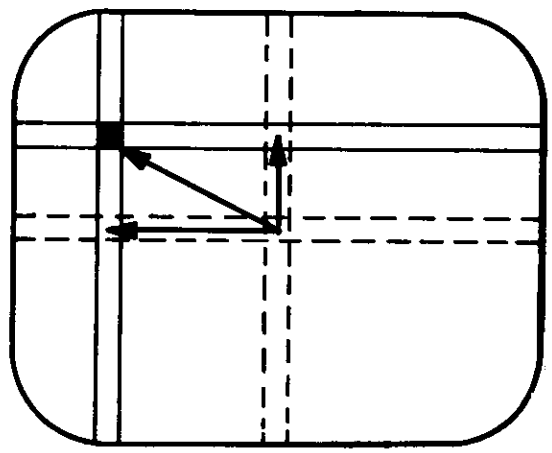
2-64. This counting differential is used to create a window that has the appearance of moving across the CRT screen. If the window is created in a slightly different place during each TV field, the window appears to move in much the same way the illusion of movement is created on the movie screen by the film in the motion picture projector. Even though ball motion consists only of a series of shifted ball images, the illusion of motion results from a combination of persistence of the image on the CRT phosphor and the persistence of the retinal after-image in the human eye. Thus, the human eye, unable to cope with the speed the



a. Ball Still



b. Equal Window Speeds



c. Faster Vertical Window

Figure 2-10. Ball Image Generation

ball image is shifted, interprets the information as real movement.

2-65. If the ball window signal occurs at the same frequency as the sync signal, the window appears in the same place each TV field. However, if the window signal that produces horizontal ball motion is delayed so that it counts one more clock pulse than horizontal sync, the window created in the next field is shifted one clock pulse to the right. If the signal is delayed yet another pulse, the resultant ball window is shifted two clock pulses to the right of the original position. The TV monitor electron beam sweeps 60 fields per second. If the vertical window is shifted one clock pulse per field, the ball will appear to move quite rapidly in the horizontal plane.

2-66. Horizontal ball motion direction is dependent on whether the horizontal motion signal is counted faster or slower than the horizontal sync signal. If it is counted at a faster rate (less clock pulses), the ball window will move left. If it is counted slower (more pulses), the window will move to the right. If it is counted at the same rate, the window does not shift either way. The velocity of the window motion is controlled by varying the distance the window is shifted per TV field. If the window is shifted one clock pulse per field, it appears to move half as fast as if it were shifted two clock pulses per field.

2-67. The horizontal motion circuit uses 9316 counters, which are almost identical to the 7493 counters of the horizontal sync circuit; the counters of both circuits are run in parallel by the same clock. The 7493 counters always start counting from zero. The count of the 9316, however, is started from a predetermined number. This predetermined number is generated by the ball direction and speed circuit and is known as the motion code. It is this binary motion code that produces the shift differential between the horizontal sync counting and the counting of the horizontal ball motion circuit.

2-68. VERTICAL BALL MOTION

2-69. The vertical ball motion circuit is almost identical to the horizontal motion circuit with the following exceptions. This circuit creates a horizontal window that moves vertically and, therefore, different inputs are used. The electron beam is blanked out during its vertical retrace, so $\overline{\text{V BLANK}}$ is used to turn the electron beam on and off at the right times. $\overline{\text{H SYNC}}$ provides the clock for the counters so that the horizontal window is created after the right number of horizontal lines. This circuit does not use a J-K flip-flop as a ninth bit for the counter because the largest number it needs to count is 272. The horizontal motion counters need to count to 455.

2-70. BALL DIRECTION AND SPEED CIRCUIT

2-71. The ball direction and speed circuit (Figure 2-11) consists of flip-flops D6-5, C6-5, D6-9/8, and C6-9/8; counter B4; up/down counter E4; exclusive OR gates C5-6, C5-3, C5-11, and C5-8; NAND gates D5-3, D5-8, and D5-11; negative-true AND gate E6-10; negative-true OR gates E5-6 and E5-11; and inverter B5-6. This circuit processes paddle, ball, serve, and score information and sends ball direction and speed information to the horizontal and vertical ball motion circuits.

2-72. Just prior to the actual serve initiation ($\overline{\text{SERVE}}$ signal going high), the $\overline{\text{SERVE TIME}}$ signal from the serve circuit goes low. This low signal clears flip-flop D6-5, causing the $\overline{\text{BACKWARDS}}$ signal to go low. A low $\overline{\text{BACKWARDS}}$ in the presence of no score directs the horizontal ball motion circuit to move the ball toward the right side of the TV picture when one-shot K1-6/7 of the serve circuit times out.

2-73. At the time of the initial serve in a game, the left player and right player scores are zero. Thus, the least significant bit signals (LSB-1 and LSB-2) from the score counters are both low and these lows force the output of exclusive-OR gate C5-8 to be low also. This low inhibits NAND gate D5-8 and is inverted by inverter B5-6 to form a high that enables NAND gate D5-11. Because the $\overline{\text{SERVE}}$ signal is also high at this time, the output of NAND gate D5-11 is forced low to clear flip-flops C6-5 and C6-9/8 and preset flip-flop D6-9. Consequently, the Q outputs of flip-flops C6-5 and C6-9/8 are low, the Q output of flip-flop D6-9/8 is high, the $\overline{\text{Q}}$ output of flip-flop D6-9/8 is low, and the $\overline{\text{Q}}$ output of flip-flop C6-9/8 is high.

2-74. The low output (signal DP) of flip-flop C6-5 is sent to the horizontal ball motion circuit and to exclusive OR gates C5-3 and C5-11. The high output (signal CP) of flip-flop D6-9/8 is applied to exclusive OR gate C5-3, and the low output (signal $\overline{\text{CP}}$) is sent to the horizontal ball motion circuit. The low output (signal BP) of flip-flop C6-9/8 is applied to exclusive OR gate C5, and the high output (signal $\overline{\text{BP}}$) is sent to the horizontal ball motion circuit. As a result, gate C5-3 furnishes a high level to negative-true OR gate E5-6, and gate C5-11 furnishes a low level to pin 15 of up/down counter E4. At the same time flip-flops C6-5, D6-9/8, and C6-9/8 are being cleared or preset, the $\overline{\text{SERVE}}$ signal from the serve circuit is low. Consequently, a low level is applied to pin 10 of counter E4 and to gate E5-6. In

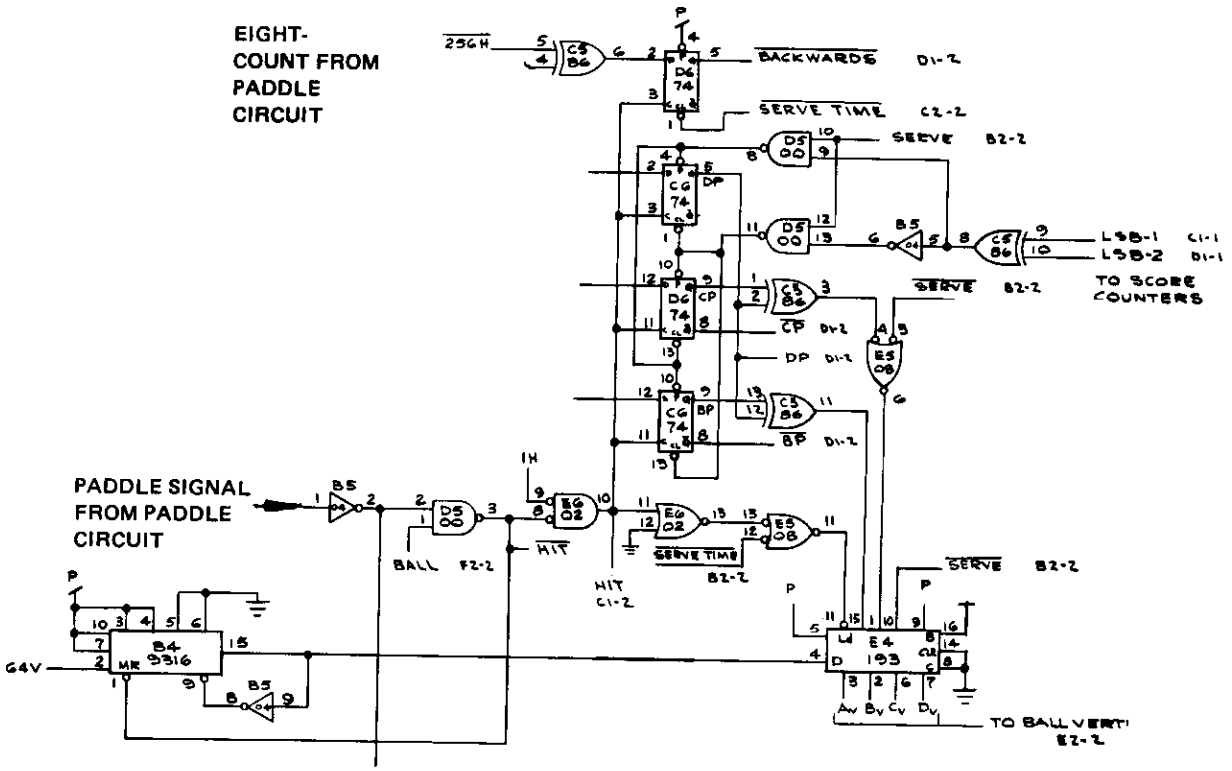


Figure 2-11. Ball Direction and Speed Circuit

turn, gate E5-6 furnishes a low level to pin 1 of counter E4. Because the $\overline{\text{SERVE TIME}}$ signal from the serve circuit is also low at the same time the $\overline{\text{SERVE}}$ signal is low, the levels at the preset inputs (pins 15, 1, 10, and 9) are loaded into counter E4 by the low output of gate E5-11. These preset levels represent a BCD 1000 (decimal 8), which is furnished via signals D_V, C_V, B_V, and A_V to the vertical ball motion circuit. This preset count is modified by a signal from the gravity simulator (counter B4), which is discussed in subsequent text.

2-75. During game play, three bits of BCD information from the multiplexer of the paddle circuit are regularly supplied to flip-flops C6-5, D6-9/8, and C6-9/8 of the ball direction and speed circuitry. This information indicates what portion (if any) of each paddle is present at each horizontal position of a horizontal line. Each time the ball "strikes" a paddle, pin 2 of NAND gate D5-3 is high (indicating the presence of a paddle), and the BALL signal from the horizontal and vertical ball motion circuits is high (indicating the presence of the ball). These highs force the output of NAND gate D5-3 low and this low $\overline{\text{HIT}}$ signal resets counter B4, enables negative-true AND gate E6-10, and is sent to the sound circuit to cause a hit sound to be generated.

2-76. When the next 1H pulse goes low, the output of gate E6-10 goes high (HIT signal). This high HIT signal causes the paddle segment information from the paddle circuit to be clocked into flip-flops C6-5, D6-9/8, and C6-9/8; is sent to the out-of-bounds/fourth hit/net hit circuit to record a hit; and is applied to NOR gate E6-13. The paddle segment information appearing at the outputs of flip-flops C6-5, D6-9/8, and C6-9/8 is sent to the horizontal ball motion circuit and via gating to the preset inputs of up/down counter E4. The high HIT signal is inverted by NOR gate E6-13 and then passed through negative-true OR gate E5-11 to pin 11 of counter E4, causing the preset information at pins 15, 1, 10, and 9 to be loaded into the counter.

2-77. Upon being reset to zero by the $\overline{\text{HIT}}$ signal, counter B4 begins accumulating 64V pulses. After 15 64V pulses have been accumulated, pin 15 of counter B4 goes high. This high causes counter E4 to be down counted one count from the preset value, which is determined by the outputs of gates C5-11 and E5-6, a high $\overline{\text{SERVE}}$ signal, and a fixed positive level. In addition, inverter B5-8 inverts the high output at pin 15 of counter B4, causing a fixed preset value (BCD 0011) to be loaded into the counter. Thus, until the next hit is sensed, the counter develops a high pulse

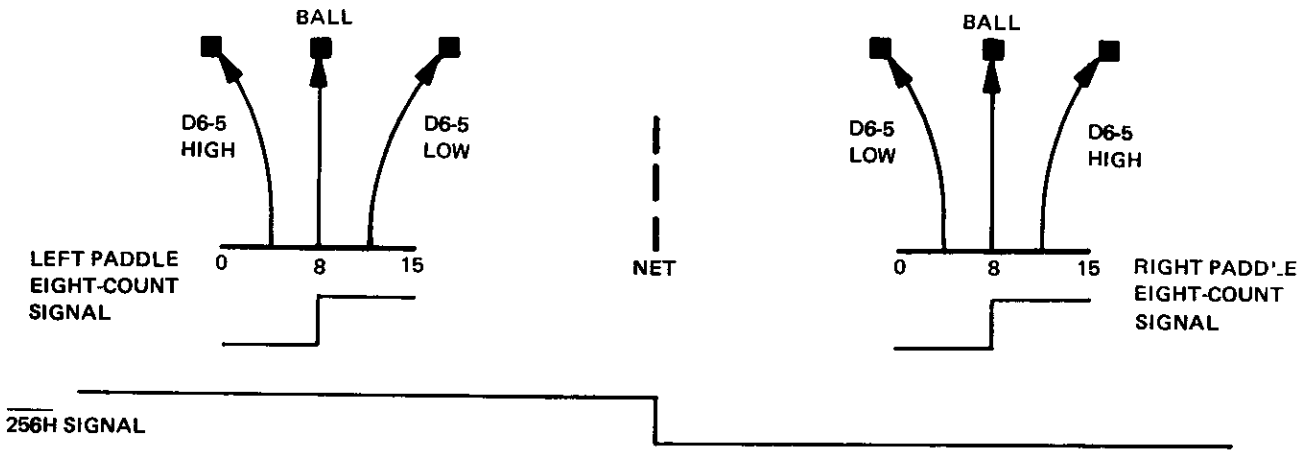


Figure 2-12. Ball Rebound

at pin 15 for every 12 64V pulses received. These positive-going pulses at pin 15 of B4 continuously cause counter E4 to be counted down one count for each positive pulse from counter B4. This technique of down counting counter E4 simulates the effect of gravity on the vertical travel of the ball. Thus, the ball symbol is caused to move in a ballistic trajectory across the screen of the picture tube.

2-78. Whenever the score is unequal during the game, the output of exclusive OR gate C5-8 is high. This high enables NAND gate D5-8 and causes NAND gate D5-11 to be inhibited. Consequently, the preset/clear configuration of flip-flops C6-5, D6-9/8, and C6-9/8 is caused to be different from the configuration caused by an equal score. This different preset/clear configuration causes a different speed code preset to be loaded into counter E4. As a result, the vertical serve speed is altered as the score changes.

2-79. Exclusive OR gate C5-6 and flip-flop D6-5 function together to cause the ball to move in various directions, depending on where the ball is hit on which paddle. The eight count in each paddle circuit, which indicates the approximate center of the paddle, is exclusively ORed with the $\overline{256H}$ signal in gate C5-6. Each time the HIT signal occurs, the output of gate C5-6 is clocked into flip-flop D6-5. Figure 2-12 depicts the direction of travel of the ball in various situations.

2-80. HORIZONTAL BALL MOTION CIRCUIT

2-81. Figure 2-13 shows the circuitry of the horizontal ball motion circuit. This circuit is composed of flip-flops F1-6 and F3-3; NAND gates E1-11, C3-6, and F4-8; negative-true OR gates F2-3 and F2-11; NOR gate H1-8; AND gate F2-6; full adder E2; and counters E3 and D3. When a START command, out-of-bounds indication, fourth-hit indication is sensed, a low $\overline{\text{SERVE}}$ signal is developed, causing counters E3 and D3 to be reset and flip-flop F3-3 to be cleared (Q output low). At the same time, a low $\overline{\text{SERVE}}$ $\overline{\text{TIME}}$ signal causes the $\overline{\text{BACKWARDS}}$ signal to go low, which causes the $\overline{Q}$ output of flip-flop F1-6 to go high. When the V RESET signal goes high, just prior to the beginning of a new field, flip-flop F1-6 is clocked and AND gate F2-6 furnishes a high level to gates F2-3, F2-11, and H1-8. This high level allows these gates to pass horizontal speed information (signals $\overline{BP}$, $\overline{CP}$, $\overline{DP}$, and DP) to the inputs of full adder E2. The horizontal speed information and a fixed zero at pin E2-1 is summed with three bits of fixed information (ones at pins E2-4 and E2-7 and a zero at pin 16) and the DP signal. The resulting sum is sent to the preset inputs of counter E3.

2-82. When the $\overline{\text{SERVE}}$ signal goes high, counters E3 and D3 begin counting CLOCK pulses and flip-flop F3-3 is allowed to be toggled. At the count of 226 (approximately half a horizontal line), pin 15 of counters E3 and D3 and pin 3 of flip-flop F3-3 are high, causing NAND gates C3-6 and F4-8 to be enabled. Enabling NAND gate F8-8 causes a low $\overline{\text{H VIDEO}}$ signal to be sent to the ball motion summing circuit to cause the ball to appear at the vertical center of the TV picture. Enabling NAND gate C3-6 causes the ball speed preset data to be loaded into counter E3 and the fixed preset data (BCD 0011) to be loaded into counter D3. These presets cause the vertical window to be displaced a fixed amount to the right of center of the display for each

new field that is painted, thus providing the horizontal speed vector of the ball during the serve. Notice that the Q output of flip-flop F3-3 is toggled low at the end of the second half line count and is then toggled high after a full line count (including presets). Consequently, the low $\overline{\text{BALL LOAD}}$ and $\overline{\text{H VIDEO}}$ are now developed once per line until the next serve.

2-83. If the ball hits the right half of the left paddle or the left half of the right paddle, a low $\overline{\text{BACKWARDS}}$ signal clears flip-flop F1-6. Therefore, gates F2-3, F2-11, and H1-8 are enabled during the next V RESET signal. However, in this instance, the speed data applied to adder E2 depends on where the ball "strikes" the paddle. As a result, the horizontal ball motion circuit develops a vertical window that moves at a rate determined by the speed data present at the inputs of gates F2-3, F2-11, and H1-8.

2-84. If the ball hits the left half of the left paddle or the right half of the right paddle, a high $\overline{\text{BACKWARDS}}$ signal is applied to pin 1 of flip-flop F1-6. Thus, the $\overline{\text{Q}}$ output of flip-flop F1-6 remains low, which inhibits F2-6. Inhibiting gate F2-6 causes a BCD 0100 to be summed with a BCD 0110 in the adder (E2) to yield a BCD 1010, which is a preset code that causes the horizontal ball motion circuit to move the vertical window at full horizontal speed.

2-85. If the ball hits the center of the paddle (count seven of the paddle counter), the circuit composed of flip-flop F1-6 and AND gate F2-6 allows speed data to pass through gates F2-3, F2-11, and H1-8 when the V RESET signal goes high. When this data and a fixed zero at pin E2-1 is summed with signal DP and fixed inputs of adder E2, a stop code (0101) appears at the output of the adder. When the stop code is preset into counter E3, the ball motion counter (E3, D3) counts in synchronism with beam sweep, which results in no horizontal motion. With no horizontal speed vector, the ball is moved straight up and down by the vertical ball motion circuit.

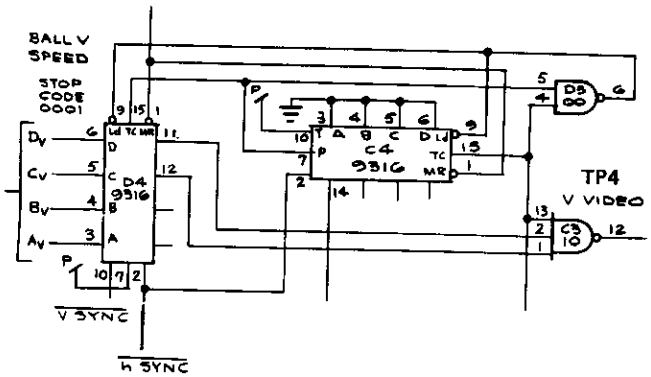


Figure 2-14. Vertical Ball-Motion Circuit

2-86. VERTICAL BALL MOTION CIRCUIT

2-87. The vertical ball motion circuit (Figure 2-14) is composed of counters D4 and C4 and NAND gates D5-6 and C3-12. This circuit is similar to the horizontal ball motion counter (E3, D3, F3-3, C3-6, and F4-8).

2-88. When the $\overline{\text{SERVE}}$ signal from the serve circuit goes low, counters D4 and C4 are reset. When the $\overline{\text{SERVE}}$ signal goes high indicating a serve is to be initiated and the $\overline{\text{V SYNC}}$ signal goes high indicating the beginning of a new field, counters D4 and C4 begin accumulating $\overline{\text{H SYNC}}$ pulses. After 225 counts (approximately one field), NAND gates D5-6 and C3-12 are enabled, causing a low V VIDEO signal to be sent to the ball motion summing circuit to cause a horizontal window and counter D4 to be preset with vertical ball motion data for the serve.

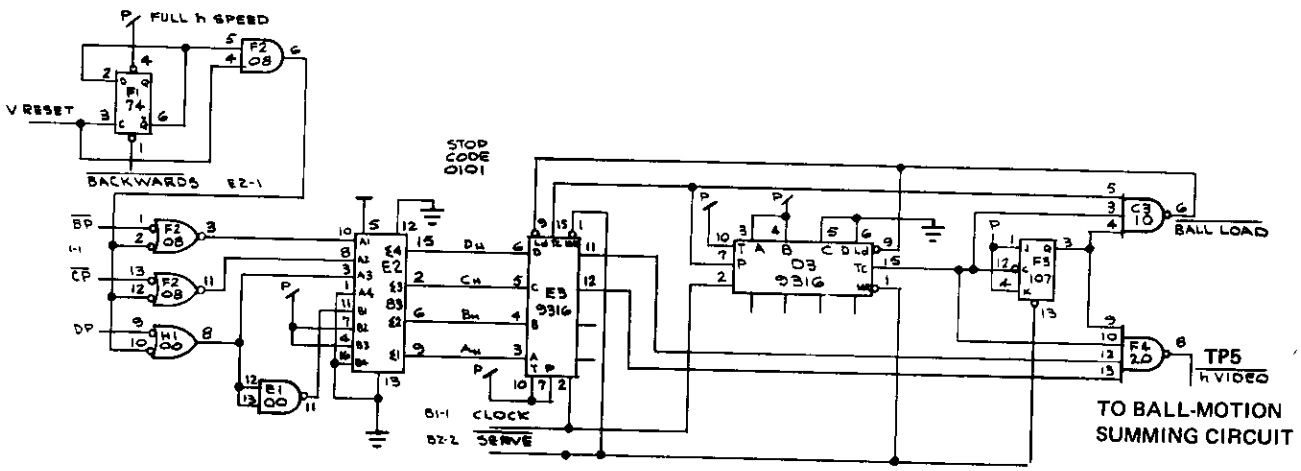


Figure 2-13. Horizontal Ball-Motion Circuit

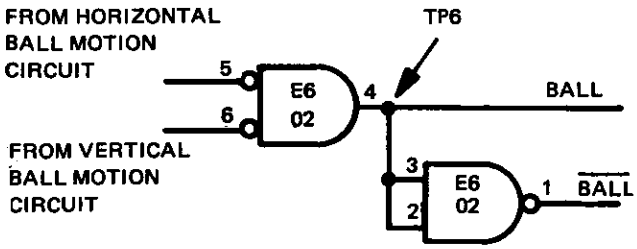


Figure 2-15. Ball Motion Summing Circuit

2-89. When the ball hits a paddle, new ball speed data is furnished to the preset inputs of counter D4. Thus, the horizontal window is caused to be moved up and down at a rate determined by the new speed data. The terminal count signal and the LSB signal of counter C4 are sent to the sound circuit. These signals help develop the sound that accompanies a hit or score.

2-90. BALL MOTION SUMMING CIRCUIT

2-91. The ball motion summing circuit (Figure 2-15) is composed of negative-true AND gate E6-4 and a NOR gate E6-1 that is used as an inverter. When the H VIDEO signal (vertical ball window) and V VIDEO (horizontal ball window) are coincidently low, a high BALL signal is sent to NOR gate E6-1 and the out-of-bounds/fourth hit/net hit circuit.

2-92. VIDEO SUMMING CIRCUIT

2-93. Figure 2-16 shows the video summing circuit, which is composed of capacitor C25 and resistors R25 through R29. This circuit combines the SCORE, $\overline{\text{COMPOSITE SYNC}}$, BALL, and PADDLES signals into a composite VIDEO OUT signal. Capacitor C25 couples the VIDEO OUT signal to the video circuits of the TV monitor.

2-94. OUT-OF-BOUNDS/FOURTH HIT/NET HIT CIRCUIT

2-95. The out-of-bounds/fourth hit/net hit circuit (Figure 2-17) consists of flip-flops B3-3, J2-5, and B2-5/6; counter C1; one-shot D1-9; negative-true OR gate B1-8; exclusive OR gate J5-3; AND gates E5-3, A1-11, and A1-3; NOR gates D2-10 and D2-1; negative-true AND gates D2-4 and D2-13; and AND-OR-INVERT gates C2-8 and C2-6. This circuit senses when the ball has hit a paddle four times; has gone out of bounds at the top, bottom, or either side of the picture; or has hit the net. If the ball is missed by a paddle, the miss is sensed when the ball goes out of bounds at the bottom of the picture. When the ball goes out of bounds, hits a paddle four times, or hits the net, a signal is sent to the sound circuit to cause a score sound; and another signal is sent to the score circuit to cause the appropriate score to be displayed

2-96. Just prior to the ball being served, the $\overline{\text{SERVE}}$ signal goes low, which clears flip-flop B3-3 and presets flip-flop J2-5. With the Q output of flip-flop B3-3 low and the Q output of flip-flop J2-5 high, exclusive OR gate J5-3 passes a high level that resets counter C1. When the next positive-going 2H pulse occurs, the Q output of flip-flop J2-5 is clocked low, which inhibits exclusive OR gate J5-3.

2-97. When the ball is served, the BALL signal goes high. Since the ball is served to the right player, the 256H signal is high at this time. As a result, the Q output of flip-flop B3-3 goes high, which causes another high reset pulse to be applied to counter C1. The high at the Q output of flip-flop B3-3 is clocked to the Q output of flip-flop J2-5 when the next positive-going 2H pulse occurs. Consequently, the output of exclusive OR gate J5-3 goes low, thereby enabling counter C1.

2-98. If a hit occurs, one-shot D1-14 is triggered by a positive-going HIT SOUND pulse and generates a negative-going pulse that increments counter C1 one count. If the ball is subsequently hit by the left paddle, flip-flop B3-3 changes states and exclusive OR gate J5-3 passes a high level that resets counter C1. If the ball goes out of bounds or hits the net, flip-flop B3-3 also is forced to change state by the next low $\overline{\text{SERVE}}$ signal, causing counter C1 to be reset. However, if the ball hits the right paddle four times without being hit with the left paddle, hitting the net, or going out of bounds, pin 8 of counter C1 goes high (4TH HIT signal). This high is applied to NOR gate D2-10.

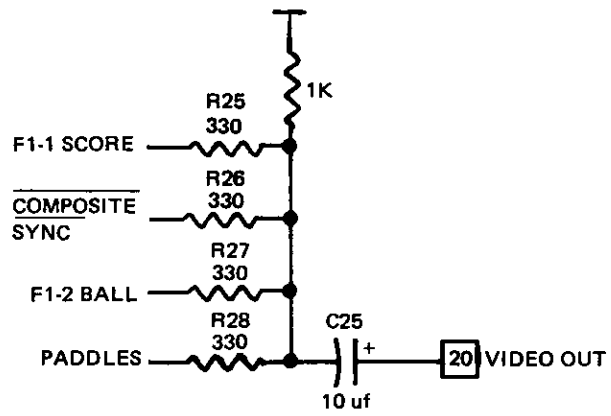


Figure 2-16. Video Summing Circuit

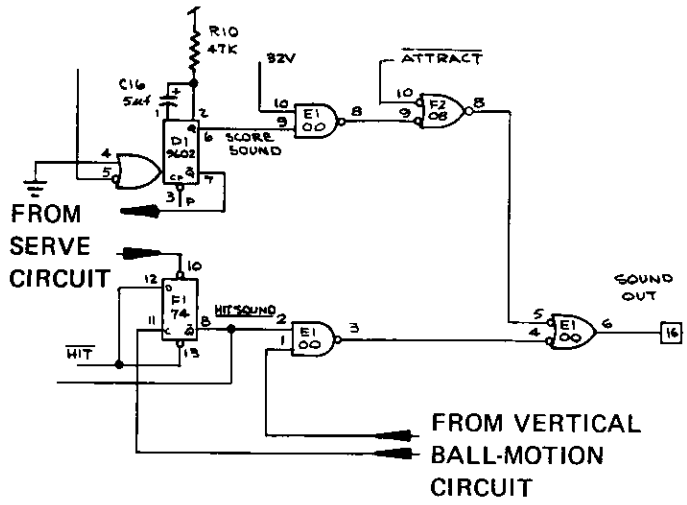


Figure 2-18. Sound Circuit

sequence and causes a positive-going pulse to be applied to NAND gate E1-8. This positive-going pulse enables gate E1-8, allowing the 32V signal to be sent to negative-true NOR gate F2-8. During the play mode. gate F2-8 is enabled by a high $\overline{\text{ATTRACT}}$ signal, allowing the 32V signal to be applied to negative-true OR gate E1-6.

2-108. When the serve sequence is initiated, a low $\overline{\text{SERVE}}$ signal presets flip-flop F1-8, which causes NAND gate E1-3 to be inhibited. When a paddle hits the ball, a negative-going $\overline{\text{HIT}}$ signal from the ball direction and speed circuit clears flip-flop F1-8, causing NAND gate E1-3 to be enabled. Upon being enabled, gate E1-3 passes a signal from the vertical ball motion circuit to gate E1-6. Later, after the $\overline{\text{HIT}}$ signal has gone high, another signal from the vertical ball motion circuit causes flip-flop F1-8 to change states, which, in turn, inhibits gate E1-3.

2-109. Negative-true OR gate E1-6 passes the periodic signal from either gate F2-8 or E1-3 to the sound circuit of the TV monitor. The sound circuit amplifies the SOUND OUT signal and provides an audible output at the speaker of the TV monitor.

2-110. NET CIRCUIT

2-111. The net circuit (Figure 2-19) consists of one-shot K1-9; flip-flops J1-5/6 and B2-8; counters K2 and K3; NAND gates H1-6, H2-8, K4-8, and B8-12; negative-true OR gate K4-6; and inverter B5-10. This circuit develops the signal for the net symbol and increases the height of the symbol after the ball has been successfully returned to the opposite side of the net two times in succession.

2-112. Just prior to each serve, the SERVE signal goes high, which clears counter K2. With the outputs at pins 9, 8, and 11 of counter K2 low, a BCD 0001 is loaded into counter K3 when the 128V signal goes low (top half of picture). When the 128V signal goes high, K3 starts counting 4V pulses. While K3 is counting, pin 15 of K3 is low, which forces the output of NAND gate K4-8 to be high. The output of NAND gate H2-8 is also high at this time, which forces the output of gate K4-6 low. Consequently, flip-flop B2-8 is held in a preset state (pin B2-8 low), which inhibits NAND gate B8-12.

2-113. When K3 reaches its terminal count, pin K3-15 goes high. Providing the lower half of the TV screen (indicated when signal 128V is high) is being swept by the electron beam, the output of NAND gate K4-8 goes low, which stops counter K3 and forces the output of gate K4-6 high. Thus, the next time a positive-going 2H pulse occurs when the 256H signal is low (left half of picture), the Q output of flip-flop B2-8 is clocked high. When the 256H signal goes high at the approximate vertical center of the picture, NAND gate B8-12 has enabling levels at pins 1 and 13. Therefore, each time the 4V signal goes high, a low $\overline{\text{NET}}$ signal is developed that causes another portion of the net symbol to appear on the TV screen. In addition, the low $\overline{\text{NET HEIGHT}}$ signal taken from the output of inverter B5-10 is sent to the out-of-bounds/fourth hit/net hit circuit to indicate the presence of the net symbol. This process continues until time 256V.

2-114. After 256V, counter K3 is preset by a low 128V signal and the outputs of NAND gates H2-8 and K4-8 go high. Flip-flop B2-8 is preset by the low output of gate K4-8, which inhibits gate B8-12 and establishes the bottom of the net. As a result, a net symbol that consists of a series of short vertical lines is formed on the TV screen.

2-115. After the ball is served, the $\overline{\text{SERVE}}$ signal goes high. If the ball is returned, the BALL MOTION signal goes high momentarily. One-shot K1-9 is triggered by the high $\overline{\text{SERVE}}$ signal and positive-going BALL MOTION pulse and produces a negative-going pulse at the $\overline{\text{Q}}$ output, which is applied to flip-flop J1-5/6. Assuming this flip-flop is in a cleared state, the trailing edge negative-going pulse clocks the Q output to a high level. The next positive-going BALL RETURN pulse causes the Q output of flip-flop J1-5/6 to be clocked to a low level, which causes counter K2 to be augmented by one count. If the ball continues in play, the counter is augmented once for every two times the ball is returned. Each time the 128V signal goes low, counter K3 is preset to a new count that is determined by the current count contained in counter K2. When the 128V signal goes high, counter K3 begins counting from the preset value. Thus, as the count builds in counter K2, the time required for counter K3 to reach its terminal count decreases. Con-

sequently, the net symbol is allowed to appear earlier after every two returns of the ball. This process continues until counter K2 reaches the BCD count of 0101 (decimal 10). At this point, the low output of NAND gate H1-6 holds flip-flop J1-5/6 in a cleared state, which prevents counter K2 from being augmented and, therefore, the net from increasing in height. Counter K2 is reset after the next serve, and the net is accordingly reduced to its minimum height.

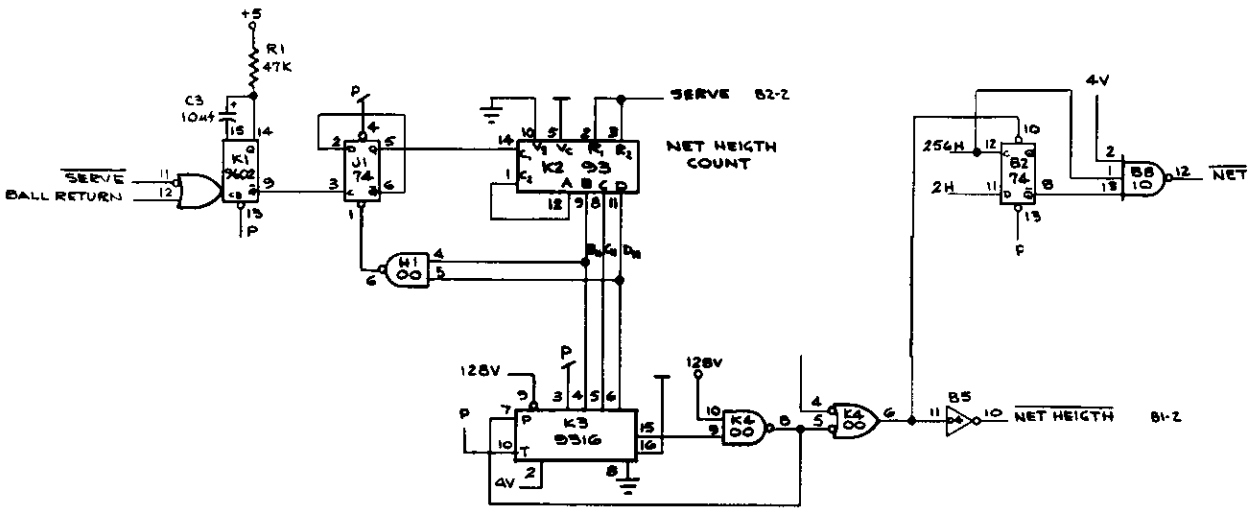
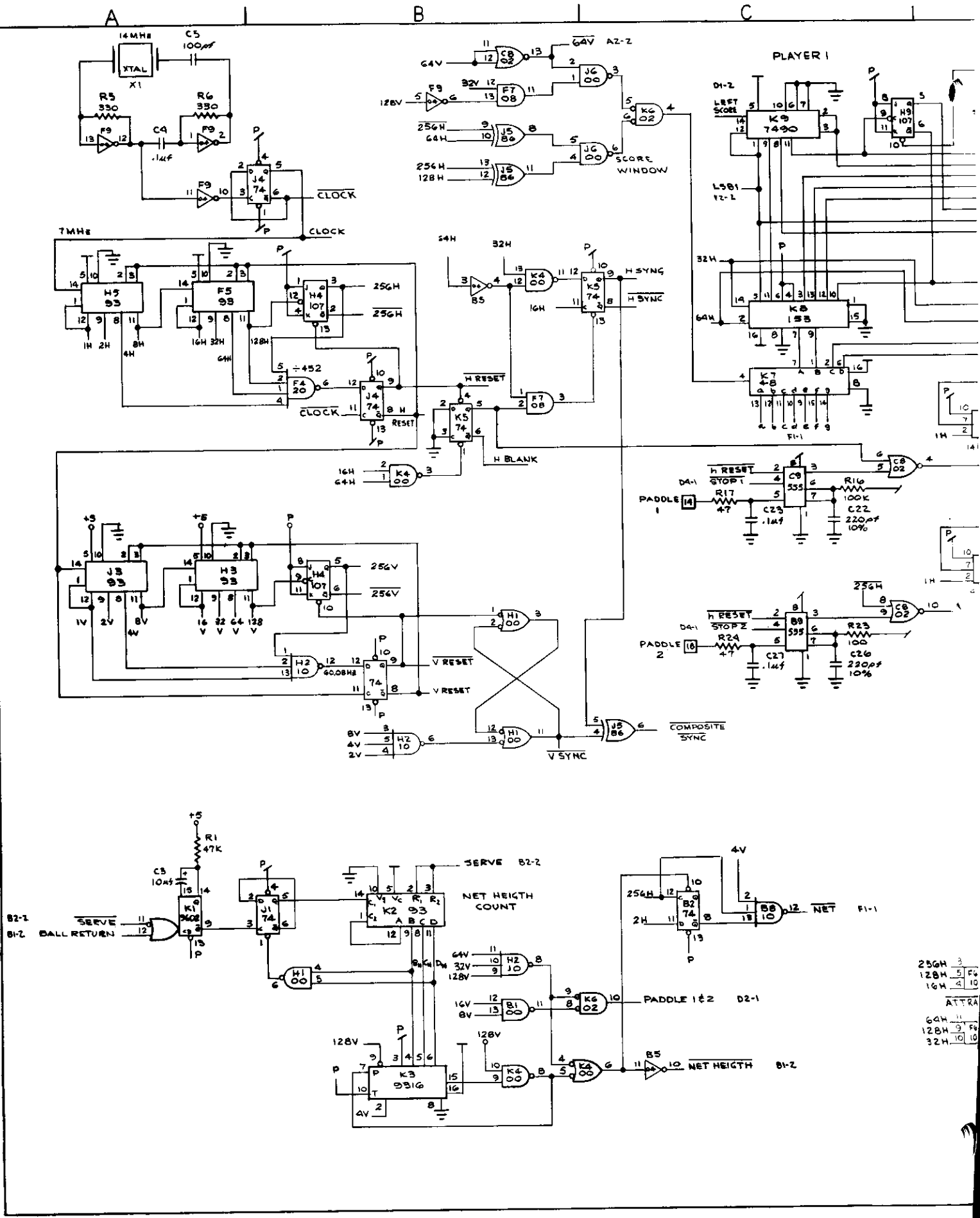
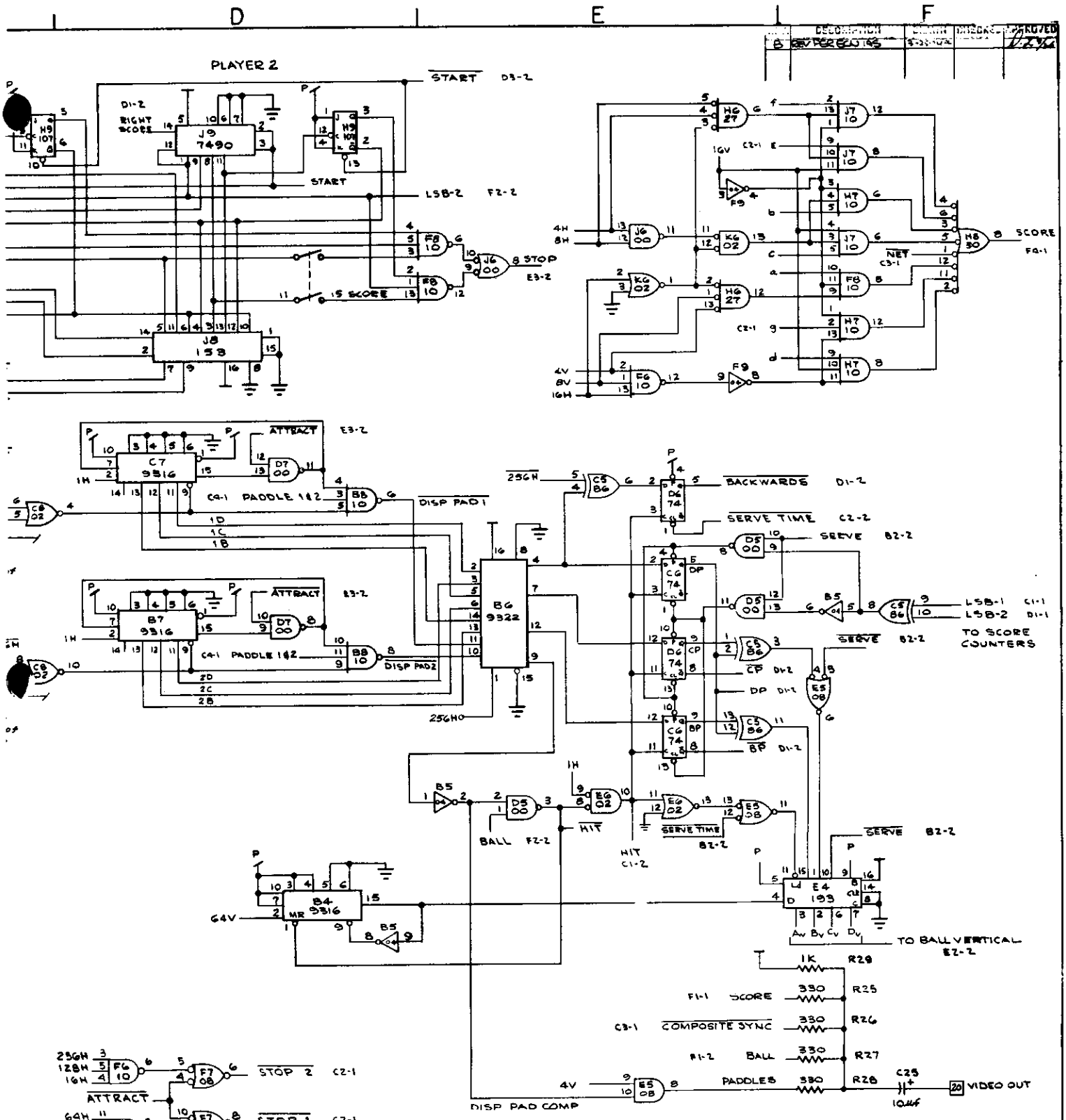


Figure 2-19. Net Circuit

Table 2-1. Rebound PCB Parts List

ITEM	PART NO.	QTY.	DESCRIPTION
1	10101	3	100 ohm ± 10%, 1/4 W, Resistor
2	10102	9	1 K ohm " " "
3	10104	3	100 K ohm " " "
4	10151	1	150 ohm " " "
5	10221	1	220 ohm " " "
6	10331	7	330 ohm " " "
7	10333	1	33 K ohm " " "
8	10470	2	47 ohm " " "
9	10473	3	47 K ohm " " "
10	19100	1	4 ohm ± 20%, 10W, Resistor, Wirewound
11	30100	1	100 pf Capacitor, Mica
12	30102	2	220 " " "
13	32101	1	0.1 uf Capacitor Mylar, ± 10%, 6V
14	34101	17	0.1 uf Ceramic Bypass Capacitor
15	35103	2	10 uf Capacitor, Electrolytic, 6V
16	35254	1	250 uf Capacitor Electrolytic, 6V
17	35473	2	47 " " " "
18	35502	1	5.0 " " " 10V
19	37000	1	8000 uf Capacitor Electrolytic, 16V
20	60000	2	Switch, DPDT Slide, PC Mount
21	70000	2	2N3643 Transistor
22	70001	1	2N3644 "
23	71000	4	1N914 Diode
24	71001	1	4001 Diode
25	71006	2	Diode, GE No. A14u
26	72000	8	7400 Integrated Circuit
27	72001	4	7402 " "
28	72002	3	7404 " "
29	72003	7	7410 " "
30	72004	1	7420 " "
31	72006	1	7427 " "
32	72007	1	7430 " "
33	72008	1	7448 " "
34	72009	1	7450 " "
35	72010	11	7474 " "
36	72011	1	7483 " "
37	72012	2	7486 " "
38	72013	2	7490 " "
39	72014	6	7493 " "
40	72015	4	74107 " "
41	72016	2	74153 " "
42	72017	8	9316 " "
43	72018	3	555 " "
44	72019	1	LM309K Voltage Regulator
45	72025	1	9322 Integrated Circuit
46	72026	2	9602 " "
47	72027	3	7408 " "
48	72035	1	74193 " "
49	75100	2	Screw, No. 6-32x5/8 Stainless St. Pan Hd.
50	75101	4	Washer, Lock No. 6-32 Internal Star, Stainless
51	75102	2	Washer, No. 6-32 Flat
52	75103	2	Hex Nut, No. 6-32
53	81001	1	Crystal, 14.31818 mhz
54	83014	1	Heatsink, Wakefield No. 690-3-B
55	84001	A/R	Heatsink Compound, Dow No. 340
56	000517	1	PCB Rev. C
57	000795	Ref	Schematic Rev. C
58	G000846	Ref	Artwork Rev. C


A
B
C
14MHz
C5
100pf
XTAL
X1
R5
330
R6
330
C9
.1uf
CLOCK
7MHz
H5
93
F5
98
256H
256H
÷452
F4
20
J4
74
H RESET
RESET
CLOCK
64V
32V
128V
F9
F7
08
J6
00
256H
64H
J5
86
256H
128H
SCORE
WINDOW
64H
32H
H SYNC
H SYNC
K4
00
K5
74
16H
H BLANK
PLAYER 1
LEFT
SCORE
K9
7490
L581
K8
153
K7
48
F1-1
h RESET
STOP 1
PADDLE
1
R17
47
C23
.1uf
C9
555
R16
100K
C22
220pf
10%
J3
93
H3
93
1V
2V
8V
4V
16
V
32
V
64
V
128
V
256V
256V
H2
10
60.08Hz
V RESET
V RESET
H1
00
8V
4V
2V
V SYNC
J5
86
COMPOSITE
SYNC
h RESET
STOP 2
PADDLE
2
R24
47
C27
.1uf
C26
220pf
10%
R23
100
256H
R1
47K
C3
10uf
K1
3608
SERVE
BALL RETURN
J1
74
SERVE
NET HEIGTH
COUNT
K2
93
64V
32V
128V
16V
8V
K6
02
PADDLE 1 & 2
128V
K3
9316
4V
128V
K4
00
B5
NET HEIGTH
256H
2H
B2
74
4V
B8
10
NET
256H
128H
16H
64H
128H
32H



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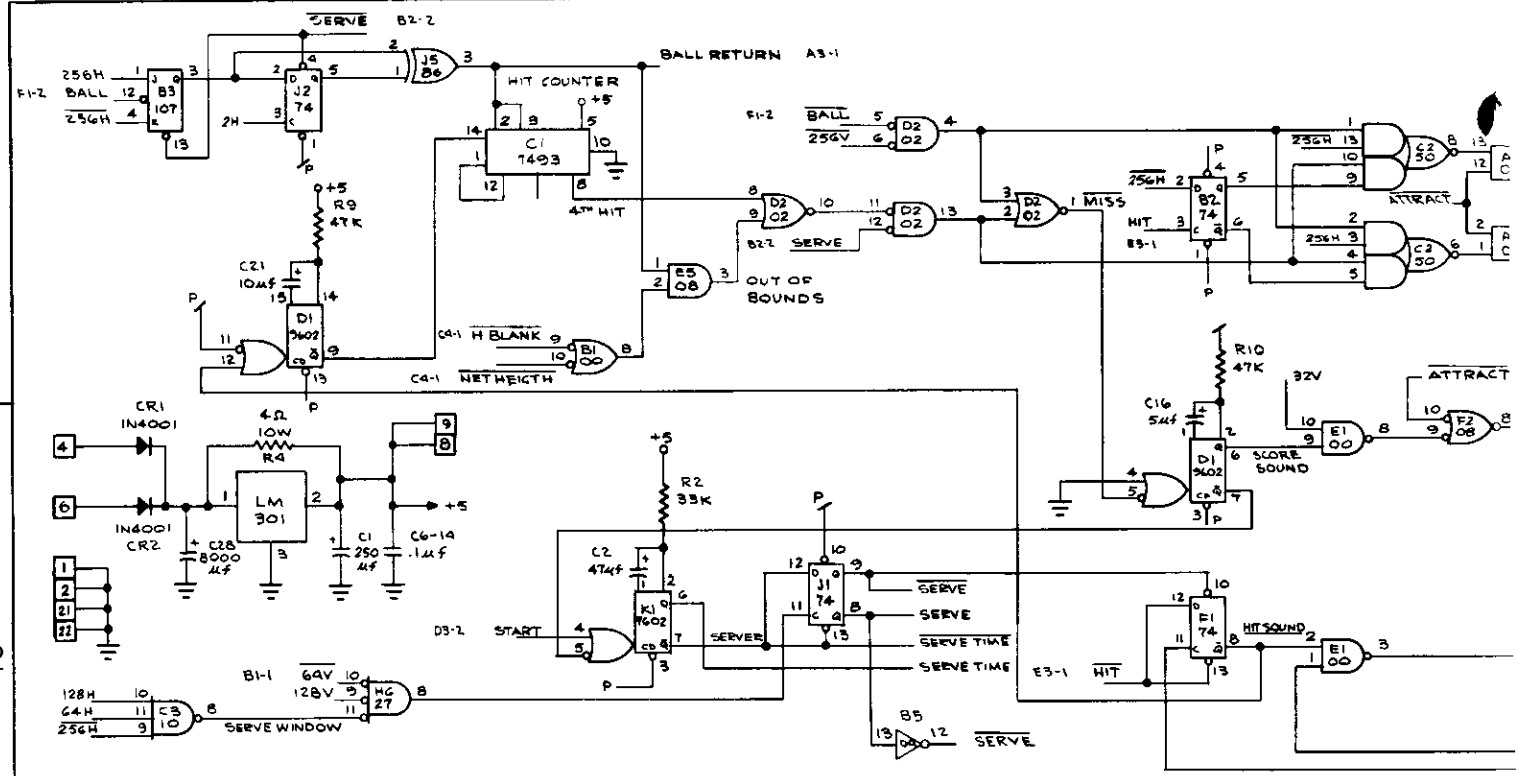
REV B

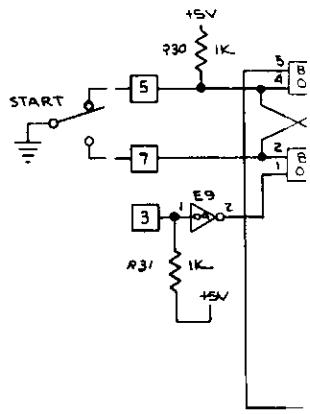
SCHEMATIC - VOLLYBALL

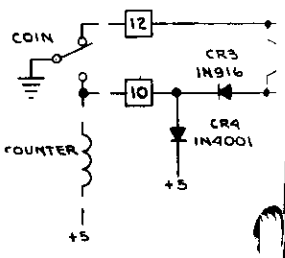
DRN: APP

#000745 SHT 1 OF 2

Figure 2-21. Computer Board Schematic, Revision B (Sheet 1)







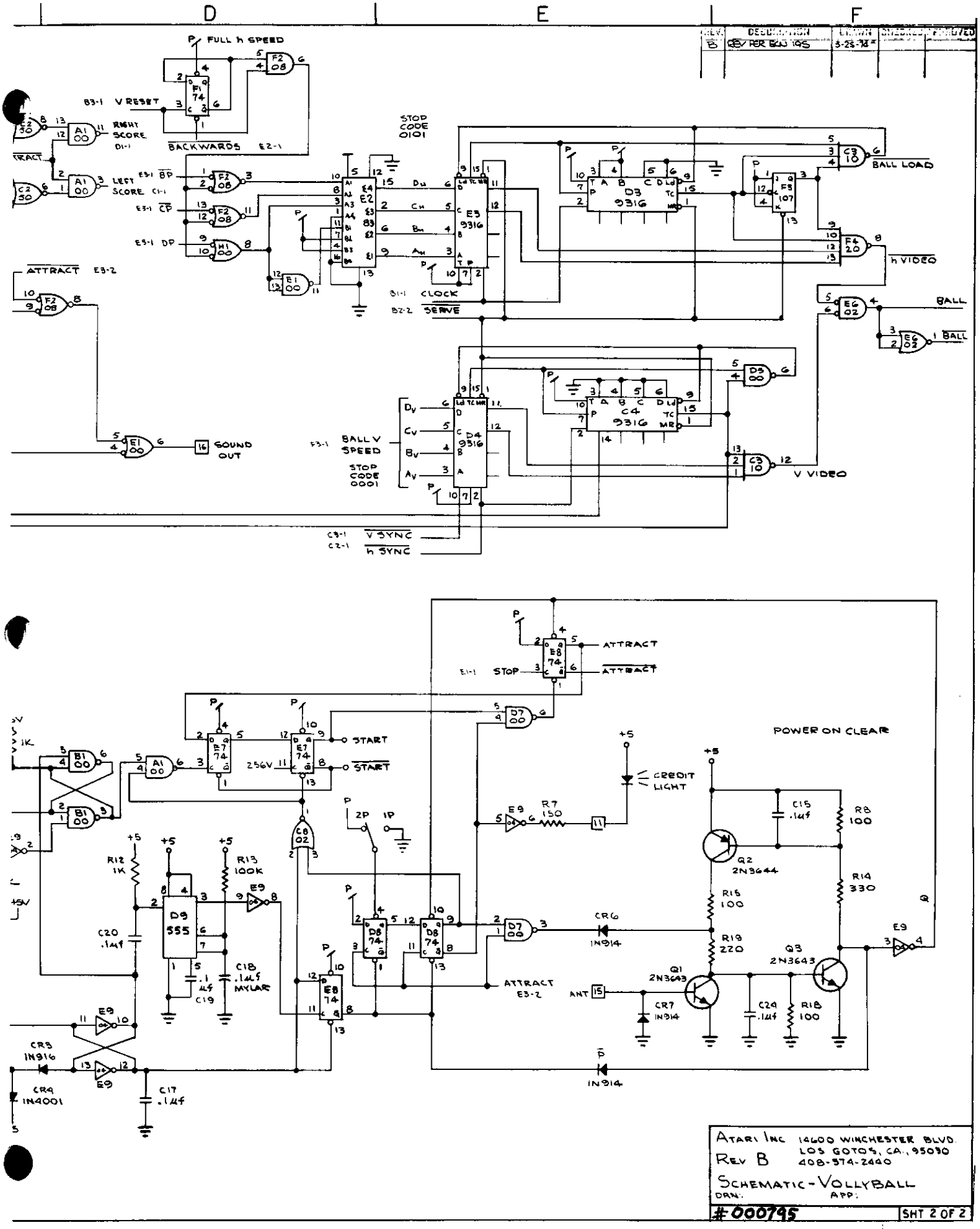


Figure 2-21. Computer Board Schematic, Revision B (Sheet 2)

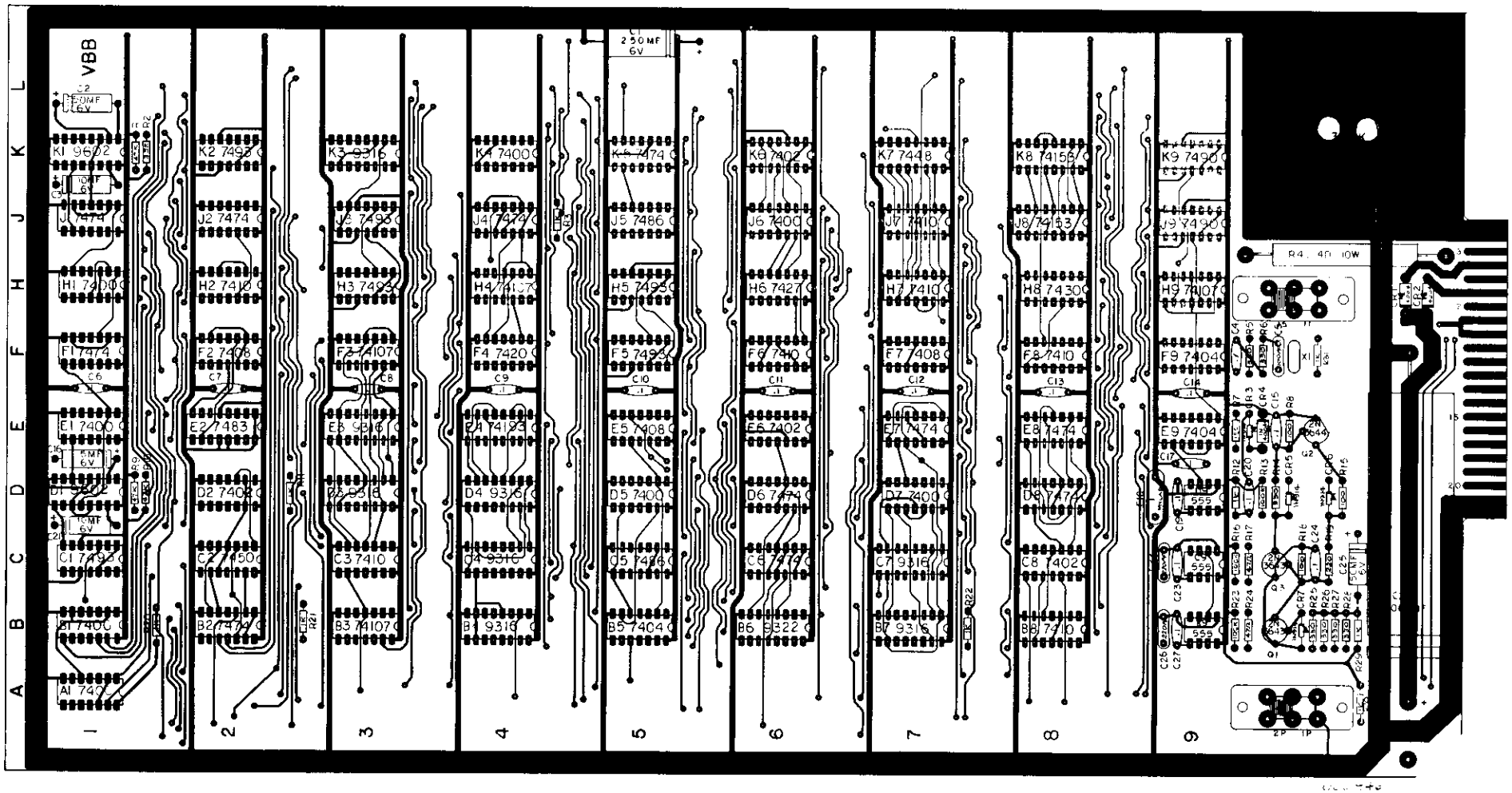


Figure 2-20. Computer Board Parts Layout