07- Pete Gervarc

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DOC. REV.	DEVICE REV.	COMMENTS	DATE	LOGIC ENGINEERING	
A	C	See page 2		C.A.D. ENGINEERING	
				TEST ENGINEERING	
				ORIGINATING DIVISION	
				DIVISION APPROVAL	

ATARI®
Semiconductor Group

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DEVICE NAME
FGTIA

DOCUMENT NUMBER
D020120

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REVISIONS

The FGTIA was changed from device REV B to device REV C in order to incorporate changes to the color generation circuitry. The audio phase locked loop circuitry was eliminated in order to add two additional color control outputs, LOCK and DICA. Additional changes have been made in the function of the color outputs during the horizontal and vertical I.D. times. The timing characteristics for the color outputs have also been changed.

This specification was changed from document REC N/C to document REV A in order to reflect these changes.

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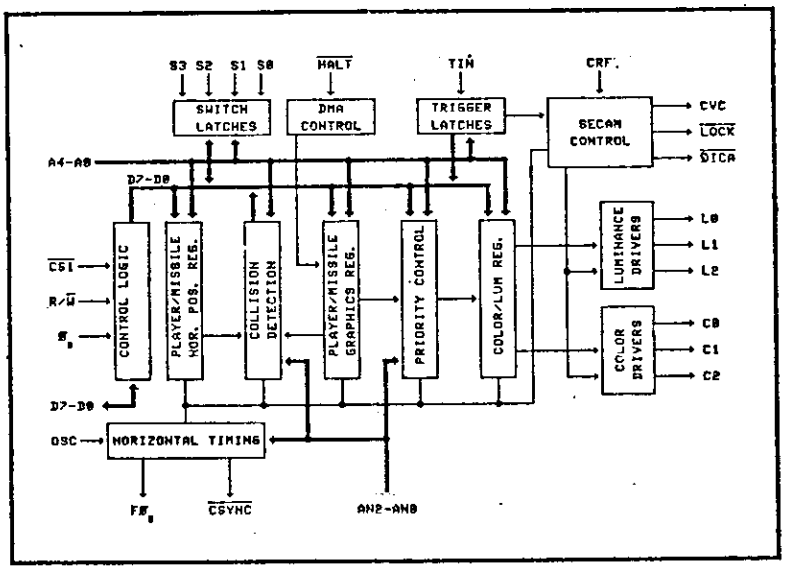
General Description

The FGTIA is an NMOS custom circuit designed to generate player/missile graphics for display on a SECAM television system. The FGTIA converts graphics data into composite sunc, luminance and chrominance information signals required by a television R.F. modulator. The FGTIA also provides four-bits of input from the joystick controllers and four-bits of general purpose I/O.

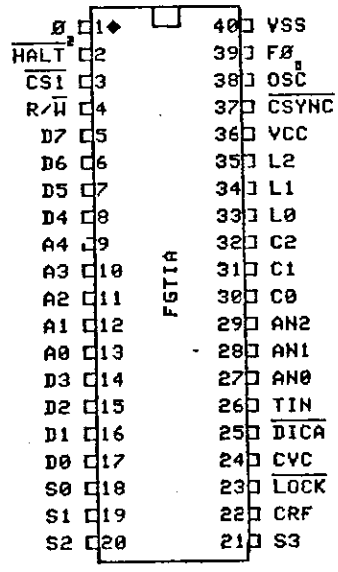
Features

- Player/Missile Graphics Generation
- Direct Memory Access of Player/Missile Graphics Information
- Priority Control Circuitry
- Video Signal Generation Circuitry

Block Diagram



Pin Assignment



Pin Description

Pin Name	Type	Pin No.	Function
$\phi 2$	I	1	Phase two microprocessor clock from the 6502 MPU. Phase two is used to synchronize data transfers between the FGTIA and microprocessor.
$\overline{\text{HALT}}$	I	2	Active low input control signal which is used to synchronize the FGTIA with ANTIC during player/missile DMA.
$\overline{\text{CSI}}$	I	3	Active low input signal which is used to enable data transfers to and from the FGTIA.
R/$\overline{\text{W}}$	I	4	Input/output control signal which controls the direction of data transfers between the FGTIA and microprocessor. When high, data is transferred from the FGTIA to the microprocessor. When low, data is transferred from the microprocessor to the FGTIA.
D7-D0	I/O	5-8 14-17	Data I/O lines which are used to transfer data to and from the FGTIA.
A4-A0	I	9-13	Address bus lines which are used to select one of the internal registers of the FGTIA.
S3-S0	I/O	18-21	Switch I/O lines which are used for general purpose I/O functions.
C_{RF}	I	22	Color phase locked loop frequency input--The input signal on this line is compared against a constant frequency reference in order to generate an error output voltage.
$\overline{\text{LOCK}}$	O	23	Active low output signal which is used to synchronize the external color frequency generation circuitry.

Pin Description (cont'd)

Pin Name	Type	Pin No.	Function
C_{VC}	O	24	Color phase locked loop error voltage output--This line outputs a voltage high level if the frequency and phase of the C_{RF} signal is greater than that of the color PLL reference signal. If the frequency and phase of the C_{RF} signal is less than that of the reference signal, a low voltage level is output. The C_{VC} line will go into a high impedance state if the input and reference signals are equal in frequency and phase.
$\overline{DICA}$	O	25	Active low output signal which is used to synchronize the external color frequency generation circuitry.
T_{IN}	I	26	Serial data input which is used to input data from the joystick controllers. One bit of data is also input to select between positive or negative video modulation.
AN2-AN0	I	27-29	ANTIC interface lines which are used to transmit playfield, blank, and vertical sync data to the FGTIA.
C2-C0	O	30-32	Color output lines which are used to generate video color frequencies.
L2-L0	O	33-35	Luminance output lines which are used to generate video luminance levels.
V_{CC}	I	36	Positive voltage power supply-- Typically +5.0 volts.
$\overline{CSYNC}$	O	37	Composite sync output which is used to generate vertical and horizontal sync pulses.
OSC	I	38	Master clock input--Typically 3.5625 MHz.

Pin Description (cont'd)

Pin Name	Type	Pin No.	Function
Fϕ	O	39	Fast phase zero output clock which is a buffered version of the OSC input. The Fϕ output is used to drive ANTIC.
V_{SS}	I	40	Power supply ground.

Key to Pin Types:

I=Input
O=Output
I/O=Input/Output

Introduction

The FGTIA is a custom NMOS LSI device that is capable of accessing player/missile graphics data stored in system memory and generating luminance, chroma, and sync signals necessary for interfacing to a SECAM video standard television. The FGTIA is software compatible with the NTSC and PAL versions of the GTIA.

FGTIA FUNCTIONAL DESCRIPTION

Graphics are divided into two basic categories: playfield graphics and player/missile graphics. ANTIC has direct control over all playfield graphics. The playfield is generally used for inanimate objects, however, playfield animation is possible. The FGTIA has direct control over player/missile graphics, with the exception that ANTIC provides the addresses for graphics stored in system memory when using player/missile DMA. Player/missile graphics are generally used to provide animation for objects that move on the screen.

1.0) Television Frame Timing

In order to understand how the FGTIA works, it is necessary to understand how a television works. An electron beam is generated at the rear of the television tube and shoots toward the television screen in the front. Along the way, it passes through a set of horizontal and vertical coils which, if energized, can deflect the beam. In this way the beam can be made to strike any point on the television screen. The electronics in the television set cause the beam to sweep across the television screen in a regular fashion. The beam's intensity can also be controlled. If the beam is intense, the spot on the screen will glow brightly. If the beam is less intense, the spot will glow dimly or not at all.

The beam starts at the top-left corner of the screen and traces horizontally across the screen. As it sweeps across the screen, its intensity paints an image on the screen. When the beam reaches the right edge of the screen, it is turned off and brought back to the left side of the screen and down just a little. The beam is turned on again and starts back across the screen. In SECAM systems, this process is repeated for 312½ sweeps across the screen. These 312½ lines fill the screen from top to bottom to make a complete field. At the bottom of the screen (after line 312½), the beam is turned off and returned to the top-left corner of the screen. This process happens 50 times every second. Since the picture is drawn so fast, the eye does not notice that the television picture is being drawn one line at a time. All televisions use a technique called "interlacing." This technique increases the vertical resolution by drawing half of the television picture in the first 312½ lines and the second half of the picture in the second 312½ lines. The second half of the picture is moved down by one half of a scan line so the two picture halves are not displayed on top of each other. The FGTIA does not do interlacing so the picture is defined by one field, not two interleaved fields per frame as in conventional TV broadcast pictures.

1.0) Television Frame Timing (cont'd)

Terminology--A single trace of the beam across the screen is referred to as a "horizontal scan line." A horizontal scan line is the fundamental unit of measurement of vertical distance on the screen. The height of an image is stated by specifying the number of horizontal scan lines it spans. The period during which the beam returns from the right edge of the screen to the left side is referred to as "horizontal blank." The period during which the beam returns from the bottom-right edge of the screen to the top-left is referred to as "vertical blank." The entire process of drawing a screen takes 20,000 microseconds. The vertical blank period is about 1,408 microseconds. The horizontal blank period is about 11.22 microseconds. A single horizontal scan line takes approximately 64 microseconds (this includes the horizontal blank time).

Most television sets are designed with "overscan." This means that the television picture is spread out so the picture edges are off the edge of the television tube. This guarantees that there will not be any unsightly borders in the television picture. For this reason the picture must be somewhat smaller than the television can theoretically display. This overscan can vary from television to television. In SECAM systems a good limit of vertical resolution to use is 228 horizontal scan lines.

The standard unit of horizontal distance is the "color clock." The width of an image is specified by stating how many color clocks wide it is. There are a total of 228 color clocks in a single horizontal scan line. Only 160 of these are actually visible due to horizontal blank and horizontal overscan. It is possible with the FGTIA to go even finer and control individual half clocks. This gives double the horizontal resolution or 320 visible picture elements. A picture element, either vertical or horizontal, is referred to as a "pixel." The maximum visible resolution of a television picture using the FGTIA is 320 pixels horizontally by 228 pixels vertically. Figure 1 illustrates the screen format as generated by the FGTIA.

NOTE: The FGTIA has been designed to interface with the PAL video standard version of ANTIC, device numbers C014887 and C021698. For additional details on screen format and the differences between the NTSC and PAL video standard versions of ANTIC, refer to ASG document number D021698.

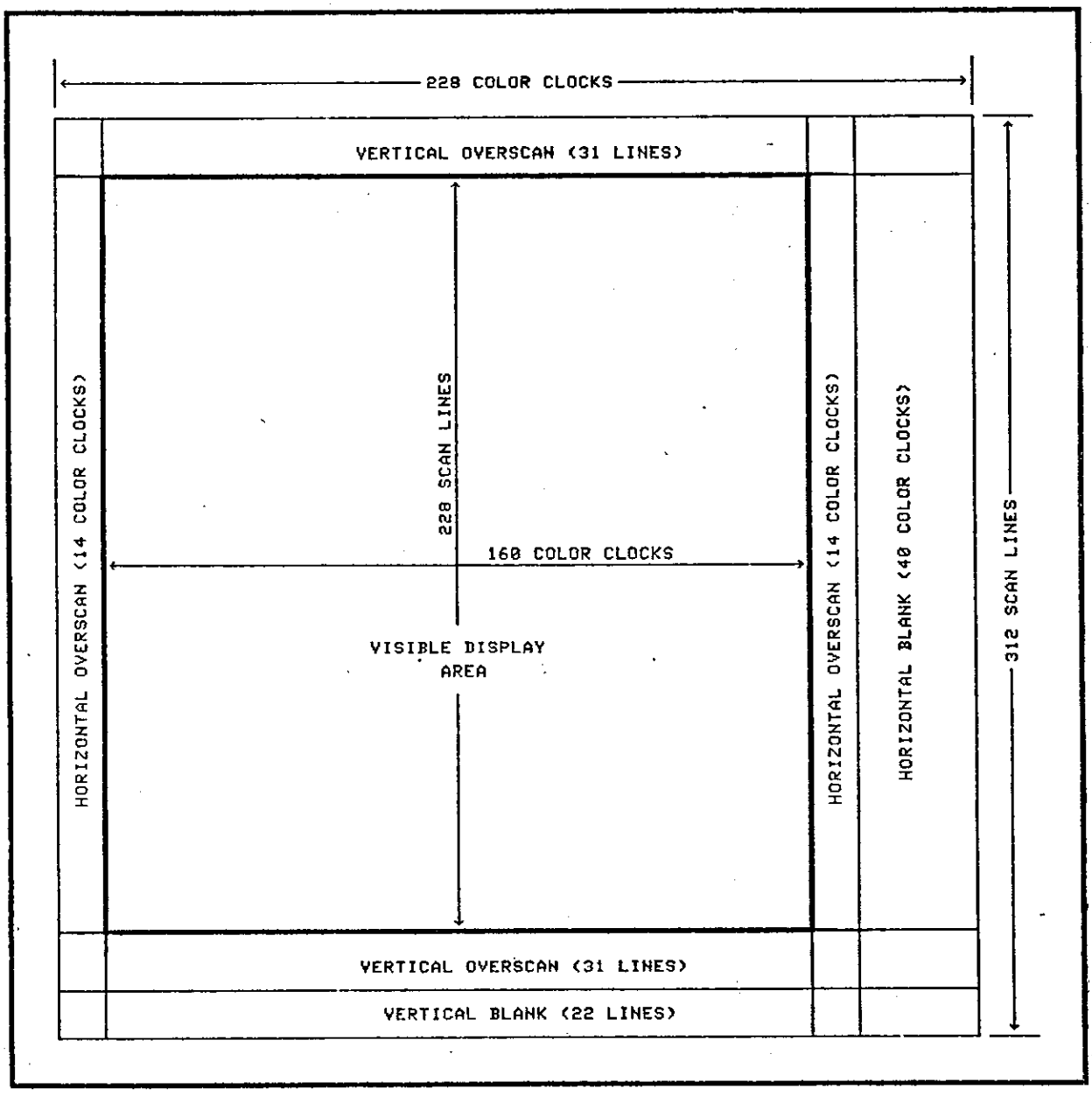


Figure 1) Television Screen Format

2.0) Player/Missile Graphics

The FGTIA is primarily responsible for generating all player/missile graphics. The exception is when player/missile graphics DMA is used. In this case, ANTIC will access the graphics data and signal the FGTIA when the data is to be loaded into its internal graphics registers.

2.1) Player/Missile Graphics Registers

Players and missiles are small objects which are not considered to be part of the playfield. There are four players available on the FGTIA. Each player is associated with its own missle. Players and missiles are created from data bits stored in individual graphics registers. Each player is eight bits wide and has its own eight-bit graphics register. Each missile is two bits wide and shares a graphics register with the other three missiles. Player/missile graphics registers are usually changed during the horizontal and vertical blank periods to avoid unwanted glitches on the TV screen. Each player/missile pixel is normally equal to one color clock horizontally by one TV scan line vertically. The width and height of each pixel can be changed by setting bits in the player/missile size registers and DMA control register. By changing bits in the player/missile size registers, each player/missile pixel can be changed from one color clock wide horizontally to two or four. By changing bit D4 of the DMACTL register on ANTIC from a one to a zero, all player/missile pixels can be changed from one line to two line vertical resolution.

The same player/missile data will be displayed every TV scan line unless the player/missile graphics register data is changed. This will tend to create bands or strips that extend from the top to the bottom of the screen at the horizontal position of each player and missile. If players and missiles are not used, the player/missile graphics registers should be loaded with all zeros. This will keep the player missile bands from appearing on the screen. The horizontal position registers can also be loaded with a value that is off of the screen.

2.2) Player/Missile Color/Lum Registers

Players and missiles get their color and luminance from their corresponding color/lum registers. There are four bits which are used to indicate which color is to be used, and three bits which are used to indicate which luminance value is to be used. This allows a player/missile pair to be one of sixteen different colors with up to eight luminance values for each color. It should be noted that a player and its corresponding missile use the same color/lum register.

2.3) Player/Missile Horizontal Position

Players and missiles have their own 8-bit horizontal position register. Position register value 30 (HEX) is the left edge of a standard width playfield screen and D0 (HEX) is the right edge. When the horizontal counter value equals a player or missile's horizontal position register value, the graphics information in the corresponding graphics register is "added" to the playfield information.

2.4) Graphics Data Priority

Since playfield and player/missile graphics are created seperatley, they must be combined before they can be displayed on the television screen. This is accomplished by establishing priorities between the different graphics objects. The FGTIA determines graphics priority by using the information stored in the priority control register. Bits D3-D0 are used to assign priorities to all graphics objects. The use of the priority control bits is a non-exclusive function. This means that no two priority bits (D3-D0) should be equal to one. If this happens, object priorities will be in conflict and the overlapping pixels will be of indeterminate color and luminance. There are four different sets of object priorities. When the fifth player is used (see section 2.5), the playfield 3 color/lum register is used to give the player its color. The fifth player will not have priority over playfield 3 objects. This means that if the fifth player is used and is positioned over a playfield 3 object, the overlapping pixels will blend together. For more information on the use of the priority bits, refer to the register description section of this specification.

2.5) Using Missiles As a Fifth Player

All missiles can be combined into a fifth player by setting bit D4 of the priority control register to a one. The fifth player gets its color and luminance from playfield 3 color/lum register. This means that if the fifth player is positioned over a playfield 3 pixel, the player and playfield pixels will merge together and portions or all of the player will appear to disappear. The fifth player is moved horizontally on the screen by changing the contents of all four missile horizontal position registers to the same value.

2.6) Multiple Color Players

The FGTIA has the ability to display players and missiles that overlap on the screen with a third color in the overlapping region. Multiple color players and missiles are enabled by setting bit D5 in the priority control register to a one. Any time a player/missile 0 pixel overlaps a player/missile 1 pixel, the pixel color and luminance will be the result of the logical OR of the corresponding color/lum registers. Likewise, any overlapping player/missile 2 and player/missile 3 pixels will have their color/lum register bits logically ORed.

2.7) Object Collisions

In order to determine if there has been a collision (overlap) between objects, the FGTIA provides 60 bits of data to detect and store overlap conditions between players, missiles and playfield. These bits can be read at any time. Collision detection bits are provided for player to player collisions, player to missile collisions, player to playfield collisions and missile to playfield collisions. There is no provision for playfield to playfield collision since this condition can not exist (except when using the fifth player, in which case fifth player collisions with playfield are not recorded). The FGTIA does not provide detection for missile to missile collisions

2.7) Object Collisions (cont'd)

In character graphics modes 2 and 3 and bit map graphics mode F, the pixel colors are generated by using color bits (D7-D4) of the playfield 2 color/lum register and the luminance bits (D3-D1) of the playfield 1 and playfield 2 color/lum register. In this case, object collisions are read as a playfield 2 collision.

2.8) Creating Players and Missiles by Using DMA

Players and missiles can be created by using direct memory access. This allows player/missile graphics for every TV scan line to be stored in system memory and loaded into the player/missile graphics registers automatically. In order to use player/missile DMA, the graphics data must first be stored in memory. The player/missile base address register (PMBASE) on ANTIC is used to specify the most significant 5 or 6 bits of the address where the player/missile graphics data is stored in memory. The remaining 10 or 11 bits are automatically calculated by ANTIC. Player/missile graphics can be displayed with either one line or two line resolution. Two line resolution means that the same graphics data is used for two TV scan lines. 640 (decimal) bytes (5 X 128) are required for two line resolution and 1280 bytes (5 X 256) bytes are required for one line resolution.

Once the player/missile graphics data has been stored in memory, player/missile DMA has to be enabled. This is accomplished by setting bits D3 and D2 of the DMACTL register on ANTIC, and bits D1 and D0 of the GRACTL register on the FGTIA, to ones. When using two line player/missile DMA, each player or missile can be delayed by one TV scan line. The VDELAY register is used to give one line resolution in the vertical positioning of a player or missile when two line resolution is used. Setting a bit in the VDELAY register to a one will move the corresponding player or missile down by one TV scan line. The vertical delay function can only be used when player/missile DMA and two line player/missile resolution are enabled.

3.0) Miscellaneous Functions

3.1) Special Graphics Functions--(GTIA Modes)

The FGTIA provides three expanded graphics modes. These modes are intended to be used in conjunction with ANTIC bit map graphics mode F. The special graphics modes are enabled by setting certain bits in the priority control register (PRIOR). Priority control register bits D7 and D6 select one of the three special playfield graphics modes plus the standard CTIA playfield mode. These playfield modes are selected as follows:

Priority Control Register Bits		Mode Select
D7	D6	
0	0	Standard CTIA Mode (4 Colors-4 Luminances)
0	1	GTIA Mode 1 (1 Color-8 Luminances)
1	0	GTIA Mode 2 (9 Colors-9 Luminances)
1	1	GTIA Mode 3 (16 Colors-1 Luminance)

When the priority control register bits D7 and D6 are set for the standard CTIA mode, the FGTIA uses the four playfield color/lum registers and the background color/lum register to generate standard playfield graphics on the screen. In the GTIA graphics modes (ANTIC display instruction mode F and PRIOR bits D7,D6 $\neq$ 0,0), each pixel is equal to two color clocks horizontally by one TV scan line vertically. There are 80 pixels per standard mode line with each pixel defined by four data bits. This means that 40 bytes of graphics data are required to define a standard width mode line. The pixel can assume a variety of colors and luminances depending of the GTIA graphics mode chosen.

GTIA Mode 1 (1 Color-8 Lums)--In GTIA mode 1, the graphics data bits are used to select one of eight different luminance values. Each pixel takes its color from the background color/lum register. The luminance value selected by the pixel data bits is logically "ORed" with the luminance bits of the background color/lum register. In this mode, COLBK register bits D3-D1 should be set to zero (COLBK bit D0 is always equal to 0).

Note: The FGTIA does not have four luminance output lines as do the NTSC and PAL versions of the GTIA. This means that the FGTIA is not compatible with its NTSC and PAL counterparts when GTIA graphics mode 1 is to be used.

3.1) Special Graphics Functions--(GTIA Modes) cont'd

GTIA Mode 2 (9 Colors-9 Lums)--In GTIA mode 2, the graphics data bits are used to select one of the nine color/lum registers on the FGTIA. The color registers are selected as follows:

Pixel Data Bits (Binary)	Color Register Selected
0 0 0 0	COLPM0
0 0 0 1	COLPM1
0 0 1 0	COLPM2
0 0 1 1	COLPM3
X 1 0 0	COLPF0
X 1 0 1	COLPF1
X 1 1 0	COLPF2
X 1 1 1	COLPF3
1 0 X X	COLBK

X=don't care

GTIA Mode 3 (16 Colors-1 Lum)--In GTIA mode 3, the graphics data bits are used to select one of sixteen different color values. Each pixel takes its luminance from the background color/lum register. The color value selected by the pixel data bits is logically "ORed" with the color bits of the COLBK color/lum register. In this mode, COLBK register bits D7-D4 should be set to zero.

3.2) Input/Output Functions

The FGTIA has a serial input port for inputting data from the joystick controller trigger buttons and a four-bit general purpose I/O port. Data inputs on the trigger port can be latched by setting a bit in the graphics control register. The trigger inputs will remain latched until the latch enable bit in the graphics control register is reset. The switch I/O port is capable of data input and output. The switch lines are programmed to be either inputs or outputs by writing to the switch I/O output register.

3.3) Determining The Television Video Standard

The PAL register is used to determine which version of the GTIA is being used. If the PAL register value is equal to 0F (HEX), the NTSC video version of the GTIA is being used. If the PAL register value is equal to 01 (HEX), the PAL or SECAM video version of the GTIA is being used. The PAL register is provided so that software can make the necessary program adjustments. Note that there is no distinction between the PAL and SECAM versions of the GTIA.

4.0) Video Generation

The FGTIA is designed to generate color and luminance, as well as, horizontal and vertical sync signals for a SECAM video standard television system. The following sections describe how these signals are generated.

4.1) SECAM Fundamentals

The existing monochrome television standards provided a foundation upon which to build the necessary innovative color television techniques while simultaneously inposing the requirement of compatibility. Within this framework, an underlying theme--that which the eye does not see does not need to be transmitted nor reproduced--set the stage for a variety of facinating developments in what has been characterized as an "economy of representation."[1]

The NTSC transmission standard was the first color video transmission standard developed and approved for public use. These transmission standards are primarily used in the United States, Canada, Japan and Mexico. The contries of Europe delayed the adoption of a color television system primarily because the technology necessary to implement some of the NTSC requirements was still in its infancy. Thus, many of the differences the NTSC and other systems are due to technological rather than fundamental theoretical considerations.[2]

An early system that received approval was one proposed by Henri de France of Paris. It was argued that if color could be relatively band limited in the horizontal direction, it could also be band limited in the vertical direction. Thus the necessary two pieces of coloring information could be transmitted as subcarrier modulation that is sequentailly transmitted on alternate lines--thereby avoiding the possibility of unwanted crosstalk between color signal components. Thus, at the receiver, a one line memory, commonly referred to as 1-H delay element, must be employed to store one line and then be concurrent with the following line. Then a linear matrix of the red and blue signal components is used to produce the third green component. Of course, this necessitates the addition of a line switching identification technique. Such an approch, designated as sequential color signal plus a memory--"sequential à mémoire" (SECAM), was developed and offically adopted by France and the USSR.[2]

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1. Pritchard, D.H., "U.S. Color Television Fundamentals--A Review," J. SMPTE (Nov. 1977).

2. Gibson, J.J. and Pritchard, D.H., "Worldwide Color TV Standards--Similarities and Differences," RCA Engineer (25-5, Feb./Mar. 1980)

4.1) SECAM Fundamentals (cont'd)

The SECAM method has several features in common with NTSC, such as the same luminance signal (Y) and the same color difference signals (R-Y) and (B-Y). However, this approch differs considerably from NTSC and even PAL in the manner in which the color information is modulated onto the subcarrier(s).

First, the R-Y and B-Y color difference signals are transmitted alternately in time sequence from one successive line to the next--the luminance signal being common to every line. Second, the R-Y and B-Y color information is conveyed by frequency modulation of different subcarriers. Thus, at the decoder, a 1-H delay element, switched in time synchronization with the line switching process at the encoder, is required in order to have simultaneous existance by B-Y and R-Y signals in a linear matrix to form the G-Y component.

As in PAL, the SECAM system must provide some means for identifying the line switching sequence between the encoding and decoding processes. This is accomplished by introducing alternate red and blue color identifying signals during the vertical blank period just after vertical sync. Also during horizontal blank, the subcarriers are blanked and a burst of F_{or}/F_{ob} (zero color frequencies) is inserted and used as a grey level reference for the FM discriminators to establish their proper operation at the beginning of each line.

Thus, the SECAM system is a line sequential color approch using frequency modulated subcarriers. A special identification signal is provided to identify the line switch sequence and is especially adapted to the 625 line/50 field wideband systems available in France and the USSR.

4.2) Monochrome Signal

As mentioned in the previous section, all televisions, regardless of the video standard used, create a picture on the TV screen in much the same way. The color video signal is composed of two primary analog signals: monochrome (luminance) and chroma. The most important portion of the video signal is the monochrome or luminance signal, which represents the picture brightness and detail. This signal is further subdivided into the active display and the horizontal and vertical blank periods. The luminance signal for the active display portion of the display is derived from the luminance bits D3-D1 of the FGTIA color/lum registers (or from the display data when in GTIA mode 1). The luminance signal is responsible for determining the brightness of the pixels or dots on the TV screen. The higher the binary luminance value, the brighter the dot on the screen. A binary value of all zeros will cause the electron beam to be turned off. This condition is more commonly called a "blank" or "blacker than black" level. A binary value of all ones will cause the electron beam to glow at its brightest. This condition is more commonly called a "white level." As the electron beam sweeps across the screen, the luminance level is constantly changing to reflect the luminance values of the graphics data stored in memory.

4.2) Monochrome Signal (cont'd)

Horizontal Blank and Horizontal Sync--In order to create a television picture by the scanning method described in section 1.0, the electron beam must be returned from the right edge of the screen to the left edge of the screen in a periodic fashion. The horizontal sync signal causes the horizontal deflection coils to return the electron beam to the left edge of the screen. The horizontal sync pulse is generated in a section of the video signal known as "horizontal blank." The horizontal blank period is divided into three parts, front porch, sync, and the back porch or horizontal retrace. The front porch is the period where the electron beam is first turned off before the sync pulse is generated. This ensures that the beam will not be seen as it is moved back across the screen. The sync period is the time during which the horizontal sync output level is generated. The sync voltage level causes the horizontal deflection coils to reposition the electron beam at the left edge of the screen. The back porch is the period during which the electron beam is actually being moved from the right edge of the screen to the left edge.

The process of horizontal blank takes exactly 40 color clocks on the FGTIA. The time period is broken down as follows:

Front Porch = 5½ color clocks*
Horizontal Sync = 16 color clocks*
Back Porch = 18½ color clocks*

Horizontal Blank Total = 40 color clocks or
= 11.23 uS

*Referenced to the color output lines (C2-C0)

Vertical Blank and Vertical Sync--The vertical blank period is the time during which the electron beam is returned from the bottom-right of the screen to the top-left. As with horizontal blank, the vertical blank period is also divided into three parts, blank, sync, and vertical retrace. The blank period is the time during which the electron beam is first turned off before the vertical sync pulse is generated. This ensures that the beam will not be seen as it is moved to the top of the screen. The sync period is the time during which the vertical sync output levels are generated. The sync pulse consists of three horizontal scan lines where the luminance levels are inverted for a normal blank display line. The sync pulse causes the vertical and horizontal deflection coils to return the electron beam to the top-left corner of the screen. The vertical retrace period is the time during which the electron beam is actually being moved from the bottom-right to the top-left of the screen.

4.3) Chrominance Signal

In order to add color to objects displayed on the screen, a color signal must be added to the monochrome video output signal. As described in the previous sections, SECAM systems transmit the color difference signals alternately in time sequence from one successive line to the next. The lines in which the R-Y infromation is transmitted are referred to as red lines.

4.3) Chrominance Signal (cont'd)

The lines in which the B-Y information is transmitted are referred to as blue lines. Since SECAM color is a frequency modulated signal, each color defined by the contents of the color/lum registers on the FGTIA corresponds to a certain color frequency. Table 1 shows the FGTIA color line (C2-C0) output codes for both red and blue TV lines.

Table 1) Color Output Codes

Color/Lum Register Bits				SECAM Color	Red Line Output Frequency	Blue Line Output Frequency
D7	D6	D5	D4			
0	0	0	0	Gray	CM3	CM5
0	0	0	1	Light Orange	CM4	CM7
0	0	1	0	Orange	CM5	CM7
0	0	1	1	Red-Orange	CM5	CM6
0	1	0	0	Pink	CM6	CM6
0	1	0	1	Purple	CM6	CM5
0	1	1	0	Purple-Blue	CM5	CM4
0	1	1	1	Blue	CM4	CM4
1	0	0	0	Blue	CM3	CM3
1	0	0	1	Light Blue	CM2	CM3
1	0	1	0	Turquoise	CM2	CM4
1	0	1	1	Green-Blue	CM2	CM5
1	1	0	0	Green	CM1	CM7
1	1	0	1	Yellow-Green	CM2	CM7
1	1	1	0	Orange-Green	CM3	CM7
1	1	1	1	Light Orange	CM4	CM7

FGTIA Color Line to Color Output Frequency Conversions

C2	C1	C0	Color Frequency #	Approx. Frequency	Standard
1	1	1	CM1	4700 KHz	4.756 MHz
1	1	0	CM2	4500 KHz	
1	0	1	CM3	4400 KHz	4.40625 MHz
1	0	0	CM4	4300 KHz	
0	1	1	CM5	4200 KHz	4.25 MHz
0	1	0	CM6	4100 KHz	
0	0	1	CM7	4000 KHz	
0	0	0	CM8	3900 KHz	3.9 MHz

4.4) Color Phase Locked Loop

In order to generate accurate color reference frequencies during the horizontal blank period of each scan line, a phase locked loop circuit (PLL) is necessary. The PLL compares a prescaled input frequency (C_{RF}) to a prescaled reference frequency (OSC) and produces an error voltage output (C_{VC}). The PLL measures changes in phase as well as frequency, however, in this case the phase relationship is not critical. The operation of the PLL can best be understood by studying a closed loop situation. Refer to figure 2 for the following explaination: The main purpose of having the PLL on the FGTIA is to produce a frequency of 4.453125 MHz during the horizontal blank period. This frequency is approximately equal to the center frequency of the red line chrominance sub-carrier. The OSC input frequency (point 1) is divided down to provide a frequency at the PLL input (point 2) which is equal to the OSC input frequency divided by 4. Likewise, the C_{RF} input frequency (point 3) is divided down to provide a frequency at the input of the PLL (point 4) which is equal to the C_{RF} input frequency divided by 5. The signal at point 2 is referred to as the reference frequency and is equal to 890,625 Hz (3.5625 MHz/4). The frequency at point 4 is constantly changing and is referred to as the input frequency. The PLL circuitry is constantly comparing the frequency and phase of the reference and input signals. An error voltage is generated at the output of the PLL (point 5) which indicates the relationship between the two input signals. If the input signal at point 3 is at a higher frequency than the input signal at point 2, then the PLL generates a high voltage output at point 5. If the input signal at point 3 is at a lower frequency than the input signal at point 2, then the PLL generates a low voltage output at point 5. If the input signal at point 3 is the same frequency and phase as the input signal at point 2, then the PLL output at point 5 is forced into a high impedance state. To complete the circle, this output voltage is next amplified and input into a voltage controlled oscillator (VCO, point 6). The VCO operates as a voltage to frequency converter. It produces an output frequency of constant voltage from a corresponding input voltage. The frequency output of the VCO is used as the frequency input (point 3) of the PLL and the process starts all over again until the frequency and phase of the two PLL input signals are equal. This condition is more commonly referred to as a "lock" condition.

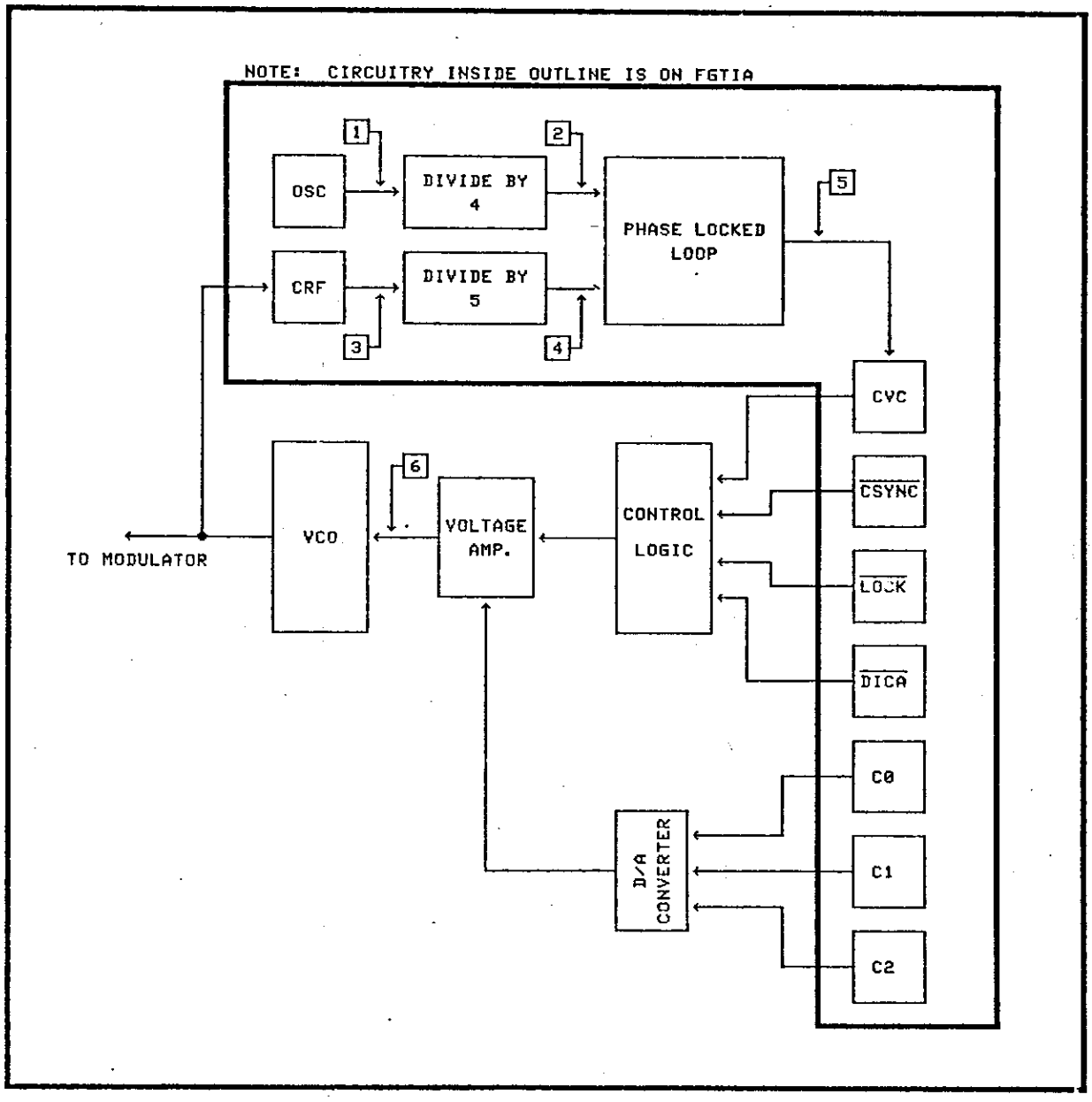


Figure 2) Diagram of a Closed Loop PLL Circuit

4.5) Line Sequence Identification

As discussed earlier, SECAM systems require some type of line identification. The FGTIA provides this by outputting certain color codes during the vertical and horizontal blank periods. During vertical blank and starting with vertical sync, the FGTIA will output 22 scan lines of vertical identification codes. These codes are designated as C2,C1,C0=1,1,1 for red lines and C2,C1,C0=0,0,0 for blue lines. The FGTIA forces the first line starting with vertical sync to be a red line. Figure 3 shows the vertical identification scheme in more detail.

During the horizontal blank period of each scan line, the FGTIA will output horizontal identification codes. These codes are designated as C2,C1,C0=1,0,1 for red lines and C2,C1,C0=0,1,1 for blue lines. These codes represent the zero color or grey level reference for the television's FM discriminators. This helps establish proper operation at the beginning of each line. During the horizontal blank period of each red line, there are two additional output signals generated. These signals are $\overline{\text{DICA}}$ and $\overline{\text{LOCK}}$. These outputs are used to control the external color phase locked loop circuitry. Figure 4 shows the horizontal identification scheme in more detail.

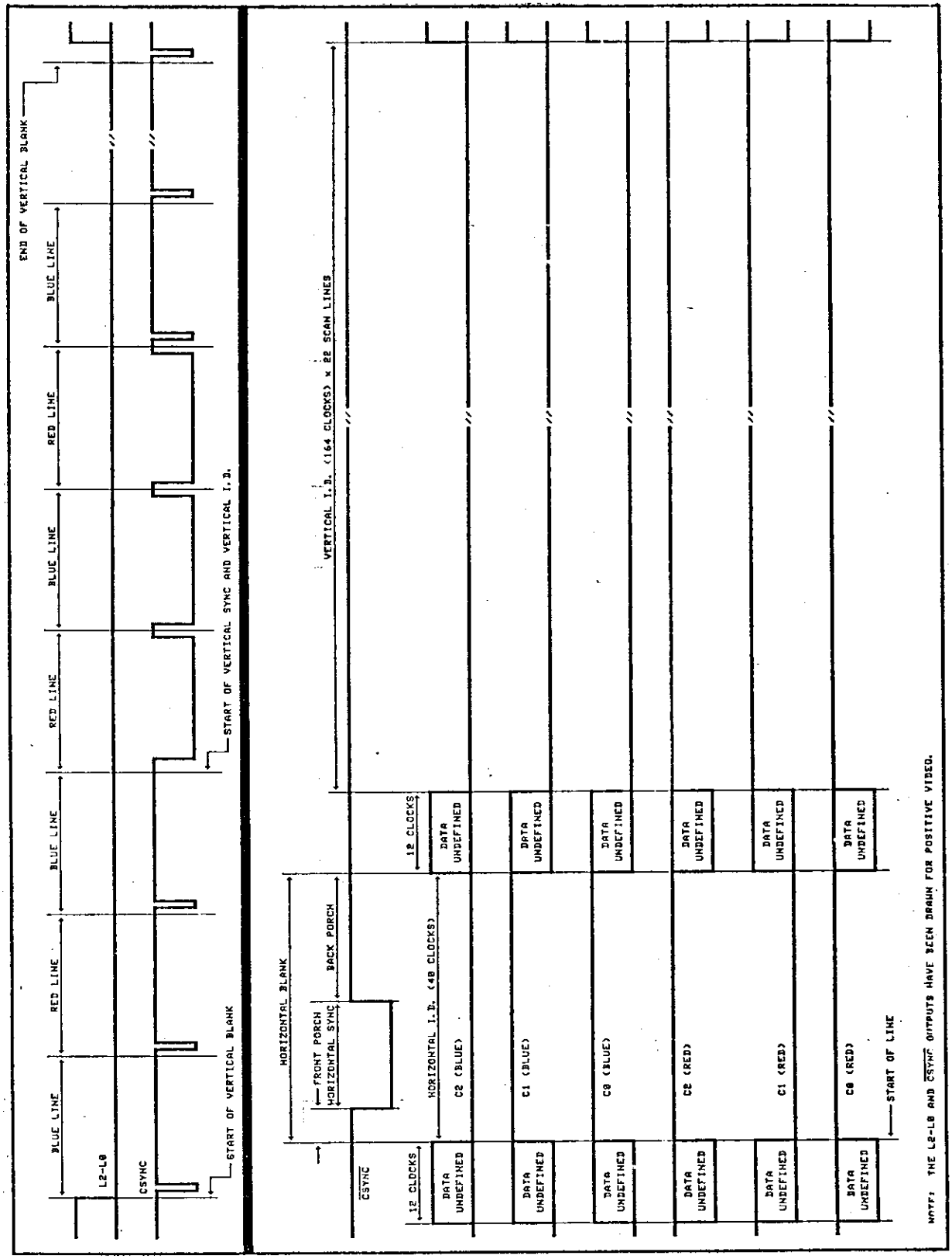


Figure 3) Vertical Identification Timing

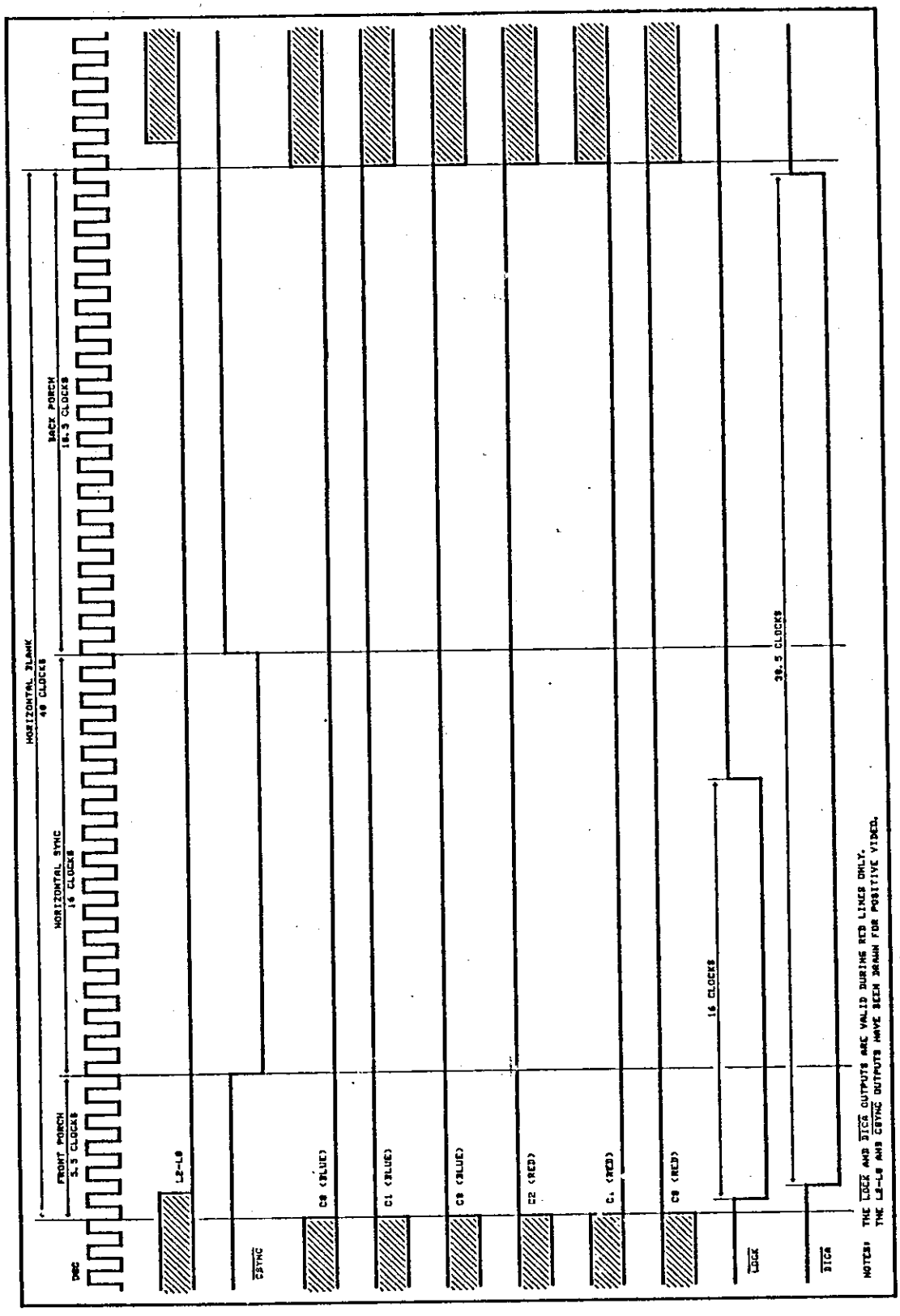


Figure 4) Horizontal Identification Timing

5.0) Interface Circuitry

5.1) Player/Missile DMA

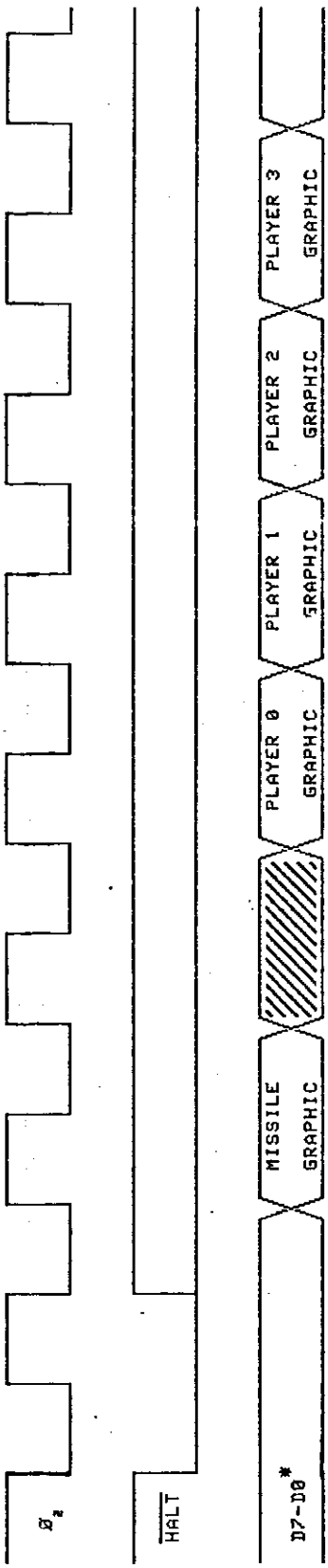
The FGTIA has the ability to access player and missile graphics data directly, through a process known as direct memory access or DMA. Player/missile DMA is enabled by setting bits D1 and D0 of the graphics control (GRACTL) register on the FGTIA and bits D3 and D2 of the DMA control (DMACTL) register on ANTIC. Once DMA is enabled, the player and missile graphics registers will be loaded with the graphics data stored in system memory for display on the next scan line. The FGTIA does not actually address the player/missile data. This is accomplished by ANTIC. The FGTIA only looks for the data on the data bus at specific times. Synchronization between ANTIC and the FGTIA is achieved with the $\overline{\text{HALT}}$ line. When the $\overline{\text{HALT}}$ line goes low during the horizontal blank time, the FGTIA recognizes that the next few $\phi 2$ clock cycles are to be used to fetch the player/missile graphics data (see figure 5 for timing and graphics data input order).

5.2) ANTIC Interface Lines (AN2-AN0)

The AN2-AN0 output lines are used to transmit serialized playfield graphics data as well as blank and vertical sync signals to the FGTIA. This information is transmitted to the FGTIA as outlined below:

All Graphics Modes

AN2	AN1	AN0	
0	0	0	Use COLBK color/lum register for pixel color and luminance.
0	0	1	Output the vertical sync signal.
0	1	0	Output the blank level on L2-L0 and disable ½ clock modes.
0	1	1	Output the blank level on L2-L0 and enable ½ clock modes.



*NOTE: THE FGTIA WILL LOAD DATA INTO THE GRAPHICS REGISTERS AS SHOWN WHEN HALT FIRST GOES FROM HIGH TO LOW DURING HORIZONTAL BLANK.

Figure 5) Player/Missile DMA Timing

5.2) ANTIC Interface Lines (AN2-AN0) cont'd

ANTIC Graphics Modes 4-E

AN2	AN1	AN0	
1	0	0	Use COLPF0 color/lum register for pixel color and luminance.
1	0	1	Use COLPF1 color/lum register for pixel color and luminance.
1	1	0	Use COLPF2 color/lum register for pixel color and luminance.
1	1	1	Use COLPF3 color/lum register for pixel color and luminance.

ANTIC Graphics Modes 2,3 and F

AN2	AN1	AN0	
1	X	X	Use AN1 and AN0 as playfield pixel data bits for ½ color clock graphics modes 2,3 and F. Pixel data bits equal to one will select COLPF1 for pixel luminance. Pixel data bits equal to zero will select COLPF2 for pixel luminance. All pixels use COLPF2 for pixel color (refer to section 3.1 for information on special FGTIA graphics functions).

6.0) General Purpose I/O Functions

6.1) Trigger Input Port (TIN)

In order to accomodate the additional pins required on the FGTIA for the color outputs and PLL, the four trigger lines were combined into one serial input (T_{IN}). The T_{IN} input also provides an additional function. An additional input bit is used to select between positive and negative video outputs on the L2-L0 and $\overline{CSYNC}$ lines. The video select and trigger information are shifted into the T_{IN} input on every occurance of the $\overline{CSYNC}$ output going from low to high. Altogether there are six bits that are shifted into the T_{IN} input. The first bit is used to select the video standard. The second bit is not used. The last four bits are used to input the trigger information from the controllers. The trigger information is input in T0, T1, T2, T3 order. Figure 6 illustrates the parallel to serial conversion of the trigger input data using a 74LS165 8-bit shift register.

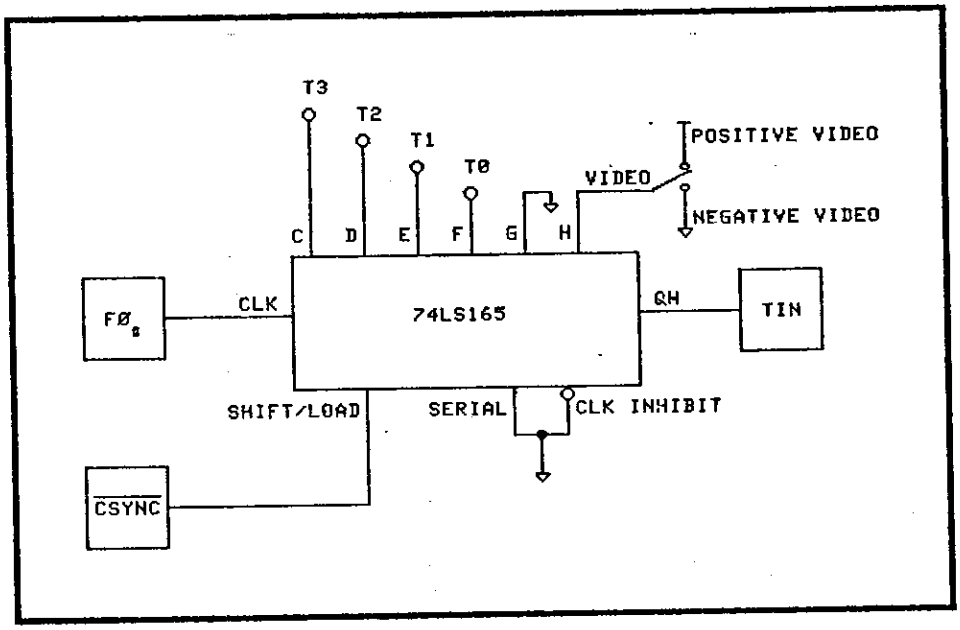


Figure 6) Trigger Data Parallel to Serial Conversion

6.1) Trigger Input Port (TIN) cont'd

The trigger input data can be read at any time just by reading the TRIG0-TRIG3 input registers. These registers are only one-bit wide and show the current status of the corresponding trigger input. The trigger button is considered to have been pressed if the input data is equal to a zero. The trigger inputs can be latched by setting bit D2 in the GRACTL register. When this bit is set to a one, all trigger inputs are latched when they make a transition from high to low. This information remains latched in the trigger input registers until GRACTL bit D2 is reset.

Note: It should be noted that the trigger input data is internally latched for a complete scan line because of the serial to parallel conversion of the data internally by the FGTIA.

6.2) Video Polarity Select

As mentioned in the previous section, the T_{IN} input is used to select the video output polarity. The VIDEO bit is used to select between positive and negative video outputs on the L2-L0 and CSYNC lines. If the VIDEO input bit is zero, the FGTIA will output negative video. If the VIDEO input bit is one, the FGTIA will output positive video. The difference between positive and negative video is that the CSYNC and L2-L0 outputs are logically inverted. Positive video will generate a low or logic 0 horizontal sync pusle and negative video will generate a high or logic 1 horizontal sync pulse.

Note: It should be noted that the function of the T_{IN} input has changed from Rev B to Rev C. The audio PLL has been removed and the audio standards select bit(s) are no longer applicable. It is suggested, however, that the second T_{IN} input bit, which has no use, be input as a logic zero.

6.3) Switch I/O Port (S3-S0)

The Switch I/O lines are used for general purpose I/O functions. The S3-S0 outputs are open-drain outputs and the inputs have internal pull-up resistors to V_{CC}. Figure 7 is a close schematical representation of the S3-S0 I/O port. The output data is latched in the FGTIA by writing to the CONSOL write register. The output of the data latch controls the switch line output transistor. If the output data is a one, the output transistor is turned on and the switch line is grounded. If the output data is a zero, the output transistor is turned off and the switch line is internally pulled-up to V_{CC}. It is important to remember that the data on the switch lines is always the inverse of what is written to the CONSOL register.

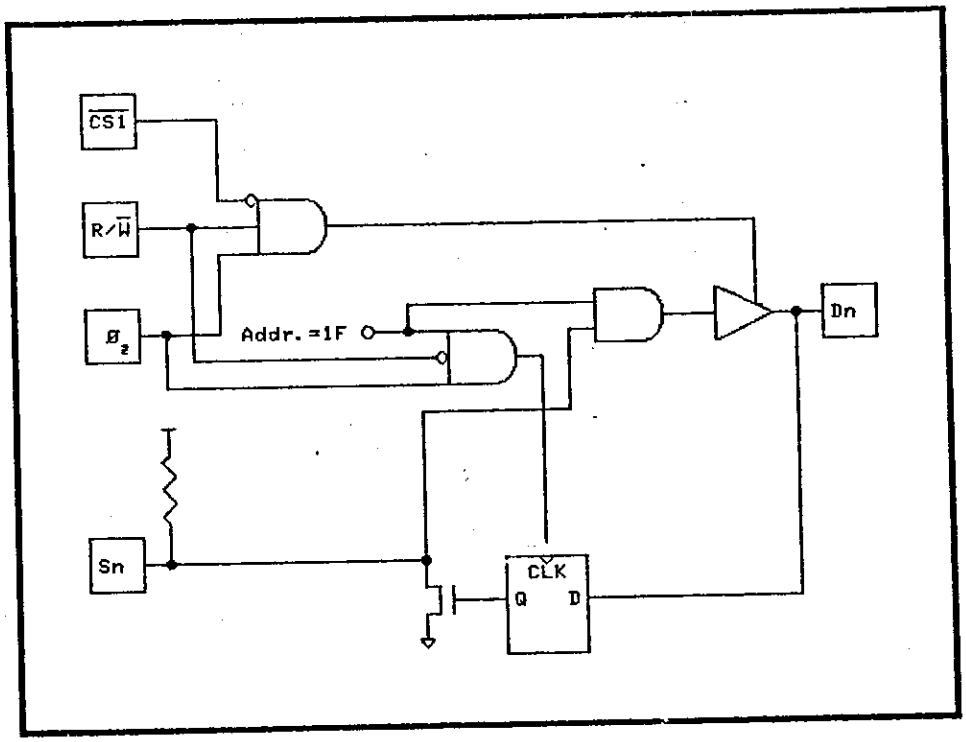


Figure 7) Schematical Representation of the Switch I/O Port

REGISTER DESCRIPTION

There are five address lines on the FGTIA which give it a total of 32 distinct read/write address locations. With the exception of the switch I/O port, all registers are either read-only or write-only address locations. There are a total of 31 write-only registers and only 21 read-only registers leaving 10 read addresses unused.

7.0) Write-Only Registers

The write-only registers control horizontal position, size, graphics and color-luminance for players and missiles as well as color-lum for playfield and background. The following sections explain the write address registers on the FGTIA.

7.1) Player/Missile Horizontal Position

PLAYER HORIZONTAL POSITION:

HPOSP0 (Player 0 position) Addr. = 00
HPOSP1 (Player 1 position) Addr. = 01
HPOSP2 (Player 2 position) Addr. = 02
HPOSP3 (Player 3 position) Addr. = 03

MISSILE HORIZONTAL POSITION:

HPOSM0 (Missile 0 position) Addr. = 04
HPOSM1 (Missile 1 position) Addr. = 05
HPOSP2 (Missile 2 position) Addr. = 06
HPOSM3 (Missile 3 position) Addr. = 07

D7	D6	D5	D4	D3	D2	D1	D0

Players and missiles are small objects which can be moved in the horizontal direction by changing their position registers. The horizontal position value determines the color clock location of the left edge of the object. Hex 30 is the left edge of a standard width screen. Hex D0 is the right edge of a standard screen.

There are a total of four players and four missiles. The four missiles may be combined together and used as a 5th player. The horizontal position registers may be reloaded at any time by the processor, allowing an object to be replicated many times across a horizontal scan line.

7.2) Player/Missile Size

PLAYER SIZE:

SIZEP0 (Player 0 size) Addr. = 08
SIZEP1 (Player 1 size) Addr. = 09
SIZEP2 (Player 2 size) Addr. = 0A
SIZEP3 (Player 3 size) Addr. = 0B

Not Used	D1	D0

0	0 = Normal Size (8 color clocks wide)
0	1 = Twice Normal Size (16 color clocks wide)
1	0 = Normal Size (8 color clocks wide)
1	1 = Four Times Normal Size (32 color clocks wide)

MISSILE SIZE:

SIZEM (All missile sizes) Addr. = 0C

D7	D6	D5	D4	D3	D2	D1	D0
M3		M2		M1		M0	

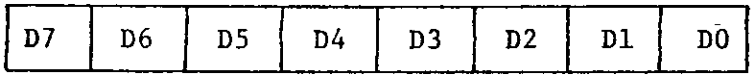
0	0 = Normal Size (2 color clocks wide)
0	1 = Twice Normal Size (4 color clocks wide)
1	0 = Normal Size (2 color clocks wide)
1	1 = Four Times Normal Size (8 color clocks wide)

Each player and missile can be displayed in three different sizes. There is normal, two times normal, and four times normal. Normal size is one color clock per bit in the graphics register.

7.3) Player/Missile Graphics

PLAYER GRAPHICS:

GRAFP0 (Player 0 graphics) Addr. = 0D
GRAFP1 (Player 1 graphics) Addr. = 0E
GRAFP2 (Player 2 graphics) Addr. = 0F
GRAFP3 (Player 3 graphics) Addr. = 10

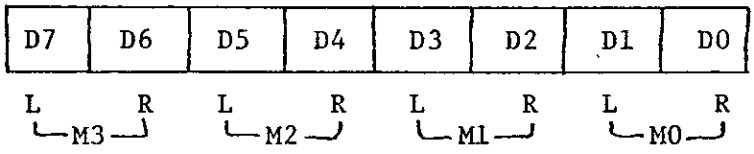


Left Right

Player on T.V. Screen

MISSILE GRAPHICS:

GRAFM (All missile graphics) Addr. = 11



The shape of a player or missile is determined by the data in the graphics register. The players have independent eight bit graphics registers. Each missile is defined by two bits of data which is stored in a register location shared by the other three missiles. These registers may be reloaded at any time by the microprocessor, although they are usually changed during horizontal blank time. The data in these graphics registers is placed on the display whenever the horizontal counter equals the corresponding horizontal position registers. The same data will be displayed every line unless the graphics registers are reloaded with new data. These player/missile graphics registers may also be reloaded automatically from memory with direct memory access (DMA).

7.4) Color-Luminance Control

PLAYER/MISSILE COLOR-LUM:

COLPM0 (Color-lum of player/missile pair 0) Addr. = 12
COLPM1 (Color-lum of player/missile pair 1) Addr. = 13
COLPM2 (Color-lum of player/missile pair 2) Addr. = 14
COLPM3 (Color-lum of player/missile pair 3) Addr. = 15

PLAYFIELD COLOR-LUM:

COLPF0 (Color-lum of playfield 0) Addr. = 16
COLPF1 (Color-lum of playfield 1) Addr. = 17
COLPF2 (Color-lum of playfield 2) Addr. = 18
COLPF3 (Color-lum of playfield 3) Addr. = 19

BACKGROUND COLOR-LUM:

COLBK (Color-lum of backfield) Addr. = 1A

Color				Luminance			
D7	D6	D5	D4	D3	D2	D1	Not Used
X	X	X	X	0	0	0	Zero Luminance (black)
X	X	X	X	0	0	1	
					Etc.		
X	X	X	X	1	1	1	Max. Luminance (white)
0	0	0	0	Grey			
0	0	0	1	Gold			
0	0	1	0	Orange			
0	0	1	1	Red-Orange			
0	1	0	0	Pink			
0	1	0	1	Purple			
0	1	1	0	Purple-Blue			
0	1	1	1	Blue			
1	0	0	0	Blue			
1	0	0	1	Light Blue			
1	0	1	0	Turquoise			
1	0	1	1	Green-Blue			
1	1	0	0	Green			
1	1	0	1	Yellow-Green			
1	1	1	0	Orange-Green			
1	1	1	1	Light Orange			

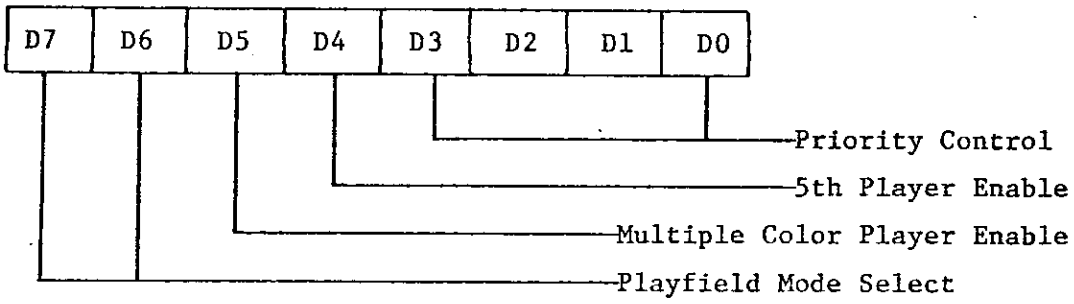
7.4) Color-Luminance Control (cont'd)

A color-luminance register is used on the FGTIA for each player/missile pair and playfield type. Each color-luminance register is loaded by the microprocessor with a code representing the desired color and luminance of its corresponding player/missile or playfield type. As the serial data of the different objects pass through the FGTIA, it gets "impressed" with the color and luminance values in these registers. Therefore, when a player, missile or playfield is turned on, the corresponding color and luminance will be turned on. To prevent a color-luminance conflict, priority is established.

7.5) Priority Control

PRIORITY:

PRIOR (Priority, 5th player, playfield mode) Addr. = 1B



When moving objects such as players, missiles and playfield overlap on the T.V. screen, a decision must be made as to which object shows in front of the other. Objects which appear to pass in front of the other objects are said to have priority over them. Priority is assigned to each object by the FGTIA before the serial data from each object is combined with the other objects and sent out to the T.V. screen. Setting the priority is done by writing to the FGTIA priority control register.

7.5) Priority Control (cont'd)

Priority Select--(Mutually Exclusive)
Bits 0-3 select one of four types of priority. Objects with higher priority will appear to move in front of objects with lower priority.

D3=1	D2=1	D1=1	D0=1
PF0	PF0	P0	P0
PF1	PF1	P1	P1
P0	PF2	PF0	P2
P1	PF3 + P5	PF1	P3
P2	P0	PF2	PF0
P3	P1	PF3 + P5	PF1
PF2	P2	P2	PF2
PF3 + P5	P3	P3	PF3 + P5
BAK	BAK	BAK	BAK

Increasing Priority

Note: The use of priority bits is a "non-exclusive" mode (ie. not more than one bit true at the same time). More than one bit true at any time will result in objects whose priorities are in conflict to turn black in the overlap region.

7.6) Fifth Player Control

The priority control register also controls the fifth player. The fifth player is the combination of all four missiles and is shown as playfield 3 color-lum. However, there is no priority between playfields, therefore, the fifth player would have no priority between playfields. Player/missile combinations are of the same priority.

D4	PRIOR Addr. = 1B

This bit causes all missiles to assume the color of playfield 3. This allows missiles to be positioned together with a common color for use as a fifth player.

7.7) Multiple Color Player Enable

The priority control register also controls multiple color players and missiles. When enabled, the color-lum of player/missile 0 and player/missile 1 is to be logically "ORed." Also the color-lum of player/missile 2 and player/missile 3 are to be logically "ORed." This permits overlapping the position of two players with the choice of a third color in the overlapping region.

D5	PRIOR Addr. = 1B

This bit causes the logical "OR" function of the bits of the colors of player/missile 0 with player/missile 1, and also of player/missile 2 with player/missile 3 when these player/missile pairs are overlapped.

7.8) Playfield Mode Control

Besides priority, fifth player and multiple color player control, the priority control register also controls the playfield data interpretation. There are four playfield modes: They are 4 color-4 luminance (standard mode), 1 color-8 luminance (GTIA mode 1), 9 color-9 luminance (GTIA mode 2), and 16 color-1 luminance (GTIA mode 3).

D7	D6	PRIOR addr. = 1B
0	0	Standard no GTIA mode (4 color, 4 luminance)
0	1	1 color, 8 luminances (GTIA mode 1)
1	0	9 colors, 9 luminances (GTIA mode 2)
1	1	16 colors, 1 luminance (GTIA mode 3)

7.9) Player/Missile Vertical Delay

VDELAY (Vertical delay for players and missiles) Addr. = 1C

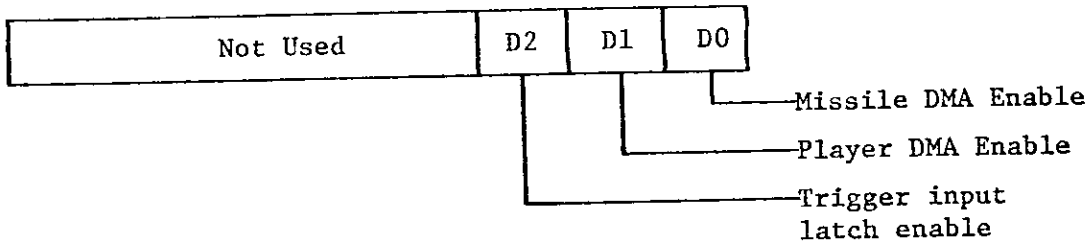
D7	D6	D5	D4	D3	D2	D1	D0
P3	P2	P1	P0	M3	M2	M1	M0

Each player or missile can be delayed by one vertical line. VDELAY is used to give one-line resolution in the vertical positioning of an object when the two-line resolution is enabled. Setting a bit in the VDELAY register to a logical one will move the corresponding object down by one T.V. line.

Note: Vertical delay can only be used when player/missile DMA is enabled. It is also recomended that vertical delay be used only when using 2 line player/missile resolution.

7.10) Graphics Control

GRACTL (Player/missile DMA and trigger latch control) Addr. = 1D



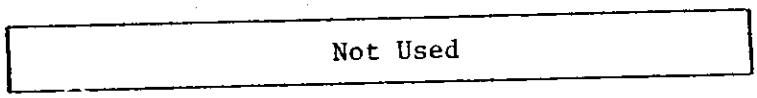
D0=1 Enable missile DMA to missile graphics register
D1=1 Enable player DMA to player graphics registers
D2=1 Enable latches on T3-T0 inputs (latches are cleared and T3-T0 act as normal inputs when this bit is zero).

Player/missile graphics are handled automatically when the DMA control bits of the GRACTL register are enabled. The graphics data is loaded into the graphics registers during the horizontal blank time of every scan line. DMACTL bits D3 and D2 must be set.

The GRACTL register also controls the T3-T0 input latches. If the latch enable bit is set, the trigger input data is latched in the trigger register. The trigger register data is not cleared until GRACTL bit 2 is reset.

7.11) Collision Register Clear

HITCLR (Collision "hit" clear) Addr. = 1E



The collision register bits can be cleared by writing to a single register HITCLR. All collision register bits are cleared when this is done.

8.0) Read-Only Registers

The read-only registers are primarily used to determine object collisions ("hits)". The read-only registers are also used to read the joystick trigger button input data as well as to determine if the system is an NTSC or a PAL/SECAM video standard system.

8.1) Missile to Playfield Collisions

M0PF (Missile 0 to playfield collisions) Addr. = 00
M1PF (Missile 1 to playfield collisions) Addr. = 01
M2PF (Missile 2 to playfield collisions) Addr. = 02
M3PF (Missile 3 to playfield collisions) Addr. = 03

Not Used (zero forced)	D3	D2	D1	D0	
	3	2	1	0	Playfield Type

These registers are used to determine if there has been a collision of one of the four missiles with the different playfields. A collision is detected as a logic one. Writing to the HITCLR register will cause all collision register bits to be reset.

8.2) Player to Playfield Collisions

P0PF (Player 0 to playfield collisions) Addr. = 04
P1PF (Player 1 to playfield collisions) Addr. = 05
P2PF (Player 2 to playfield collisions) Addr. = 06
P3PF (Player 3 to playfield collisions) Addr. = 07

Not Used (zero forced)	D3	D2	D1	D0	
	3	2	1	0	Playfield Type

These registers are used to determine if there has been a collision of one of the four players with the different playfields. A collision is detected as a logic one. Writing to the HITCLR register will cause all collision register bits to be reset.

8.3) Missile to Player Collisions

M0PL (Missile 0 to player collisions) Addr. = 08
M1PL (Missile 1 to player collisions) Addr. = 09
M2PL (Missile 2 to player collisions) Addr. = 0A
M3PL (Missile 3 to player collisions) Addr. = 0B

Not Used (zero forced)	D3	D2	D1	D0
	3	2	1	0 Player Number

These registers are used to determine if there has been a collision of one of the four missiles with the different players. A collision is detected as a logic one. Writing to the HITCLR register will cause all collision register bits to be reset.

8.4) Player to Player Collisions

P0PL (Player 0 to player collisions) Addr. = 0C
P1PL (Player 1 to player collisions) Addr. = 0D
P2P1 (Player 2 to player collisions) Addr. = 0E
P3PL (Player 3 to player collisions) Addr. = 0F

Not Used (zero forced)	D3	D2	D1	D0
	3	2	1	0 Player Number

These registers are used to determine if there has been a collision of one of the four players with any of the other players. A collision is detected as a logic one. Player to same player collisions are always forced to a logic zero. Writing to the HITCLR register will cause all collision register bits to be reset.

8.5) Collisions (Special Conditions)

Altogether there are 60 bits of collision detection provided to detect and store overlap (hits) between players, missiles, and playfield. These collisions can be read by the microprocessor at any time but are generally read during the vertical blank time. There are no bits for missile to missile or playfield to playfield collisions. There are only 12 bits of player to player collision because P0 to P0, etc. will always read as zero. In the high resolution mode (one pixel per ½ color clock), the playfield is represented by playfield 1 luminance and playfield 2 color. In this mode, playfield collision is stored as playfield 2 collision.

8.6) Trigger Input Latches

TRIG0 (Trigger 0 input latch) Addr. = 10
TRIG1 (Trigger 1 input latch) Addr. = 11
TRIG2 (Trigger 2 input latch) Addr. = 12
TRIG3 (Trigger 3 input latch) Addr. = 13

Not Used (zero forced)	D0

0 = Button Pressed
1 = Button Not Pressed

Trigger button data is accessed by the microprocessor by reading TRIG0-TRIG3. If bit 2 of GRACTL is set to a logic one, trigger input data is latched whenever the T3-T0 inputs go to a logic zero. These latches are reset (logic one) when bit 2 of GRACTL is set to a logic zero.

8.7) Television Standards Register

PAL (Television standard identification) Addr. = 14

Not Used (zero forced)	D3	D2	D1	D0	
	1	1	1	1	= NTSC Video Standard
	0	0	0	1	= PAL/SECAM Video Standard

The PAL register is used to determine which version of the GTIA is being used. If bits D3-D0 = HEX F, then the NTSC video standard version of the GTIA is being used. If bits D3-D0 = Hex 1, then the PAL/SECAM video standard version of the GTIA is being used.

8.8) Unused Read Addresses

There are 10 unused read locations of the FGTIA. These addresses are continuous from hex addresses 15 through 1E. Any attempt to read these address locations will return logic zero for data bits D7 through D4 and logic ones for data data bits D3 through D0.

9.0) Read/Write Registers

There is only one read/write register on the FGTIA. This register is used to input and output four bits of parallel data on the S3-S0 I/O lines. Data direction is achieved indirectly by writing to the switch I/O port.

9.1) CONSOL (Switch I/O Port) Read/Write Register

Write location

CONSOL (Write to switch I/O port) Addr. = 1F (write)

Not Used	D3	D2	D1	D0
	S3	S2	S1	S0

0 = Output a logic one and enable input
1 = Output a logic zero and disable input

The switch lines have open-drain output devices which are pulled-up to V_{CC}. In order to use the switch lines as inputs, the output transistor must be turned off by writing a zero to the CONSOL write register.

Read Location

CONSOL (Read switch I/O port) Addr. = 1F (read)

Not Used (zero forced)	D3	D2	D1	D0
	S3	S2	S1	S0

This register reads the condition of the switch input lines (S3-S0). In order to use a switch line as an input, the output bit(s) (CONSOL write) must be zero. Any write bit which is set to a logic one will cause the corresponding read register bit to read as a logic 0 regardless of the input condition.

ABSOLUTE MAXIMUM RATINGS

Voltage at any pin (with respect to V_{SS}).....-0.5V to +9.0V
Operating temperature range.....0°C to +70°C
Storage temperature range.....-40°C to +90°C

D.C. OPERATING CHARACTERISTICS

V_{CC}=5 Volts ±5%, V_{SS} = 0 Volts, T_A = 0 to +70°C

Pin Name	Parameter	Symbol	Min.	Max.	Units	Conditions/Comments
$\phi 2$	Input High Voltage	V_{IH}	2.4	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.4	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	
$\overline{HALT}$	Input High Voltage	V_{IH}	2.0	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.7	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	
$\overline{CS1}$	Input High Voltage	V_{IH}	2.0	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.7	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	
R/$\overline{W}$	Input High Voltage	V_{IH}	2.0	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.7	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	

D.C. OPERATING CHARACTERISTICS (cont'd)

V_{CC}=5 Volts ±5%, V_{SS} = 0 Volts, T_A = 0 to +70°C

Pin Name	Parameter	Symbol	Min.	Max.	Units	Conditions/Comments
D7-D0	Input High Voltage	V_{IH}	2.0	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.7	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V, D_7-D_4 pulldown turned off
	Input Capacitance	C_{IN}		10.0	pF	
D3-D0	Output High Voltage	V_{OH}	2.4		Volts	I_{LOAD}=-0.1mA
	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.6mA
	Load Capacitance	C_{LOAD}		130.0	pF	
D7-D4	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.6mA/ Open Drain Output
	Load Capacitance	C_{LOAD}		130.0	pF	
A4-A0	Input High Voltage	V_{IH}	2.0	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.7	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	
S3-S0	Input High Voltage	V_{IH}	2.0	V_{CC}	Volts	Internal Pull-up
	Input Low Voltage	V_{IL}	V_{SS}	0.7	Volts	
	Pull-Up Current	I_P	-100.0		uA	V_{IN}=+2.4V
	Input Capacitance	C_{IN}		10.0	pF	
	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.6mA/ Open-Drain Output
	Load Capacitance	C_{LOAD}		25.0	pF	

D.C. OPERATING CHARACTERISTICS (Cont'd)

V_{CC}=5 Volts ±5%, V_{SS} = 0 Volts, T_A = 0 to +70°C

Pin Name	Parameter	Symbol	Min.	Max.	Units	Conditions/Comments
C_{RF}	Input High Voltage	V_{IH}	2.4	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.4	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	
$\overline{LOCK}$	Output High Voltage	V_{OH}	2.8		Volts	I_{LOAD}=-0.1mA
	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.6mA
	Load Capacitance	C_{LOAD}		25.0	pF	
C_{VC}	Output High Voltage	V_{OH}	2.4		Volts	
	Output Low Voltage	V_{OL}		0.4	Volts	
	Output Source Current	I_{OH}		-200	uA	V_{OUT}=+1.6V
	Output Sink Current	I_{OL}	200		uA	V_{OUT}=+1.6V
	3-State Leakage Current	I_{TS}	-10	10	uA	V_{OUT}=+1.6V
	Load Capacitance	C_{LOAD}		25.0	pF	
$\overline{DICA}$	Output High Voltage	V_{OH}	2.8		Volts	I_{LOAD}=-0.1mA
	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.6mA
	Load Capacitance	C_{LOAD}		25.0	pF	
T_{IN}	Input High Voltage	V_{IH}	2.0	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.7	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	

D.C. OPERATING CHARACTERISTICS (Cont'd)

V_{CC}=5 Volts ±5%, V_{SS} = 0 Volts, T_A = 0 to +70°C

Pin Name	Parameter	Symbol	Min.	Max.	Units	Conditions/Comments
AN2-AN0	Input High Voltage	V_{IH}	2.0	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.7	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	
C2-C0	Output High Voltage	V_{OH}	2.8		Volts	I_{LOAD}=-0.1mA
	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.0mA
	Load Capacitance	C_{LOAD}		25.0	pF	
L2-L0	Output High Voltage	V_{OH}	2.8		Volts	I_{LOAD}=-0.1mA
	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.0mA
	Load Capacitance	C_{LOAD}		25.0	pF	
$\overline{\text{CSYNC}}$	Output High Voltage	V_{OH}	2.8		Volts	I_{LOAD}=-0.1mA
	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.0mA
	Load Capacitance	C_{LOAD}		25.0	pF	
OSC	Input High Voltage	V_{IH}	2.4	V_{CC}	Volts	
	Input Low Voltage	V_{IL}	V_{SS}	0.4	Volts	
	Leakage Current	I_L		10.0	uA	V_{IN}=+7.0V
	Input Capacitance	C_{IN}		10.0	pF	

D.C. OPERATING CHARACTERISTICS (Cont'd)

V_{CC}=5 Volts ±5%, V_{SS} = 0 Volts, T_A = 0 to +70°C

Pin Name	Parameter	Symbol	Min.	Max.	Units	Conditions/Comments
FØ0	Output High Voltage	V_{OH}	2.8		Volts	I_{LOAD}=-0.1mA
	Output Low Voltage	V_{OL}		0.4	Volts	I_{LOAD}=+1.6mA
	Load Capacitance	C_{LOAD}		25.0	pF	
POWER REQUIREMENTS						
V_{CC}	Supply Voltage	V_{SUP}	4.75	5.25	Volts	
	Supply Current	I_{CC}		175.0	mA	

DYNAMIC OPERATING CHARACTERISTICS

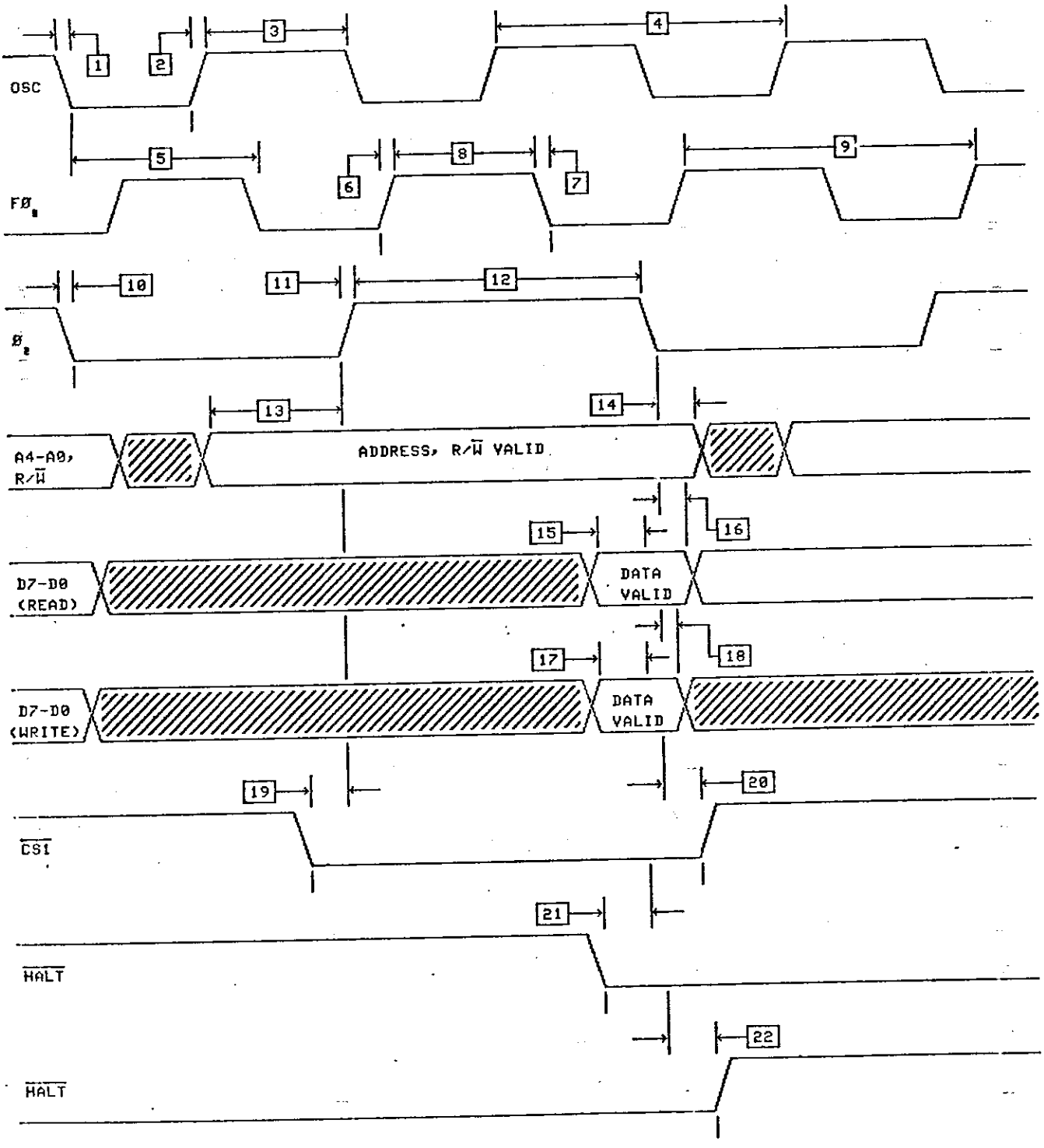
V_{CC} = 5 Volts ± 5%, V_{SS} = 0 Volts, T_A=0 to +70°C

Ref. No.	Parameter	Description	Ref. Pt.	Min.	Typ.	Max.	Units
	F_{OSC}	OSC Clock Input Frequency			3.579		MHz
	$F_{\phi 0}$	Fφ0 Clock Output Frequency			F_{OSC}		
	$F_{\phi 2}$	φ2 Clock Input Frequency			F_{OSC}÷2		
	F_{CRF}	Color PLL Input Frequency				5.5	MHz
	T_{RES}	PLL Freq./Phase Resolution		±20			nS
1	T_{FOSC}	OSC Clock Fall Time				15	nS
2	T_{ROSC}	OSC Clock Rise Time				15	nS
3	T_{OSCHI}	OSC Clock High Time		135		145	nS
4	T_{OSCYC}	OSC Clock Cycle Time			280		nS
5	T_{FPD}	Fφ0 Clock Output Delay	ATE OSC	30		180	nS
6	T_{RCO}	Fφ0 Clock Rise Time				30	nS
7	T_{FFP}	Fφ0 Clock Fall Time				25	nS
8	T_{FPHI}	Fφ0 Clock High Time		105		145	nS
9	T_{FPCYC}	Fφ0 Cycle Time			280		nS
10	T_{FC}	φ2 Clock Fall Time				25	nS
11	T_{RC}	φ2 Clock Rise Time				25	nS
12	T_{CHI}	φ2 Clock High Time		230		260	nS
13	T_{ADS}	Address, R/$\overline{W}$ Setup Time	BLE φ2	130			nS
14	T_{ADH}	Address, R/$\overline{W}$ Hold Time	ATE φ2	30			nS
15	T_{DSR}	Data Setup Time (Read)	BTE φ2			50	nS
16	T_{DHR}	Data Hold Time (Read)	ATE φ2	20			nS
17	T_{DSW}	Data Setup Time (Write)	BTE φ2	50			nS
18	T_{DHW}	Data Hold Time (Write)	ATE φ2	10			nS
19	T_{CSS}	Chip Select Setup Time	BLE φ2	50			nS
20	T_{CSH}	Chip Select Hold Time	ATE φ2	30			nS
21	T_{HS}	$\overline{HALT}$ Setup Time	BTE φ2	50			nS
22	T_{HH}	$\overline{HALT}$ Hold Time	ATE φ2	50			nS

DYNAMIC OPERATING CHARACTERISTICS (cont'd)

V_{CC} = 5 Volts ± 5%, V_{SS} = 0 Volts, T_A = 0 to +70°C

Ref. No.	Parameter	Description	Ref. Pt.	Min.	Typ.	Max.	Units
23	T_{ANS}	AN2-AN0 Setup Time	BLE OSC	50			nS
24	T_{ANH}	AN2-AN0 Hold Time	ALE OSC	130			nS
25	T_{SSI}	S3-S0 Input Setup Time	BLE ϕ2	100			nS
26	T_{SHI}	S3-S0 Input Hold Time	ATE ϕ2	100			nS
27	T_{SSO}	S3-S0 Output Delay	ATE ϕ2			800	nS
28	T_{OCD}	OSC to C2-C0 Delay	ATE OSC	60		270	nS
29	T_{LD}	L2-L0 Output Delay	ATE OSC	360		590	nS
30	T_{OLD1}	OSC to L2-L0 Delay (full cycle resolution)	ATE OSC	80		310	nS
31	T_{OLD2}	OSC to L2-L0 Delay (½ cycle resolution)	ATE OSC	95		315	nS
32	T_{OLD3}	OSC to L2-L0 Delay (½ cycle resolution)	ALE OSC	95		315	nS
33	T_{SNCD}	$\overline{\text{CSYNC}}$ Output Delay	ATE OSC			650	nS
34	T_{OSNCD2}	OSC to $\overline{\text{CSYNC}}$ Output Delay	ATE OSC			85	nS
35	T_{LKHL}	$\overline{\text{LOCK}}$ High to Low Transition	ATE OSC	75		315	nS
36	T_{LKLH}	$\overline{\text{LOCK}}$ Low to High Transition	ALE OSC	80		355	nS
37	T_{DAHL}	$\overline{\text{DICA}}$ High to Low Transition	ALE OSC	75		325	nS
38	T_{DALH}	$\overline{\text{DICA}}$ Low to High Transition	ALE OSC	80		355	nS
39	T_{TS}	T_{IN} Setup Time	BTE Fϕ0	50			nS
40	T_{TH}	T_{IN} Hold Time	ALE Fϕ0	0			nS



ATARI Semiconductor Group	COMPANY CONFIDENTIAL	DEVICE NUMBER C020120	DEVICE NAME FGTIA
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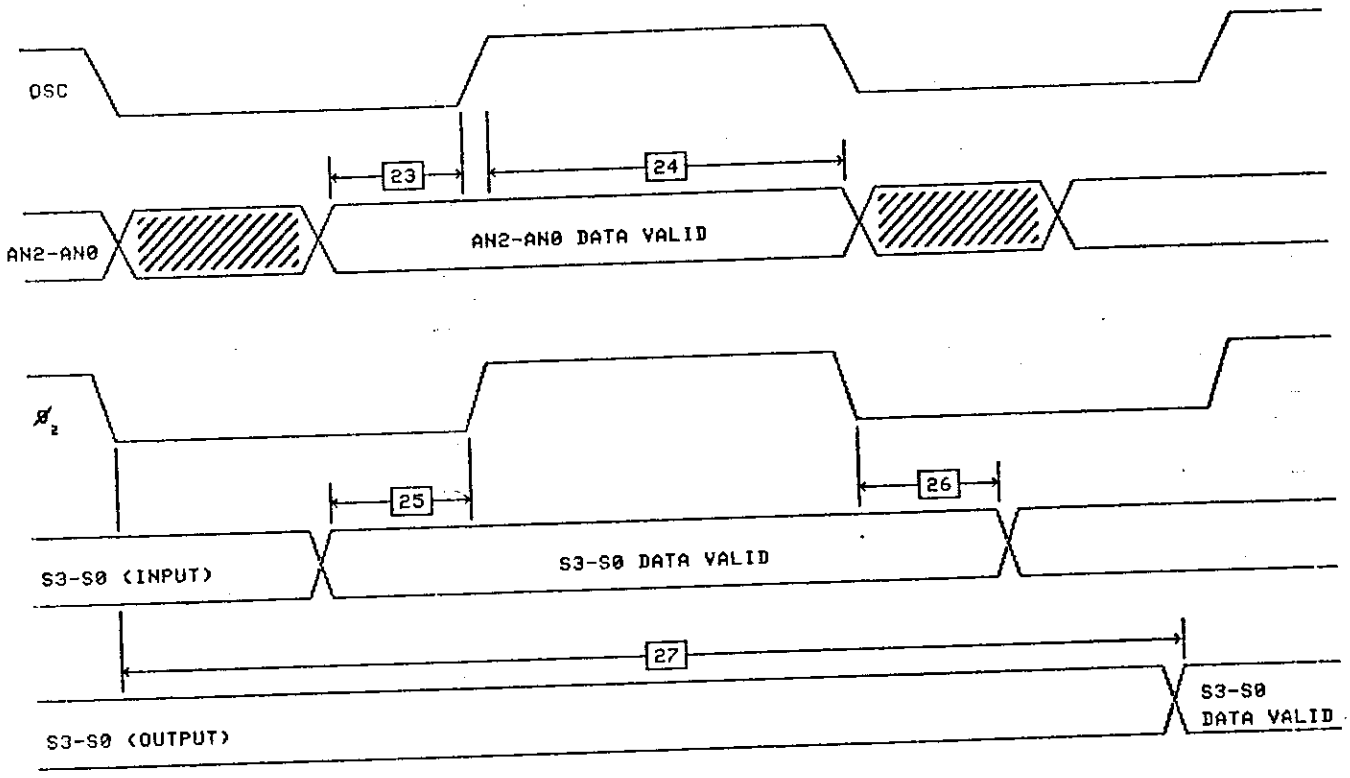
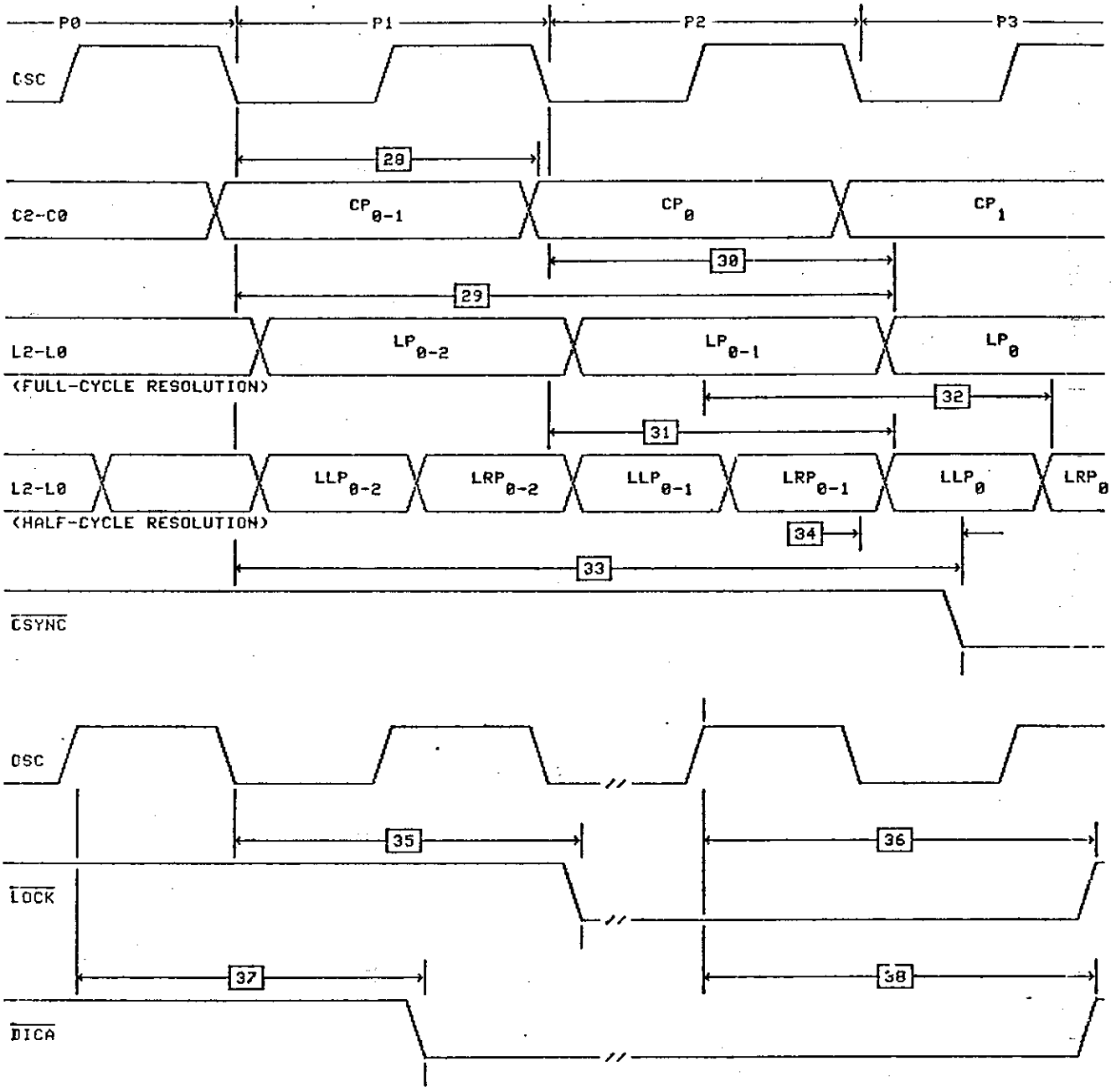
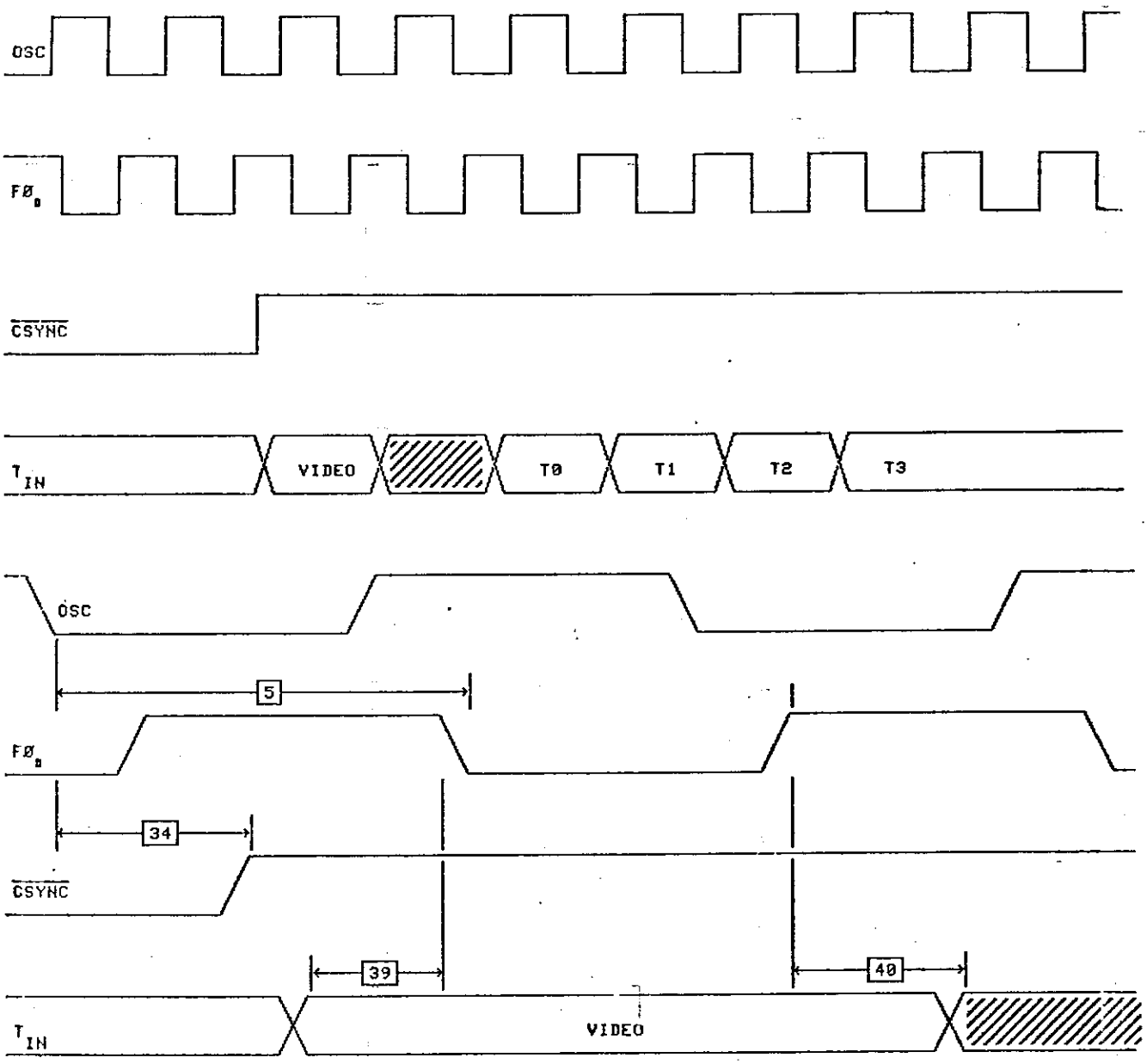

OSC
23
24
AN2-AN0
AN2-AN0 DATA VALID
ϕ_2
25
26
S3-S0 (INPUT)
S3-S0 DATA VALID
27
S3-S0
DATA VALID
S3-S0 (OUTPUT)



NOTES: Pn IS DEFINED AS SOME ARBITRARY PIXEL TIME.
CPn IS DEFINED AS THE COLOR INFORMATION FOR Pn.
LPn IS DEFINED AS THE LUMINANCE INFORMATION FOR Pn (FULL-CYCLE RESOLUTION).
LLPn IS DEFINED AS THE LEFT PIXEL LUMINANCE INFORMATION FOR Pn (HALF-CYCLE RESOLUTION).
LRPn IS DEFINED AS THE RIGHT PIXEL LUMINANCE INFORMATION FOR Pn (HALF-CYCLE RESOLUTION).



DATA IS SHIFTED INTO THE TIN INPUT AFTER A LOW TO HIGH TRANSITION ON THE $\overline{\text{CSYNC}}$ OUTPUT, REGARDLESS OF THE VIDEO MODULATION MODE (POSITIVE OR NEGATIVE VIDEO).

FGTIA Address Table

Address	WRITE		READ	
	Name	Description	Name	Description
00	HPOSP0	Horz. Posit. Player 0	M0PF	Read Missile to Playfield Collisions
01	HPOSP1	Horz. Posit. Player 1	M1PF	
02	HPOSP2	Horz. Posit. Player 2	M2PF	
03	HPOSP3	Horz. Posit. Player 3	M3PF	
04	HPOSM0	Horz. Posit. Missile 0	P0PF	Read Player to Playfield Collisions
05	HPOSM1	Horz. Posit. Missile 1	P1PF	
06	HPOSM2	Horz. Posit. Missile 2	P2PF	
07	HPOSM3	Horz. Posit. Missile 3	P3PF	
08	SIZEP0	Size Player 0	M0PL	Read Missile to Player Collisions
09	SIZEP1	Size Player 1	M1PL	
0A	SIZEP2	Size Player 2	M2PL	
0B	SIZEP3	Size Player 3	M3PL	
0C	SIZEM	Size All Missiles	P0PL	Read Player to Player Collisions
0D	GRAFP0	Graphics Player 0	P1PL	
0E	GRAFP1	Graphics Player 1	P2PL	
0F	GRAFP2	Graphics Player 2	P3PL	
10	GRAFP3	Graphics Player 3	TRIG0	Read Joystick Trigger Buttons
11	GRAFM	Graphics All Missiles	TRIG1	
12	COLPM0	Color-lum of Player-Missile 0	TRIG2	
13	COLPM1	Color-lum of Player-Missile 1	TRIG3	
14	COLPM2	Color-lum of Player-Missile 2	PAL	Read PAL/NTSC Bits
15	COLPM3	Color-lum of Player-Missile 3		
16	COLPF0	Color-lum of Playfield 0		
17	COLPF1	Color-lum of Playfield 1		
18	COLPF2	Color-lum of Playfield 2		
19	COLPF3	Color-lum of Playfield 3		
1A	COLBK	Color-lum of Background		
1B	PRIOR	Priority Select		
1C	VDELAY	Vertical Delay		
1D	GRACTL	Graphic Control		
1E	HITCLR	Collision Clear		
1F	CONSOL	Write to Switch I/O Port	CONSOL	Read from Switch I/O Port