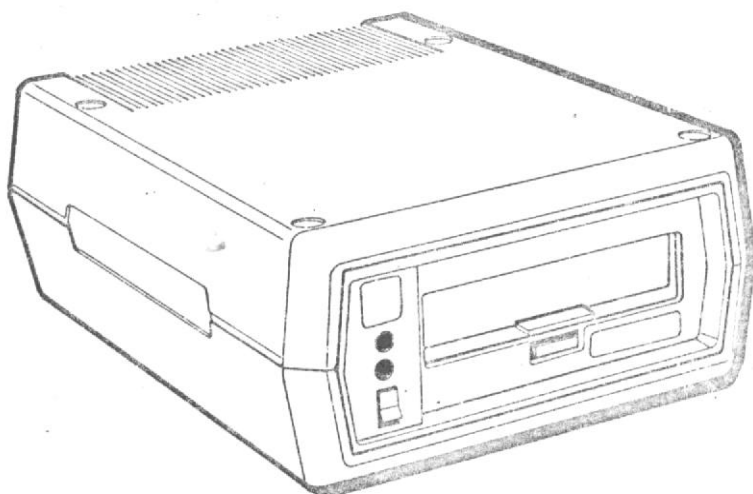


ATARI 810 DISK DRIVE



FIELD SERVICE MANUAL

JULY 1980
FS015854
REV. 1

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SPECIFICATIONS

TECHNICAL SPECIFICATIONS

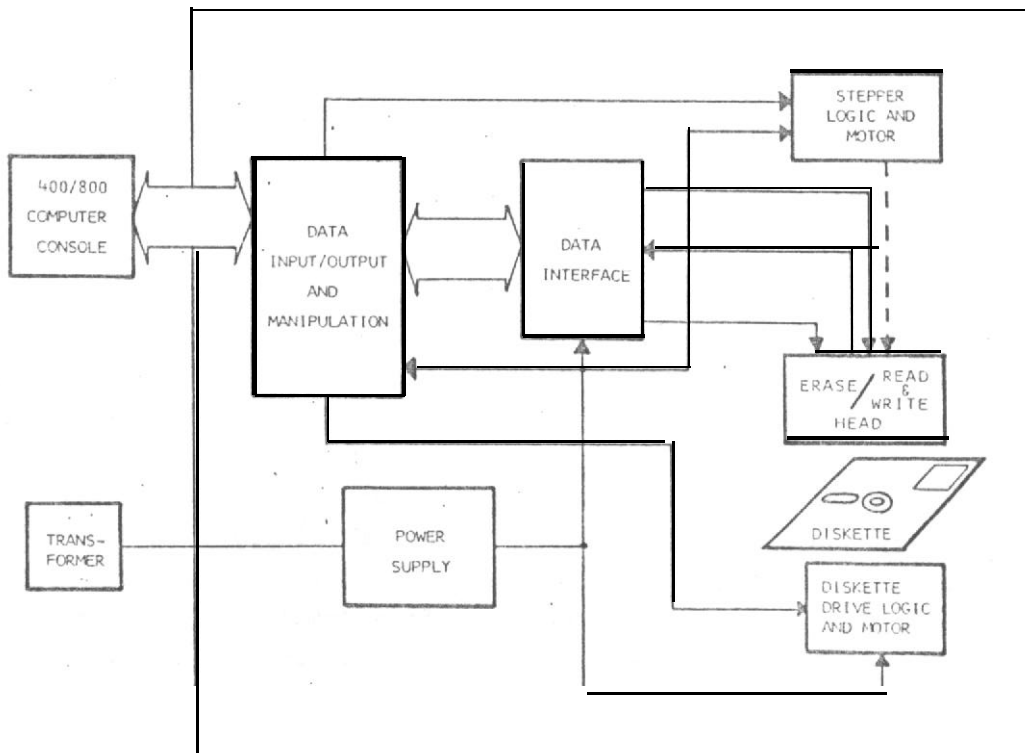
1. Uses ANSI standard 5¼ inch diskettes in a soft sector format.
2. 40 tracks at 48 TPI track density.
3. Single density (FM), single sided recording.
4. Over 90K bytes storage per diskette.
5. 709 sectors of 128 bytes each.
6. Minimum data access time: 236 milliseconds.
7. Average data transfer rate: 6000 bits per second.
8. Automatic stand-by capability (built in microprocessor).
3. Up to four Drives can be daisy chained to a single 400/800 Computer Console (w/minimum 16K RAM) via select switches at the rear of the Drive.
10. Drives directly interface with the ATARI 400/800 Computer Console (16K RAM) or indirectly through the ATARI 850 Interface Module or 820 Printer.-

THEORY OF OPERATION

THEORY OF OPERATION

The ATARI 400/800 Computer Console with 16K of RAM installed connects directly to the 810 Floppy Disk Drive. The Drive may also be daisy chained through the 820 Printer or the 850 Interface Module. up to four Disk Drives can be connected to a single Console.

Refer to the Disk Drive Operators Manual for installation and operating instructions.

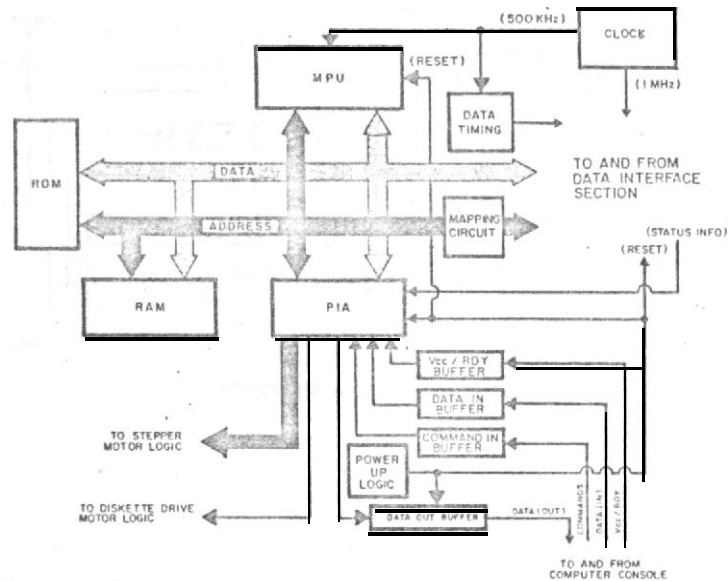


ATARI 810 FLOPPY
DISK DRIVE

The ATARI 810 Floppy Disk Drive consists of the following major sections:

- * Data Input/Output and Manipulation
- * Data Interface
- * Read/Write and Erase Heads
- * Stepper Motor and Logic
- * Diskette Drive Motor and Logic
- Power Supply

DATA INPUT/OUTPUT AND MANIPULATION SECTION

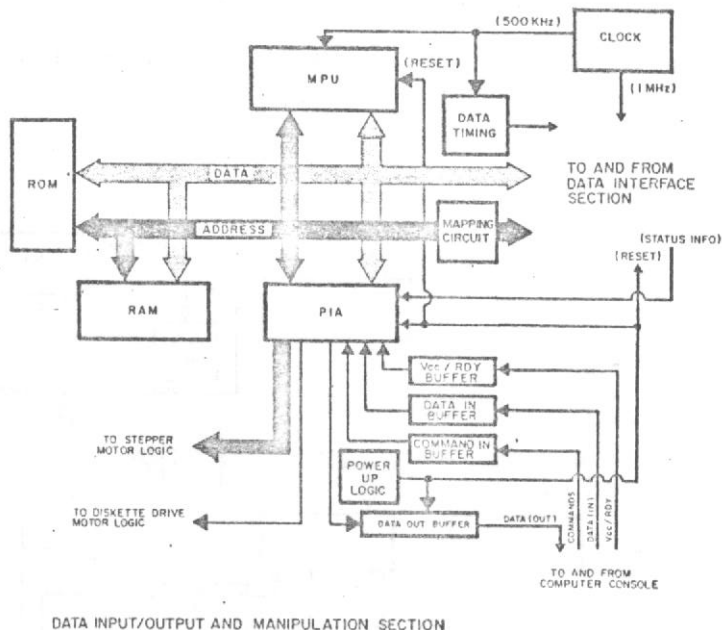


DATA INPUT/OUTPUT AND MANIPULATION SECTION

Data, control commands and a VCC/RDY signal from the Computer Console enter the Disk Drive through either of the two serial I/O connector jacks at the rear of the Drive chassis.

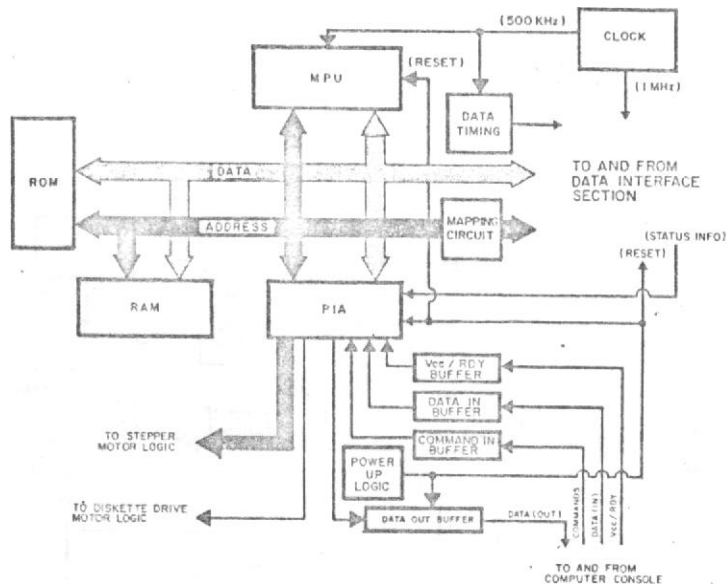
Each of the three main signal input lines are buffered for static protection and to reduce power consumption on the 800 I/O lines.

Data is sent by the Console in serial format, with checksums accompanying the data for validity verification.



The Drive's PIA is primarily a buffering and signal formatting device, with no decision making or computational capability. It is responsible for the following:

- * Applying the Console's serial outputs to the Data and Address Busses when requested by the Drive's Microprocessor Unit (MPU).
- * Assisting in the control of the Read/Write and Erase Head position by buffering commands sent to the Stepper Motor Logic.
- * Assisting in control of the Diskette Drive Motor Logic.
- * Providing 128 bytes of RAM for temporary storage of status information and data sent by the Data Interface Section for application to the HP".

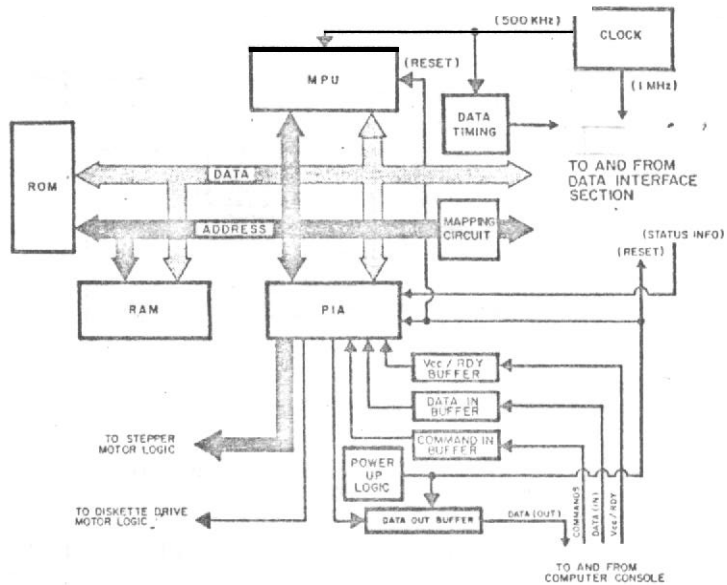


The MPU provides the primary decision making and computational capabilities for the Disk Drive. The Drive's MPU is responsible for the following:

- * Controlling data transfers, through its control over the Common Data and Address Busses.
- * Interpreting and controlling the accomplishment of Console commands (temporarily stored in RAM) and Disk Drive operating instructions (permanently stored in ROM).
- * Controlling the Stepper, Disk Drive and Motor Logics, which are buffered by the PIA.

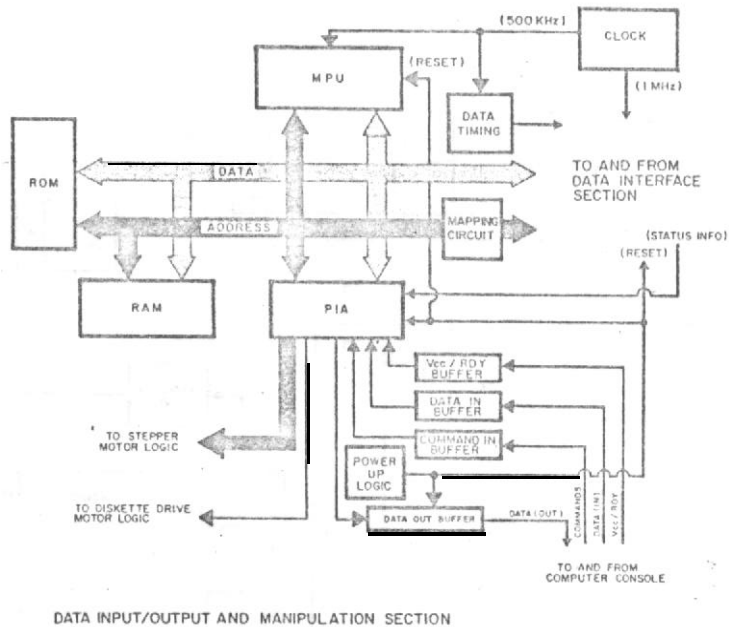
The Drive's ROM contains specific operating instructions used by the CPU to accomplish a variety of functions. These functions include telling the Disk controller (1771-01) what task to perform.

The Drive's RAM is used by the CPU for temporary storage of both data and system information.



DATA INPUT/OUTPUT AND MANIPULATION SECTION

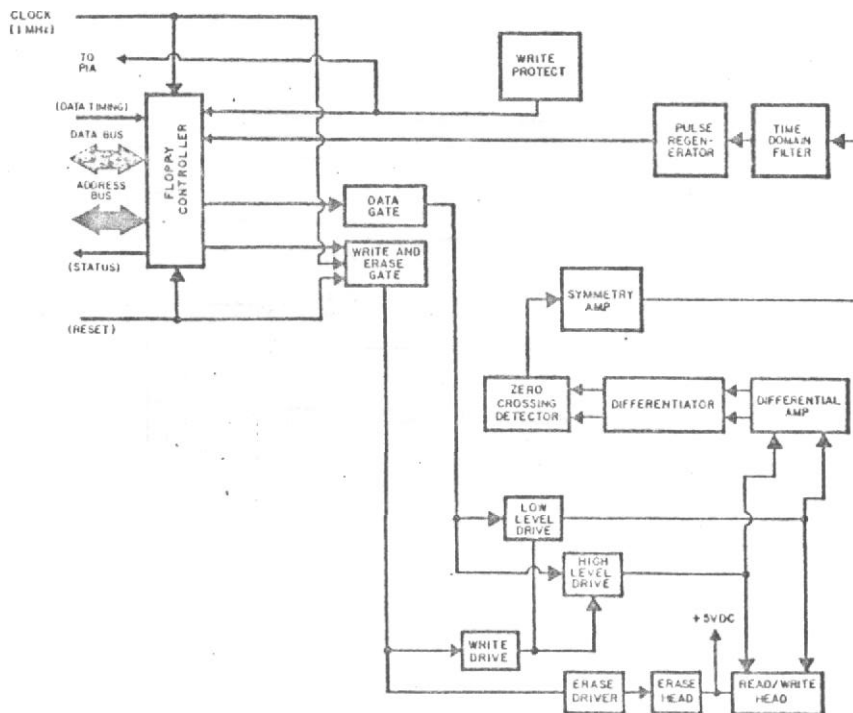
The Drive's Data Output Buffer transfers the formatted data through the PIA to the Data (out) line going to the Computer Console.



The Drive's Power Up Logic circuit resets the MPU, PIA and Data Interface Section whenever the Disk Drive is turned on. The RESET references the electrical circuits to their starting conditions. Additionally, the Power Up Logic circuit locks the Data Output Buffer off during a short period when the Drive is turned on. This prevents random pulses generated by the Drive's circuitry (during the initializing period) from being sent to the Console.

The Drive's Clock circuitry generates both a crystal controlled 1 MHz. and a 500 KHz. clock signal. The 1 MHz. signal is used by the Data Interface Section. The 500 KHz. signal is used both as a clock signal to the MPU, and to time data exiting from the Data Input/Output and Manipulation Section into the Data Interface Section.

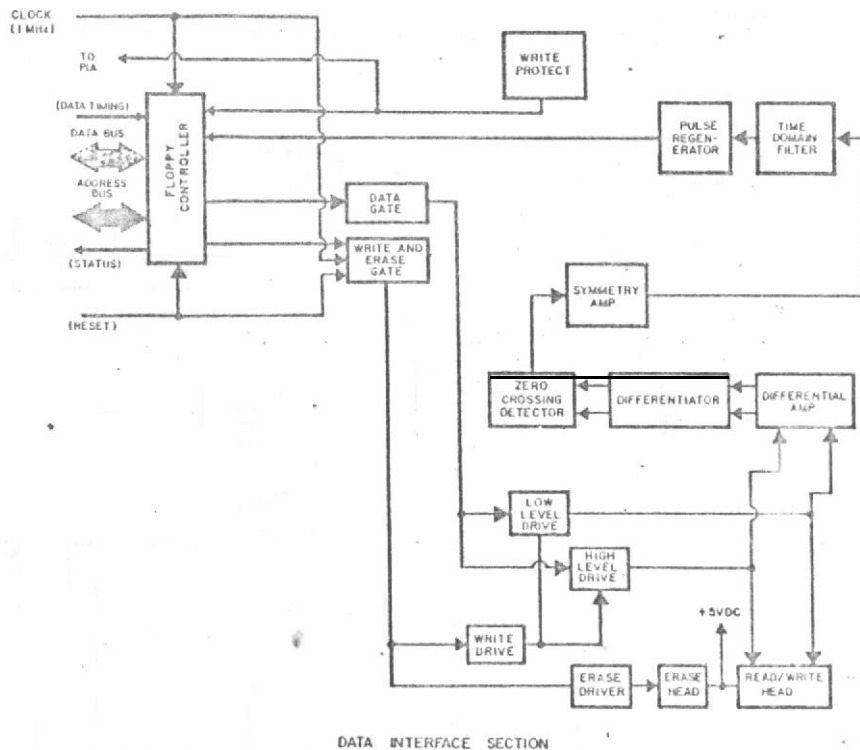
DATA INTERFACE SECTION



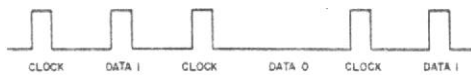
The major element of the Data Interface Section is a Floppy Disk Controller (FDC). The FDC is a highly specialized microprocessor. It is responsible for the following activities:

- * Combining data, timing and data validity pulses into the serial format to be recorded.
- * Separating the above and providing the output data in parallel during a read operation.
- * Controlling the Write and Erase Logic circuitry during a write operation.

- * Generating the data validity codes (called Cyclic Redundancy Checks - or CRC's) during a write operation, and checking them during a read operation.



The Drive's Write and Erase Logic circuitry is controlled by, and receives its data from the FDC. Initially, the Data Gate converts the leading edge of each pulse (data, clock, etc.) into a single corresponding change of signed level. These levels then determine the polarity of the Drive's currents applied to the Read/Write Head through the High and Low level Drives, The Write Driver limits the write currents.

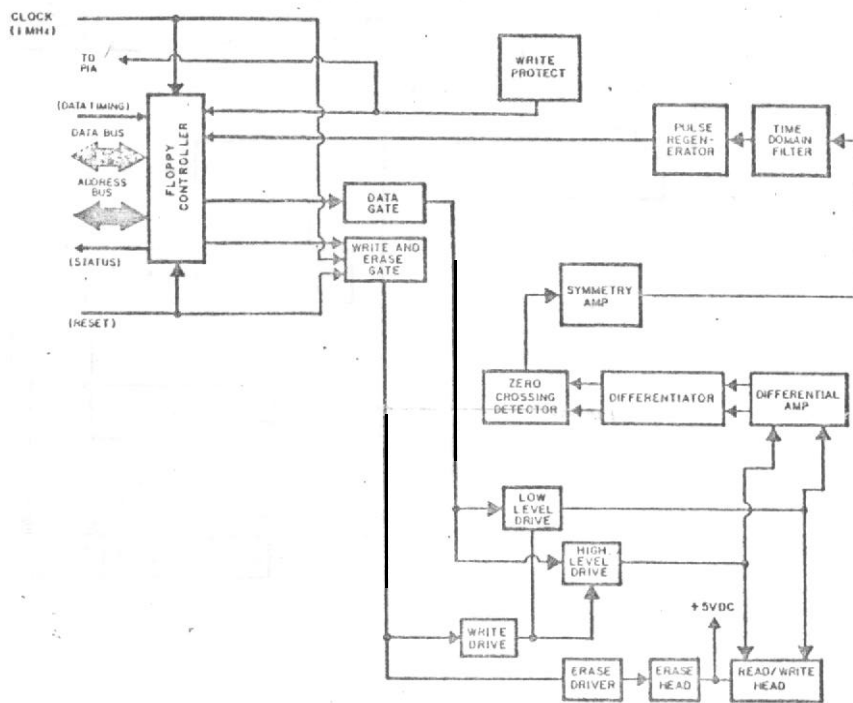


The FDC combines clock pulses with data to form a serial signal.



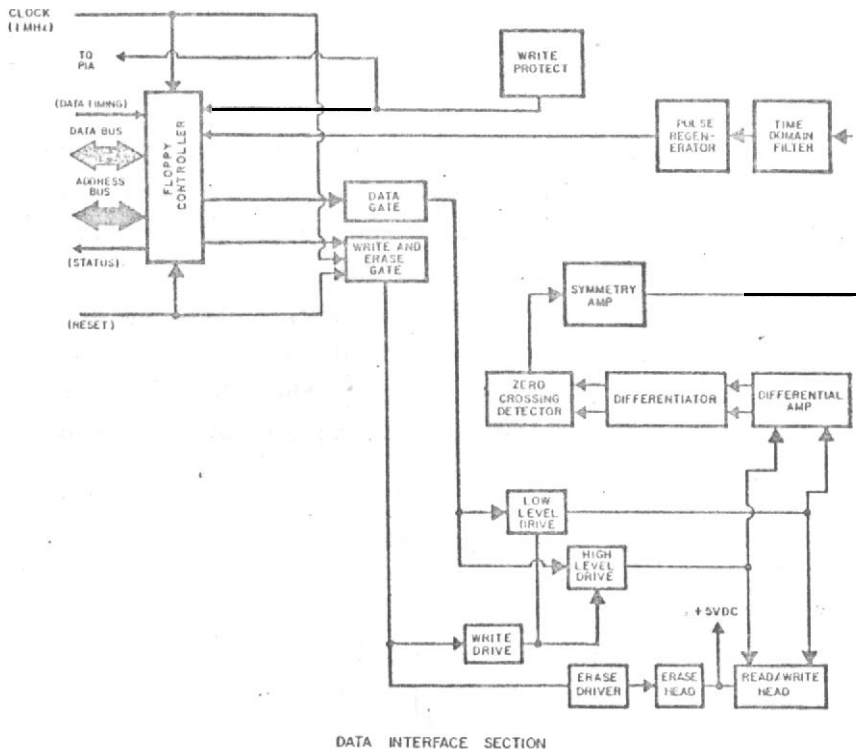
The Data Gate converts each pulse's leading edge into a logic level change, as shown.

Basically, this is the signal applied to the head during a write operation. The high levels out of the Data Gate turn on the High level Driver, and the low levels turn on the Low level Driver.



DATA INTERFACE SECTION

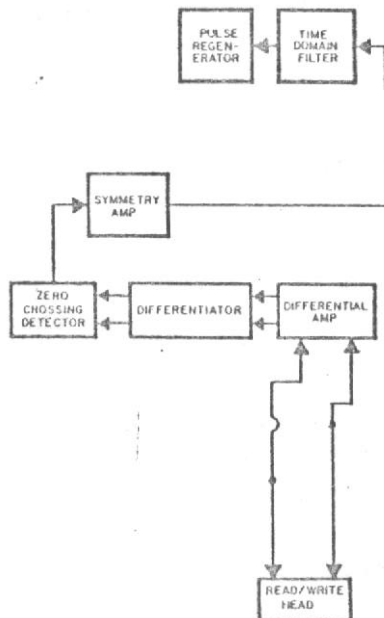
The Write and Erase Gate turns on both the Write and Erase Drivers during a write operation, and turns them off during a read operation. The Erase Driver drives the Erase Head during a write operation. See the Read/Write and Erase Head discussion for further information.

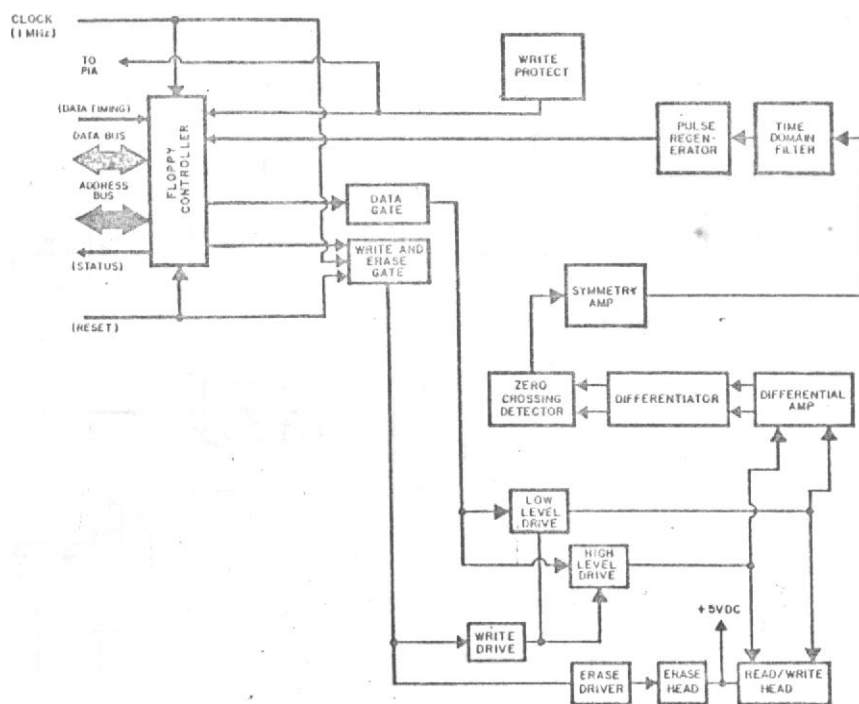


Major elements of the Drive's Read Data Conditioning circuitry are:

- * **Differential Amp** - Initial amplification of Read/Write Head signals.
- * **Differentiator** - Squaring up the two differential amp outputs.
- * **Zero Crossing Detector** - The single output changes level whenever the two 180° out-of-phase input signals cross their zero axis coincidentally (eliminates false pulses caused by Read/Write Head signal decay, rather than intentional signal level changes).
- * **Symmetry Amp** - Ensures exact zero referencing of the signal.
- * **Time Domain Filter** - Trims and further shapes the signal.
- * **Signal Gate** - Produces a single pulse out for each logic level transition at its input. This results in the reproduction of the original FDC signal.

During a read operation the Read/Write Head produces two 180° out-of-phase signals. These are very weak, highly distorted versions of the original signals produced by the Write Logic Data Gate. The Read Data Conditioning circuitry must amplify, square up and filter the read signals to reproduce the original serial string of bits produced by the FDC. This reproduced signal is returned to the FDC by the Read Data Conditioning circuitry.





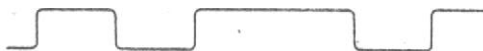
Signal Decay



Two 180° out-of-phase signals are generated by the head during a read operation and amplified by the Differential Amplifier.



The Differentiator squares the two out-of-phase signals.



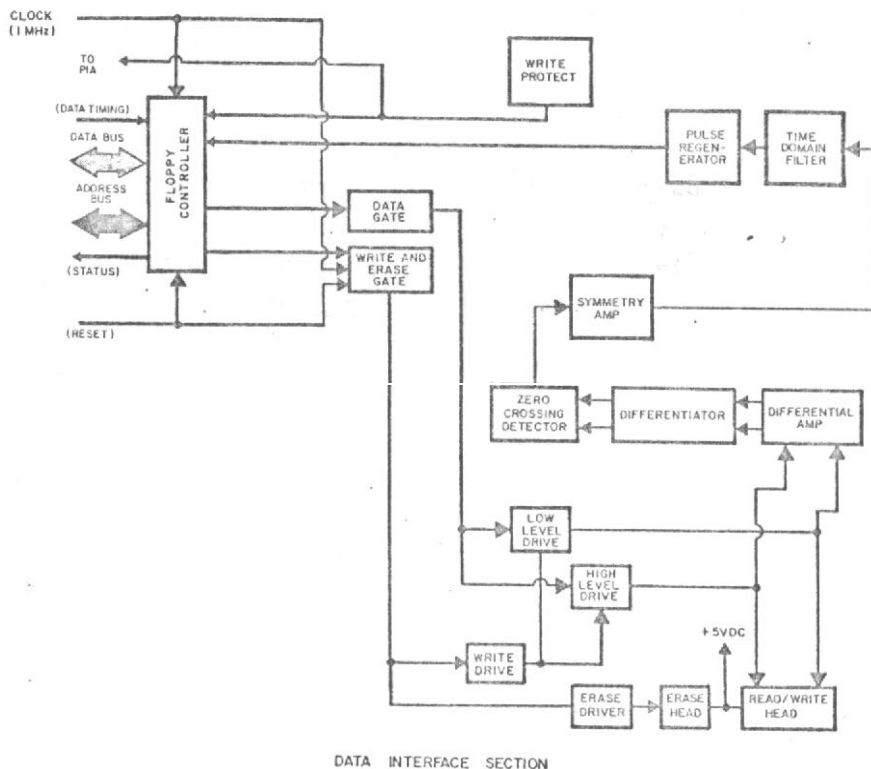
The Zero Axis Crossing Detector provides a single output, further squared and now without any signal decay effects.



The Time Domain Filter provides a signal with very sharp leading and trailing edges.

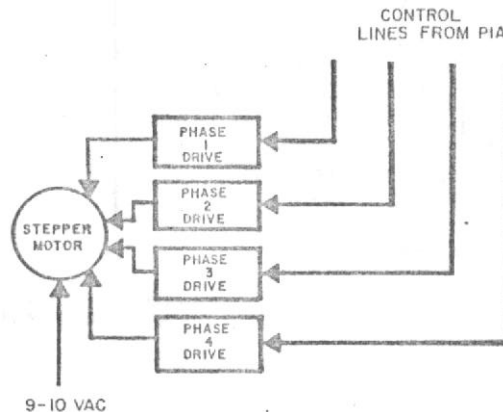


The Pulse Regenerator converts each logic level change into a single pulse, recreating the original signal produced by the FDC during the write operation.



The Drive's Write Protect circuit senses the presence or absence of a special notch in one side of the diskette casing. A write protected diskette's notch will be covered with an opaque tape. The circuit is basically an LED/photo transistor sensor, whose output is buffered before being applied to the FDC.

With an unprotected diskette, the sensor signal allows the FDC to write data onto the diskette.

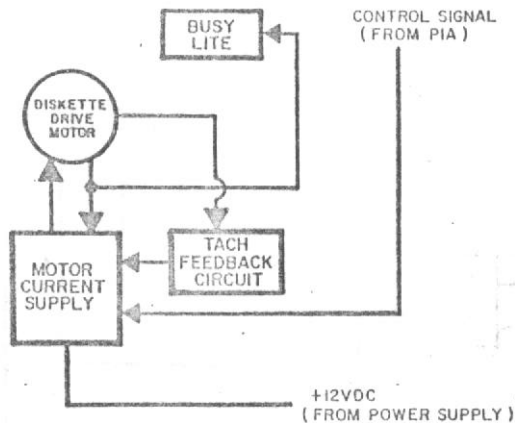


STEPPER MOTOR AND LOGIC

The Stepper Motor is a four phase motor with a 3.6° rotor rotation per step. The motor has a total of 100 poles, providing 100 rotor steps for the motor's full 360° rotation. Each step change in the motor is translated, through a steel band connection, to a single track change for the Read/Write and Record Bead assembly. The diskette is divided into 40 tracks, so-the full range of the Stepper Motor is not used.

The Stepper Logic is controlled from the PIA. The four PIA signals are logic levels acting as the Stepper Motor's four phase inputs. These levels, in their various possible combinations, drive the Stepper Motor to reposition the head assembly from track to track.

The Stepper Motor is supplied with a nominal 3 to 10 VAC from the Power Supply.



DISKETTE DRIVE MOTOR AND LOGIC

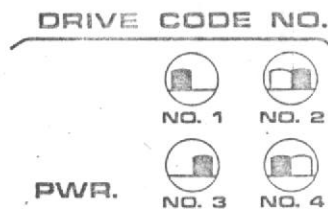
The Diskette Drive Motor is a DC motor that indirectly drives the diskette. The motor includes an internal tachometer, whose output is monitored in the Tach Feedback circuit. Variations in motor speed, as sensed by the Tach Feedback circuit, vary the current supplied to the motor. Diskette speed is set to 290 RPM $\pm 1\%$.

Motor rotation is translated into diskette rotation via a pulley (attached to the motor shaft), a drive belt and a flywheel attached to a diskette drive spindle.

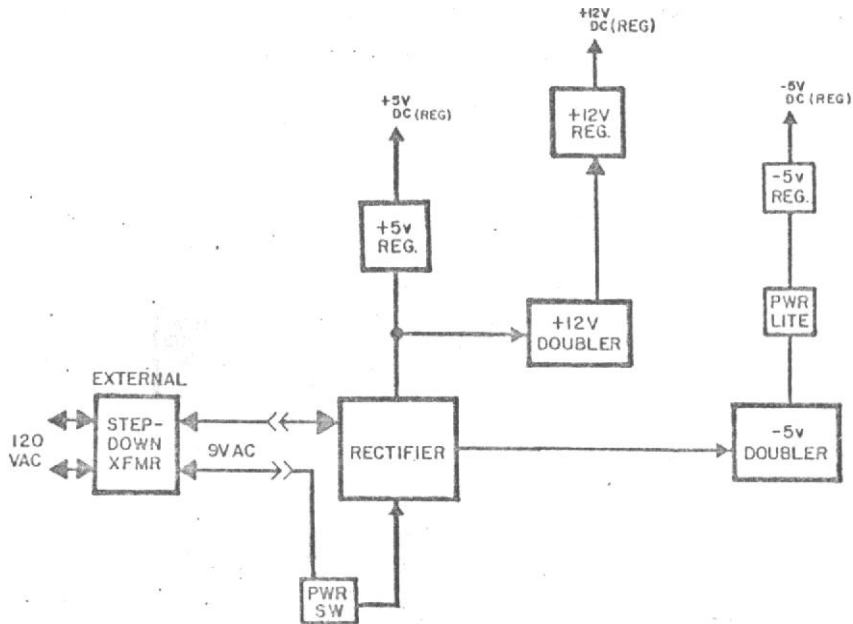
When a diskette has been inserted into the Disk Drive, and the front door has been latched closed, the diskette is centered and clamped to the spindle by a clutching cone assembly.

Whenever the Diskette Drive Motor is supplied with power, the Drive's BUSY lite (LED) is turned on.

DISK DRIVE SELECT



A double "Single pole - Double throw" switch gives the Disk Drive operator the ability to assign a number to, and therefore a code for addressing, each of up to four Drives that could be daisy chained together. The switch is accessible at the rear of the Drive chassis. The switch settings are read by the Drive's MPU through the PIA.



POWER SUPPLY

An external step-down transformer is supplied with each Drive. The 120 VAC line Power is dropped to 9 VAC by the transformer. This 9 VAC enters the Drive through the "PWR" jack at the back of the chassis.

Turning the Drive's front panel "PWR" switch ON applies the 9 VAC to a full wave bridge rectifier. The Power Supply provides the following:

- * The unregulated 9-10 VDC Diskette Drive Motor supply.
- * A regulated +5 VDC.
- * A regulated +12 VDC (initially produced by a voltage doubler circuit).
- * A zener regulated -5 VDC (also produced by a voltage doubler circuit).

A "PWR ON" lite (LED) is turned on through the -5 VDC section of the supply.

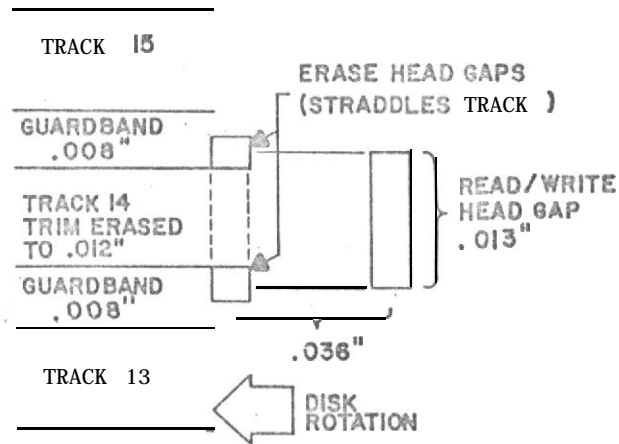
READ/WRITE AND ERASE HEADS

A magnetic head converts electrical currents into magnetic fields, and vice-versa. The Read/Write Head consists primarily of two ferrite core halves, wound with a centertapped coil. The centertap is connected to the regulated +5 VDC from the Power Supply. One end of the coil is connected to the High level Driver, and the other end to the Low level Driver.

WRITE OPERATION

Each logic level causes current to flow in one half of the coil, with a high in one direction and a low in the other. These currents 'set up corresponding magnetic fields in the core halves, with a high represented by a field in one direction, and a low by a field in the opposite direction.

When the ferric oxide coating on the diskette is in contact with the head, it completes the magnetic path between the core halves. In response to the change in direction of the magnetic field (logic level change) passing through the diskette's coating, the oxide particles realign themselves. Particle alignment in one direction represents a high level, and alignment in the other direction a low level. "



During a write operation, the magnetic fields coupling through the diskette print a relatively wide (.013") path of aligned particles. In order to prevent one recorded track from interfering with either the next inner or next outer track, a blank space, called a guardband, is created between tracks. The Erase Head creates these guardbands. It straddles the Read/Write Head in such a way that just after (.036") the data is written onto the diskette, the Erase Head "tunnel" erases the track width down to .012", leaving .008" guardbands between tracks.

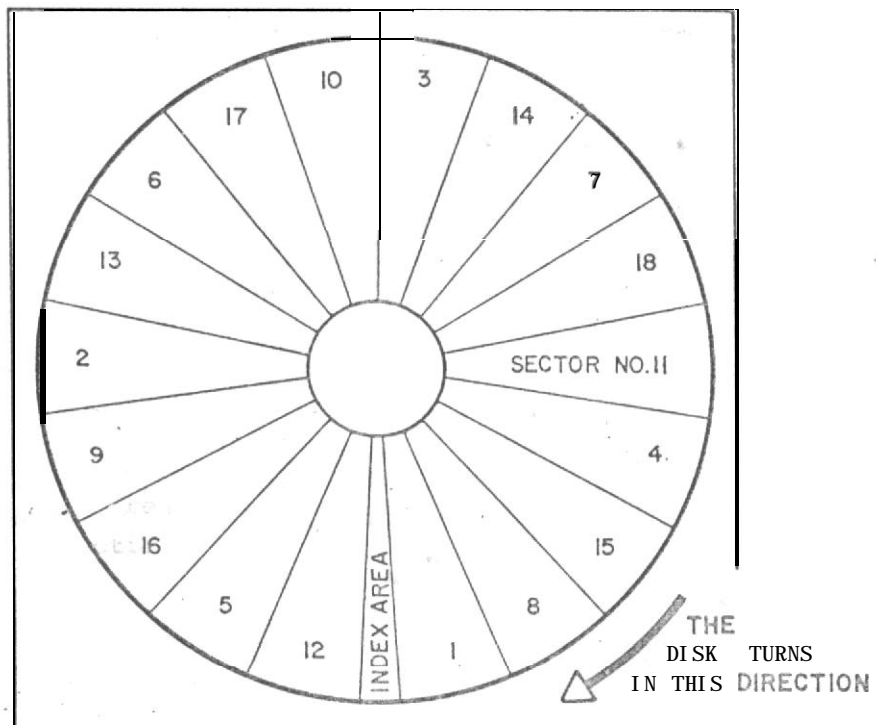
READ OPERATION

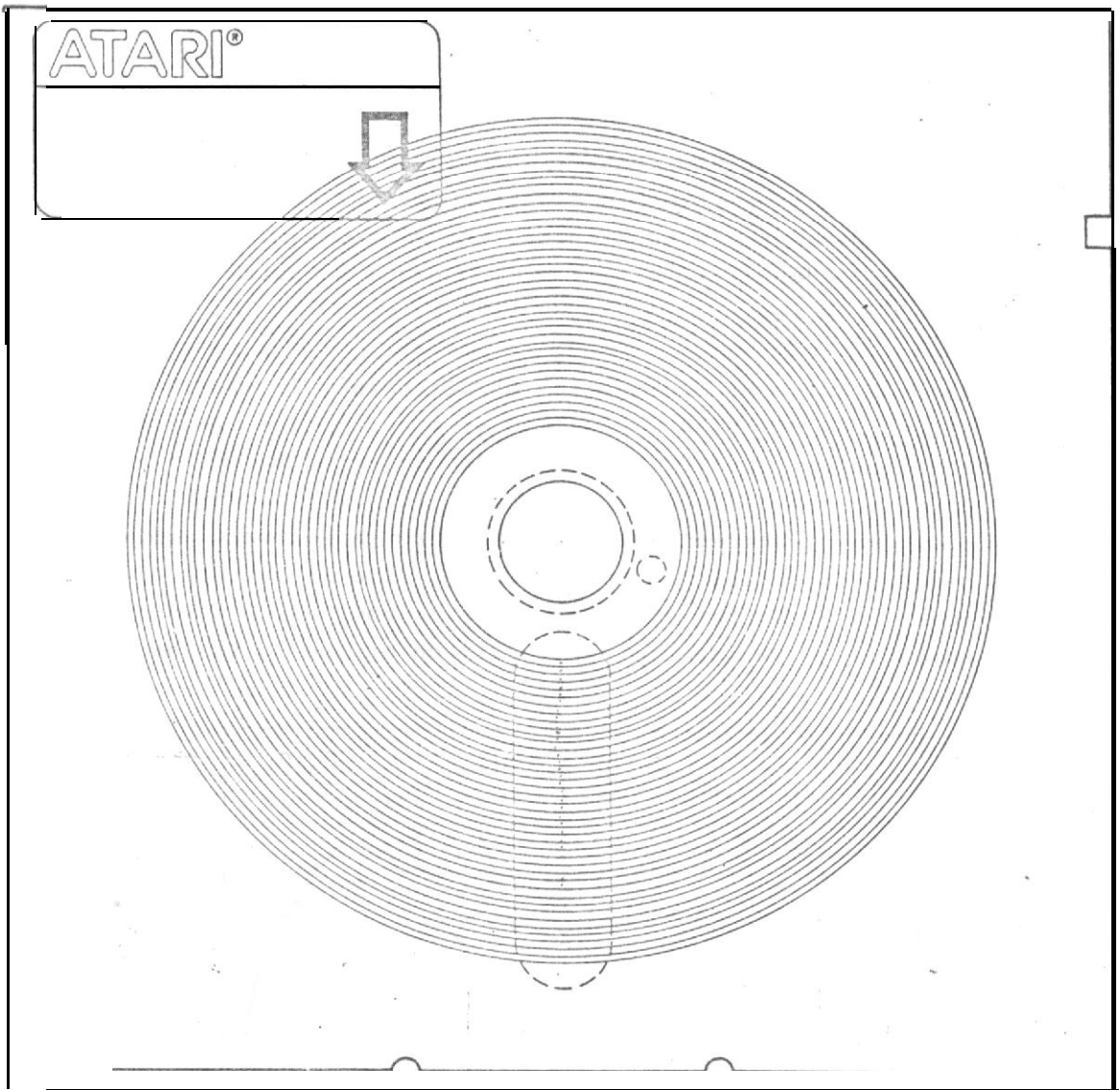
During a read operation, the very small fields existing due to particle alignment on the diskette couple through the head core halves. The diskette is rotating, causing the specific field being felt in the core halves to change for each change in particle alignment (ie. change of recorded logic level). The changing fields in the core halves generate corresponding currents in the head coil windings. It is these very small signals that are applied to the differential amplifier.

DISKETTE FORMATTING

The specific arrangement of information recorded onto a diskette is called the diskette format. Unless a Master Diskette is to be used, the diskette must be initially formatted with a Disk Operating System (DOS) software program.

The DOS software divides the diskette into 19 pie-shaped slices, 18 of which are called sectors. These are not the same as the "709 FREE SECTORS" referred to when you list the directory of a disk. Because the diskette division is accomplished totally through software, this process is called "soft sectoring". The 18 sectors are equal in size, but the 19th (very narrow) slice acts as an index to define the start of each of the 40 tracks.





All 40 tracks receive the same formatting as follows:

*	256	bytes	00
	1	byte	FC (index mark)
	11	bytes	00 or FF
**	6	bytes	00
	1	byte	FE
	1	byte	Track Number (00 thru 27) (HEX)
	1	byte	00
	1	byte	Sector Number (01 thru 12) (HEX)
	1	byte	00
	1	byte	CRC byte 2
	1	byte	CRC byte 1
	17	bytes	00
		or	
	11	bytes	FF
	6	bytes	00
	1	byte	FB (data address mark)
	128	bytes	Data (FF for blank fill)
	1	byte	CRC byte 2
	1	byte	CRC byte 1
	11	bytes	00 or FF

Cyclic Redundancy Checks (CRCs) are generated in the Drive's Floppy Disk Controller (FDC) during a write operation. The FDC uses the recorded CRCs during a read operation to verify the data. CRCs are similar in function to the checksums used between the Computer Console and the Disk Drive's MPU.

* Appear only once per track for indexing.

** Repeated 18 times per track, producing the full 18 sectors.

