# Atari VME Expansion For
## TT030 and Mega STE Products

Abstract:

The TT030 and Mega STE each support one single height (3U) VME slot.

This slot complies with the VITA C.1 specification, with minor differences in electrical drive and termination. The following information is intended for VME card designers, and does not represent variances from the VITA specification (other than mentioned above).

Specification:

VITA C.1
ANSI/IEEE STD 1040 (1987)
IEC 821 and 297

Mechanical:

Single height Eurocard (3U)

Data Transfer Bus: A24/D16 or A16/D16

Arbitration:

Slave only. Alternate bus masters are not supported.

BR0*, BR1*, BR2*, and BR4* are connected together and pulled up by a 1K resistor to VCC.

BG0IN*, BGG1IN*, BG2IN*, and BG3IN* are connected together and pulled up by a 1K resistor to VCC.

BBSY* and BCLR* are each pulled up by a 1K resistor to VCC but are not otherwise driven.

BG0OUT, BG1OUT, BG2OUT, and BG3OUT are not connected.

Interrupts:

IRQ1* thru IRQ7* can each be used and are pulled up by a 1K resistor to VCC. IRQ3*, IRQ5*, and IRQ6* can also be driven low by the system.

The SYSFAIL* signal is also pulled up by a 1K resistor and can generate a level 7 system interrupt when asserted by a card.

IACK* and IACKIN* are driven by the system. A card should not drive these signals.

IACKOUT* is not connected.

The status word supplied by the card during the interrupt acknowledge cycle is used as the 68030 interrupt vector. For compatibility with Atari products, the vector supplied must not be OxFF. All VME bus and system interrupts are independently maskable in the SCU.

Third parties should provide interrupt status bytes in the range 0x80-0xBF (i.e., vectors between 0x200 and 0x2FF).

**Clocks:**          SYSCLK is driven with a 16.107953 MHz clock in the TT030 and a 16.021226 MHz clock in the Mega STE. SERCLK and SERDAT* are not connected.

**ACFAIL*:**         The ACFAIL* signal is driven low by the system when the power supply is not stable. ACFAIL* will be asserted 1ms before the supply leaves the regulated range. It is driven by an open collector device, and pulled up by a 1K resistor.

**Address Modifiers:**  AM0, AM1, AM2, and AM4 are driven by the system. AM3 and AM5 are connected together and pulled up by a 1K resistor to VCC. This implementation allows Standard Supervisory and Non-Privileged Program and Data accesses and Short Supervisory and Non-Privileged Accesses. Block Transfers are not supported. LWORD* is pulled up by a 1K resistor but not otherwise driven.

**Miscellaneous:**   BERR* and SYSRES* are connected directly to the system bus error and reset signals. The bus error timer implemented on the system board will time out and generate a bus error if the card does not assert DTACK* within 255 cycles of 16MHz after the VME AS* falls. The SYSRES* generated when the 68030 executes a Reset instruction may be as short as 16us long. They are pulled up by 1.2K resistors and can be driven low by the system as well as by the card. The +5VSTDBY signal is connected to +5V. DTACK* is pulled up by a 1K resistor.

**Termination:**     10K pullups on the data bus. Other pullups are mentioned above. The remaining signals are not terminated, since this is a single slot system.

**Electrical Drive:**  All outputs have at least three LS TTL loads drive capability. Atari do not recommend loading any signal by more than this.

| | |
|---|---|
| Input load: | No signal represents more than two LS TTL loads. |
| Address space: | On the TT030, just under the entire 16Mb A24 space is available: |

FEOO 0000 - FEFE FFFF  A24:D16, VME card
sees least significant 24
bits of address

FEFF 0000 - FEFF FFFF  A16:D16

On the Mega STE, the address space is more limited to accommodate the existing ST memory map:

ʌᴑ 0000    - DE FFFF    A24:D16, VME card
sees all address bits
(i.e., there is no
translation or offset).

DF 0000    - DF FFFF    A16:D16

Power:

| Voltage | Max Current | Regulation | Ripple/Noise (pk-to-pk) |
|---|---|---|---|
| +5V | 2.0A | +5%/-4% | 60mV |
| +12V | 50mA | +/-5% | 120mV |
| -12V | 50mA | +/-10% | 120mV |

Future Atari products will variously support both 3U and 6U (A32/D32) cards, multiple slots, full drive and termination and alternate bus masters. VME card designers should therefore follow the specification completely. It is good design practice to provide strappable addresses, interrupt priorities and vectors and to decode all signals and buses as fully as possible. If cards are designed following these rules, they will work in future systems with little or no modification.

Vl.l  19 July 1991