TT030 Correction Pages

The Following pages should be inserted into your TT030 Service Guide replacing the existing pages. Remove the pages which contain the same page numbers and insert the correction pages in their place.

Atari TT030
Computer Field Service Manual
Part Number: C302483-001
REV B

Audio/Video Subsystem

- Bit Mapped video display using 32 Kbytes in ST™ mode and 153.6 Kbytes in TT™ mode of RAM relocatable anywhere in memory.
- Six available display modes:

  ST™ Mode:

  1. 320 X 200 16 out of 4096 colors
  2. 640 X 200 4 out of 4096 colors
  3. 640 X 400 monochrome

  TT™ Mode:

  1. 320 X 200 16 out of 4096 colors
  2. 640 X 200 4 out of 4096 colors
  3. 640 X 400 2 out of 4096 colors
  4. 640 X 480 16 out of 4096 colors
  5. 1280 X 960 monochrome
  6. 320 X 480 256 out of 4096 colors

- Monitor interfaces include:

  1. RGB
  2. ECL Monochrome

- Audio outputs internally mixed together:

  1. Programmable sound generator
  2. Stereo DMA sound

2.2 MAIN SYSTEM

The hardware contained in the main system of the Atari® TT030™ are the processor, optional coprocessor, ROM, RAM, Interrupt control (SCU and MFP), Memory, Timing and Bus control (MCU), DMA support (DMAC), and Real-time clock (MC146818).

2.2.1 Processor

The processor used in the Atari® TT030™ system is a 32 MHz Motorolar MC68030® with a 32-bit internal architecture, 32-bit external data bus, and a 32-bit address bus. This single chip contains a 68020 superset processor, a paged memory management unit, and independent data and instruction caches. The processor is clocked at 32 MHz.

2.2.2 Coprocessor

The TT030™ provides a Motorola® high performance MC68882 floating point coprocessor. The MC68882 coprocessor is clocked at 32 MHz. The processor recognizes the coprocessor as the standard floating point coprocessor ID of 1 in the 68030 CPU address space.

2.2.3 ROM

The system contains four 1 Mbit ROMs for a total of 512 Kbyte of access space. Since system bus access is 32-bits wide, all four ROMs must be present for proper operation. Included in the tasks the ROM performs is system initialization and boot code. The ROM also contains the TOS operating system.

2.2.4 RAM

The TT030™ includes 2 Mbytes of RAM used for both system and video. The RAM is implemented with 16 256 Kbit X 4 100 ns DRAMs set up to yield a 64-bit wide internal bus for high performance video access. Memory accesses to the RAM are interleaved between the Memory Controller and the Video Controller in 250ns time slices. During display cycles the processor is prevented from accessing the RAM. However, the processor will be allotted the next 250ns time slice.

The processor accesses the RAM through a 32-bit bus, even though the video system accesses the bus through a 64-bit wide architecture. The TT video chip (TTVIDEO) has on-chip buffering to provide very high bus bandwidths.

2.2.8.1 Clock Dividers

The clock dividers within the MCU are used to take the 16 MHz input and divide it into 4 MHz, 8 MHz, and 500 kHz clocks for use by other devices in the system.

2.2.8.2 Video Timing

MCU uses the input signals DE (Display Enable), VSYNC, and HSYNC from TTVIDEO to synchronize and control system video RAM refresh. There is also a read/write register within the MCU which is used to configure for 50, 60, or 71 Hz monitor operation (done by the Operating System).

2.2.8.3 Signal and Bus Arbitration

The MCU arbitrates the bus during DMA cycles to prevent the processor and DMA controller from interfering with each other.

2.2.8.4 Memory Control

The MCU takes addresses from the address bus and converts them to Row Address Strobe (RAS) and Column Address Strobe (CAS) signals to control all RAM accesses. The Memory Controller internal to this device is also responsible for refreshing the DRAM (dynamic RAM), loading the Video Shifter with display data, and sending or receiving data during DMA cycles.

2.2.8.5 Chip Selects

The MCU decodes addresses and generates chip selects to the 6850's, 68901 MFP, DMA Controller, Programmable Sound Generator, internal Memory Controller, and ROMs. It receives signals from the MFP, DMA, and Memory Controller to synchronize data transfers. The MCU also decodes the addresses necessary to enable the RAM and ROM.

2.2.9 Real-time Clock

The TT030™ system includes a Real-time Clock chip. When the system is powered on the real-time clock is powered by the main PCB power supply. In the event of a power failure, or when the system is powered off, the real-time clock is powered by a 3.6v lithium battery. This allows the date, time, and configuration data to be maintained even when there is no power to the unit. 50 bytes of battery backed-up RAM is also provided for storing diagnostic and configuration data.

The real-time clock provides time of day (down to one second resolution) and date. The RTC is provided with a 32.760 kHz oscillator that is independent of all other system clocks.

The chip is accessed through two consecutive word ports. The first word is a write-only port used to set the real-time clock chip address desired. The second word is the read-write data port. When doing a write to a clock chip register, a double word write can be performed. The first word would set the address, and the second word would load the data.

2.3 AUDIO/VIDEO SUBSYSTEM

2.3.1 Video Subsystem

The video subsystem consists of the video display memory (an arbitrary block of RAM starting on any word boundary), the MCU, a graphics control chip TTVIDEO, and some discrete components to drive the video output. The role of the MCU has already been covered in section 2.2.8.2

2.3.1.1 TTVIDEO

A video shifter is provided internal to the TTVIDEO chip. ST™ and TT™ modes of operation can be selected through the respective ST or TT Shift Mode Register. In the ST™ mode there are 16 color palette registers used in the shifter. All 16 may be used in low resolution (320 X 200) or TT mode (640 X 480).

Four may be used in medium resolution (640 X 200), and one may be used in monochrome (640 X 400) high resolution. Contained in each entry are twelve-bits of color; four-bits each for red, green, and blue. Therefore there are 16 X 16 X 16 or 4096 colors possible for each entry.

SECTION SEVEN

PARTS LIST AND ASSEMBLY DRAWINGS

Major Subassemblies

Main PCB Assemblies

ITEM	PART NUMBER	DESCRIPTION
41	CA400770-001	ASSY PCB TT030 32MHZ USA
41	CA400770-002	ASSY PCB TT030 32MHZ CAN
41	CA400770-003	ASSY PCB TT030 32MHZ UK
41	CA400770-004	ASSY PCB TT030 32MHZ FRA
41	CA400770-005	ASSY PCB TT030 32MHZ GER
41	CA400770-006	ASSY PCB TT030 32MHZ ITA
41	CA400770-007	ASSY PCB TT030 32MHZ NETH-UK
41	CA400770-008	ASSY PCB TT030 32MHZ NETH-FRA
41	CA400770-009	ASSY PCB TT030 32MHZ SPA
41	CA400770-010	ASSY PCB TT030 32MHZ SWG
41	CA400770-011	ASSY PCB TT030 32MHZ MEXICO
41	CA400770-012	ASSY PCB TT030 32MHZ SWD
41	CA400770-014	ASSY PCB TT030 32MHZ AUS
41	CA400770-020	ASSY PCB TT030 32MHZ SWF

Keyboard/Mouse Assemblies

ITEM	PART NUMBER	DESCRIPTION
	CA200182	MOUSE (TT030)
	CA400599-001	K/B TT030 USA
	CA400599-003	K/B TT030 UK
	CA400599-004	K/B TT030 FRE
	CA400599-005	K/B TT030 GER
	CA400599-006	K/B TT030 ITA
	CA400599-009	K/B TT030 SPA
	CA400599-010	K/B TT030 SWISS
	CA400599-012	K/B TT030 SWD

Disk Drives

1 Megabyte Drives

ITEM	PART NUMBER	DESCRIPTION
	C070004-001	SCREW SELF TAP M3*5
	C070004-003	SCREW SELF TAP PAN HD 3*8
	C070835-001	SCREW PAN HEAD W/WASHER M3*6
	C302401-001	BRKT FLOPPY DRIVE
	C301894-001	BRKT RETAINER LED
	C300973-001	LIGHT PIPE
	C398785-001	SLEEVE LED RUBBER
	C302014-001	FDD 1MB 3.5" EPSON
	C103558-201	FDD 1M FOR TT030 Alternate

2 Megabyte Drives

ITEM	PART NUMBER	DESCRIPTION
	C070004-001	SCREW SELF TAP M3*5
	C070004-003	SCREW SELF TAP PAN HD 3*8
	C070835-001	SCREW PAN HEAD W/WASHER M3*6
	C302401-001	BRKT FLOPPY DRIVE
	C301894-001	BRKT RETAINER LED
	C300973-001	LIGHT PIPE
	C398785-001	SLEEVE LED RUBBER
	C301371-101	FDD 2MB 3.5" EPSON

POWER SUPPLY

ITEM	PART NUMBER	DESCRIPTION
56	C302074-001	PSU PHIHONG PSM 5341 FCC

MEMORY

ITEM	PART NUMBER	DESCRIPTION
59	CA401058-001	ASSY 4 MEG TT RAM TT030
	CA401058-002	ASSY 16 MEG TT RAM TT030
58	CA401059-001	ASSY 2 MEG ST RAM TT030
	CA401059-002	ASSY 8 MEG ST RAM

TT030ROM SETS

ITEM	PART NUMBER	DESCRIPTION
U601,2,3,4	CA400836-001	TOS ROM ASSY TT030 USA
U601,2,3,4	CA400836-002	TOS ROM ASSY TT030 UK
U601,2,3,4	CA400836-004	TOS ROM ASSY TT030 FRA
U601,2,3,4	CA400836-005	TOS ROM ASSY TT030 GER
U601,2,3,4	CA400836-006	TOS ROM ASSY TT030 ITA
U601,2,3,4	CA400836-009	TOS ROM ASSY TT030 SPA
U601,2,3,4	CA400836-010	TOS ROM ASSY TT030 SWG
U601,2,3,4	CA400836-012	TOS ROM ASSY TT030 SWD
U601,2,3,4	CA400836-020	TOS ROM ASSY TT030 SWF

INTEGRATED CIRCUITS AND COMPONENTS

ITEM	PART NUMBER	DESCRIPTION
U409	C302096-001	IC AJAX FDD CONTROLLER 28P ST
U204	C398082-001	IC VIOEO SHIFTER PLCC 84P
U101	C398754-001	68882 COPROCESSOR 68P
57	C301020-001	BATTERY LITHIUM 3.6V 400MM

CABLE ASSEMBLIES

ITEM	PART NUMBER	DESCRIPTION
9	CA400335-001	ASSY CABLE DISK TT030
10	CA400336-001	ASSY CABLE FLOPPY TT030
	CA200237-017	ASSY CABLE FLAT 50 PIN INTERFACE

LED ASSEMBLIES

ITEM	PART NUMBER	DESCRIPTION
	CA400365-003	ASSY CABLE PWR/LED 550MM GREEN
	CA400365-002	ASSY CABLE HDD/LED 180MM YELLOW
	CA400972-001	CABLE PWR ASSY 150MM DISK DRIVE

SEPARATE ROMS

ITEM	PART NUMBER	DESCRIPTION
U601	C301925-004	TT.TOS 3.06 REV.D EE USA
U602	C301926-004	TT.TOS 3.06 REV.D OE USA
U604	C301927-004	TT.TOS 3.06 REV.D EO USA
U603	C301928-004	TT.TOS 3.06 REV.D OO USA
U601	C301929-004	TT.TOS 3.06 REV.D EE UK
U602	C301930-004	TT.TOS 3.06 REV.D OE UK
U604	C301931-004	TT.TOS 3.06 REV.D EO UK
U603	C301932-004	TT.TOS 3.06 REV.D OO UK
U601	C301933-005	TT.TOS 3.06 REV.E EE FRA
U602	C301934-005	TT.TOS 3.06 REV.E OE FRA
U604	C301935-005	TT.TOS 3.06 REV.E EO FRA
U603	C301936-005	TT.TOS 3.06 REV.E OO FRA
U601	C301937-005	TT.TOS 3.06 REV.E EE GER
U602	C301938-005	TT.TOS 3.06 REV.E OE GER
U604	C301939-005	TT.TOS 3.06 REV.E EO GER
U603	C301940-005	TT.TOS 3.06 REV.E OO GER
U601	C301941-003	TT.TOS 3.06 REV.C EE ITA
U602	C301942-003	TT.TOS 3.06 REV.C OE ITA
U604	C301943-003	TT.TOS 3.06 REV.C EO ITA
U603	C301944-003	TT.TOS 3.06 REV.C OO ITA
U601	C301945-004	TT.TOS 3.06 REV.D EE SPA
U602	C301946-004	TT.TOS 3.06 REV.D OE SPA
U604	C301947-004	TT.TOS 3.06 REV.D EO SPA
U603	C301948-004	TT.TOS 3.06 REV.D OO SPA
U601	C301949-005	TT.TOS 3.06 REV.E EE SWF
U602	C301950-005	TT.TOS 3.06 REV.E OE SWF
U604	C301951-005	TT.TOS 3.06 REV.E EO SWF
U603	C301952-005	TT.TOS 3.06 REV.E OO SWF
U601	C301953-005	TT.TOS 3.06 REV.E EE SWG
U602	C301954-005	TT.TOS 3.06 REV.E OE SWG
U604	C301955-005	TT.TOS 3.06 REV.E EO SWG
U603	C301956-005	TT.TOS 3.06 REV.E OO SWG
U601	C301957-004	TT.TOS 3.06 REV.D EE SWD
U602	C301958-004	TT.TOS 3.06 REV.D OE SWD
U604	C301959-004	TT.TOS 3.06 REV.D EO SWD
U603	C301960-004	TT.TOS 3.06 REV.D OO SWD

MECHANICAL ASSEMBLIES

ITEM	PART NUMBER	DESCRIPTION
12	C300740-001	TOP CASE
	CA400417-001	ASSY VME FILLER PANEL
8	C070012	RUBBER FOOT
18	C300739-001	BTM CASE
14	C301910-001	SHIELD REAR TTO30
15	CA400311-001	ASSY PCB VME BACKPLANE TT030
	C300738-001	BRKT VME HOUSING
17	C300977-001	PCB INSULATOR
55	CA400414-001	ASSY SPEAKER/SHIELD TT030
57	CA400361-002	ACCESSORY COVER PLASTIC
57	CA400361-001	ASSY HDD COVER TT030
	C300838-001	SHIELD CART TOP
	C070613-003	NYLON WASHER 3.1*2T
	C398751-002	HEX STAND OFF M2.6*0.45P*10L

SECTION EIGHT

SCHEMATICS AND PCB SILKSCREEN

SECTION NINE

GLOSSARY OF PART NAMES AND TERMS

BUS ERROR	Logic has asserted BERR to inform the processor that there is a problem with the current cycle. This could be due to a device not responding (for example, CPU tries to read memory but the Memory Controller fails to assert DSACK), or an illegal access (attempting to write to ROM). A bus error causes exception processing.
CPU	The 68030 microprocessor.
DMA	Direct memory access. Process in which data is transferred from external storage device to RAM, or from RAM to external storage. Transfer is very fast, takes place independent of the CPU, so the CPU can be processing while DMA is taking place. MCU arbitrates the bus between the CPU and DMA.
DMA CONTROLLER	Atari proprietary chip which controls the DMA process. All disk I/O goes through this device.
EXCEPTION	A state in which the processor stops the current activity, saves what it will need to resume the activity later in RAM, fetches a vector (address) from RAM, and starts executing at the address vector. When the exception processing is done, the processor will continue what it was doing before the exception occurred. Exceptions can be caused by interrupts, instructions, or error conditions. See also Section Two, System Errors, or a 68030 reference for more detail.
HALT	State in which the CPU is idle, all bus lines are in the high-impedence state, and can only be ended with a RESET input. This is a bi-directional pin on the CPU. It is driven externally by the RESET circuit on power-up or a reset button closure, and internally when a double bus fault occurs. A double bus fault is an error during a sequence which is run to handle a previous error. For example, if a bus error occurs, and during the exception processing for the bus error, another bus error occurs, then the CPU will assert STATUS.

HSYNC	Timing signal for the video display. Determines when the horizontal scan is on the screen, and when it is blank (retracing). The synchronization (approx. every 63 microseconds) also is encoded onto IPL1,2 as an interrupt to the CPU.
INTERRUPT	A request by a device for the processor to stop what it is doing and perform processing for the device. It is a type of exception. Interrupts are maskable in software, meaning they will be ignored if they do not meet the current priority level of the CPU. There are three priorities: the highest are MFP interrupts, then VSYNC interrupts, and lowest are HSYNC interrupts. Interrupts are signaled to the CPU on the Interrupt Priority Level inputs (IPL0-2). See Theory of Operation, Main System, MFP, and MCU.
MCU	Atari proprietary chip which handles all RAM accesses. See Theory of Operation, Main System and Video Subsystem for details.
MIDI	Musical Instrument Digital Interface. An electrical standard by which electronic instruments communicate. Also, the logical system for such communication. In the TT030™, consists of a 6850 communications chip, driver and receiver chips (74LS04, 74LS05, and PC-900 photocoupler), and an MFP interrupt channel.
MFP	Multi-function Peripheral, also 68901. Interrupt control, timers, and USART for RS232 communication. See Theory of Operation, Main System.
PSG	Programmable Sound Generator, also YM2149. Yamaha version of General Instruments AY-3-8910. Has two 8 bit I/O ports and three sound channels. Used in parallel port and audio.
RS232C	Electical standard for serial digital communication. Also the physical and logical device which performs communication using this standard. In the STr computers, consists of the MFP, PSG, 1488, and 1489 chips.
1772	Western Digital Floppy Disk Controller.

6850	Also ACIA (Asynchronous Communication Interface Adapter). Interfaces between 8 bit parallel bus and serial communication bus. In the ST™, there are two 6850s, one for keyboard communication, and one for MIDI communication.
68901	See MFP.
Supervisor Mode	State of the CPU in which it is allowed to access all hardware and RAM locations, and perform some privileged instructions. Determined by the state of a bit in the Status Register. The operating system operates in supervisor mode, and switches to user mode before passing control to an application (although the application can enter supervisor mode if it wishes).
User Mode	State of the CPU in which certain instructions and areas in the memory map are disallowed (resulting in a privilege violation exception if attempted). See also SUPERVISOR MODE.
VSYNC	Signal used for vertical synchronization of CRT display device. Occurs at 70 Hz (monochrome), or 50 or 60 Hz color.
YM2149	See PSG.