REV	REVISIONS DESCRIPTION	DATE	APPROVED
1	ENG REL PER ERC E0204C	9/22/83	

CONFIDENTIAL

[redacted]

CA062174	1400XL
CA024357-001	1450XL
NEXT ASSY	USED ON

DRAWN BY PMS DATE 6/4/83

CHECKED PMS 6/4/83

ENGINEER Pearce 6/4/83

APPROVED [signature] 9/9/83

APPROVED [signature] 9/12/83

ATARI®

Atari, Inc.
30 E. Plumaria Drive
San Jose, CA 95134

A Warner Communications Company

TITLE MCU - MEMORY CONTROL UNIT, FREDDIE

SIZE	DRAWING NO.	REV
A	C061922	1

SCALE

SHEET 1 OF 10

1.0 SCOPE

1.1 General

This specification covers the detail requirements for an electronic component.

2.0 APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the issue in effect on date of latest revision of this specification shall apply.

2.1 Atari Documents

C099901 Qualification, Reliability Requirements for Integrated Circuits and Discrete Semiconductors.

C099902 Handling of Devices Susceptible to Static Discharge.

C099931 40-Lead Dual in-line package.

2.2 ANSI Y32.14-1973 Logic Diagrams, Graphic Symbols for.

3.0 REQUIREMENTS

3.1 Electrical Requirements - See Table I thru IV and Figures I and II.

3.1.1 Absolute Maximum Ratings in Free Air. Exceeding the "absolute maximum ratings," may result in failure or permanent damage to the part. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Logic Function

Logic functions shall be as depicted in Figure (NA) as defined by American National Standards Institute Y32.14.

3.3 Marking

The part shall be marked with manufacturer's name or logo, type number, lot date code (on top), and Pin Number 1 identification.

3.4 Pin Assignment

Pin assignment shall be depicted in Figure I when related to package configuration in drawing.

3.5 Package Configuration

Package configuration shall conform to the requirements of drawing C099931 Dual in-line package.

3.6 Vendor Screen

Vendor screen shall conform to the Specification C099901. Burn-in circuit Figure III shall be used, 48 hrs. at 125 ^{o}C.

3.7 Package for Shipment

All parts shipped to this specification shall be packed in accordance with C099901 and C099902 to prevent physical damage, corrosion, static discharge and deterioration during shipment.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Vendor Qualification

Must meet the Atari Specification C099901, "Qualification, Reliability Requirements for Integrated Circuits and Discrete Semiconductors".

Functional Description

"Freddie RAM" is a custom LSI chip providing dynamic RAM control functions of the Atari "XL" home-computer products. It replaces a number of SSI and MSI TTL parts, including a custom delay line. Freddie RAM multiplexes 16-bit address bus into 8-bit row and 8-bit column address, and generates precisely timed row and column address strobes. Freddie RAM will be supplied in a 40-pin DIP with pin numbers shown below.

Pin Number Name Description (Apostrophe (') denotes active-low)

DRAM Outputs

These multiplexed DRAM address bus outputs provide for direct connection to 64 K x 1 dynamic RAMs, selected from Intel 2164-20, Fujitsu MB 8264-20, Hitachi HM4864-3, NEC MPD 4164-2, Toshiba TMM 4164-4, Motorola MCM 6665A-20, or to 16 K x 4 dynamic RAMS, selected from Texas Instruments TMS 4416-20.

		Row	Column
32	RA0	A0	A14*
31	RA1	A1	A8
30	RA2	A2	A9
29	RA3	A3	A10
28	RA4	A4	A11
27	RA5	A5	A12
26	RA6	A6	A13
25	RA7	A7	A15*

* Note: These bits are ignored by 16Kx4 RAMs; they allow for possible 64Kx1 applications.

33	RAS'	DRAM Row address strobe output. A negative transition on this line indicates that RA0-RA7 contain a valid Row Address.
35	CAS'	DRAM column address strobe output. A negative transition on this line indicates that RA0-RA7 contain a valid Column Address.
36	16KCAS'	DRAM column address strobe output for first 16K only. Same as CAS' for addresses 0000-3FFF; always high for addresses 4000-FFFF. In Atari 600 with16K RAM, this line connects to RAM chips; CAS' connects to PBI.
34	Wrt'	WRITE' output to DRAM. This (transparent-) latched version of R/W' becomes stable shortly after R/W' and remains stable until after RAS' and CAS' have risen. See timing diagram.

Memory Map Qualifier Inputs

3	ExtSel'	External Select input from parallel bus. Low forces CAS' high (immediately, asynchronously)
4	CasInh'	CAS-Inhibit input. Similar to ExtSel' but latched. When CasInh' is low at beginning of cycle, CAS' is kept high for complete cycle.

Miscellaneous Pins

40	Vdd	Power (+5 volts)
20	Gnd	Ground (0 volts)
8-19 21-24	A0-A11 A12-A15	Address bus input from CPU and ANTIC
38	R/W'	Read/Write' input from CPU
39	Reset'	Reset input. A negative-going transition on this line sets the Wrt' latch high (read mode), sets the CasInh' latch to inhibit CAS'. This may take several Phi2 cycles. The chip then begins normal operation (without waiting for Reset' to rise again).

An internal inverter between pins 1 and 2 provides for direct connection to a 14.31818 MHz parallel-resonant, AT-cut crystal. Alternately, external clock square-wave may be input to pin 2.

1	XTAL/ClkOut	Output to crystal
2	XTAL/ClkIn	Input from crystal or Ext. clock input
37	OSC	3.579545 MHz output to GTIA
5	Phi2	Clock "Phi2" input from 6502 CPU
7	OE'	"Output Enable" output.
6	LE'	"Latch Enable" output.

Pins 6 and 7 provide control signals for use with an optional equivalent replacement for the PIA Port B register, as follows:

OE'	LE'	Function
L	L	Reset
L	H	Read
H	L	Write
H	H	Hold

Required Operating Environment

Vdd	4.75	5.25	v	Power Supply Voltage
Tamb	0	70	C	Ambient temperature
VIH	3.5	5.0	V	Input High voltage (XTAL/ClkIn input only)
VIH	2.0	5.0	V	Input High voltage (all other Inputs)
VIL	-0.3	0.8	V	Input Low voltage
fOSC	14.31817	14.31819	MHz	Crystal Frequency
tCYC	559	560	ns	Phi2 Period
tLPhi2	250	320	ns	Phi2 low time
tRWV		145	ns	Phi2 falling to R/W' Valid
tABV		145	ns	Phi2 falling to Address Bus Valid
tRV		145	ns	Phi2 falling to Ref' Valid
tRWC	30		ns	Phi2 falling (again) to R/W' Change
tABC	30		ns	Phi2 falling (again) to Address Bus Change
tRC	30		ns	Phi2 falling (again) to Ref' Change
tCIS		250	ns	Setup: Phi2 falls to CI' valid
tCIH	370		ns	CI' hold time after Phi2 falling
tESS		260	ns	ExtSel' setup after Phi2 falling
tESC	40		ns	Setup, ExtSel' to CAS' would fall
tESH	0		ns	ExtSel' hold time after CAS' rising

Operational Characteristics & Propagation Delays

Propagation delays are measured from when input crosses 1.5 v until output crosses 1.5 v.

Pd	0	500	mW	Power Dissipation
Cin	0	10	pF	Input Capacitance (all inputs)
Iin	-10	+10	uA	Input leakage current (0 < Vin < 5 v)
VOL	0	0.4	V	Output low voltage (Isink <= 1.6 mA)
VOH	2.4	5.0	V	Output high voltage (Isource <= 0.1 mA)
tR,tF	0	15	nS	Output rise, fall times (CL <= 80 pF).
tARA	0	60	ns	Address bus to RAM Address pins
tASR	0		ns	Row Address Setup to RAS' falling
tRAH	30		ns	Row Address Hold after RAS' falling
tRSH	200		ns	RAS' low time
tRP	135		ns	RAS' high time
tRF	210	305	ns	Phi2 falling to RAS' Falling (read, write, or refresh cycle)
tCR	10	100	ns	Phi2 falling to CAS' rising (from previous cycle)
tCRP	0		ns	CAS' rising (from previous cycle) to RAS' falling
tCAS	135		ns	CAS' low time
tCPN	35		ns	CAS' high time
tRCD	80		ns	RAS' falling to CAS' falling
tCFR	300	370	ns	Phi2 falling to CAS' Falling (read cycle)
tCFW	425		ns	Phi2 falling to CAS' Falling (write cycle)
tASC	0		ns	Column Address Setup before CAS' falling
tCAH	80		ns	Column Address Hold after CAS' falling
tAR	135		ns	Column Address Hold after RAS' falling
tWRCS	0		ns	Wrt' setup before CAS' falls
tWCH	80		ns	Wrt' hold after CAS' falls
tRCH	0		ns	Wrt' hold after both RAS' and CAS' have risen
tRWWRT		50	ns	R/W' to Wrt' (transp. latch loading)
tLEF	240	360	ns	Phi2 falls to LE' falls, D301 Write
tLER	440	600	ns	Phi2 falls to LE' rises
tOEF	240	450	ns	Phi2 falls to OE' falls, D301 read
tOER	570	660	ns	Phi2 falls to OE' rises

Note: tESS(max) and tCFR(min) are specified so that an external parallel device has adequate time, after ExtEn becomes valid, to assert ExtSel' at least tESC before CAS would fall.

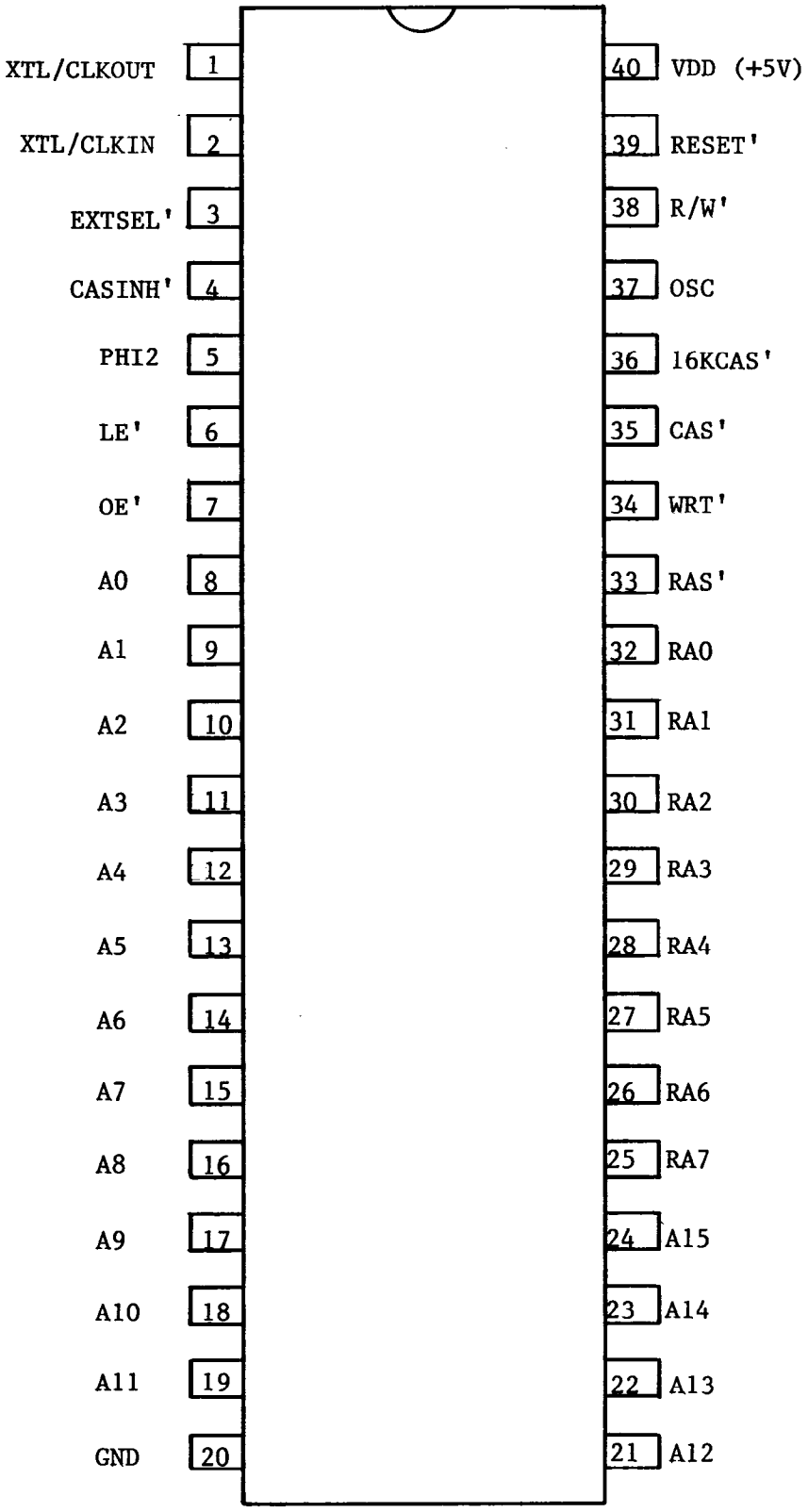


FIGURE 1 - PIN DIAGRAM

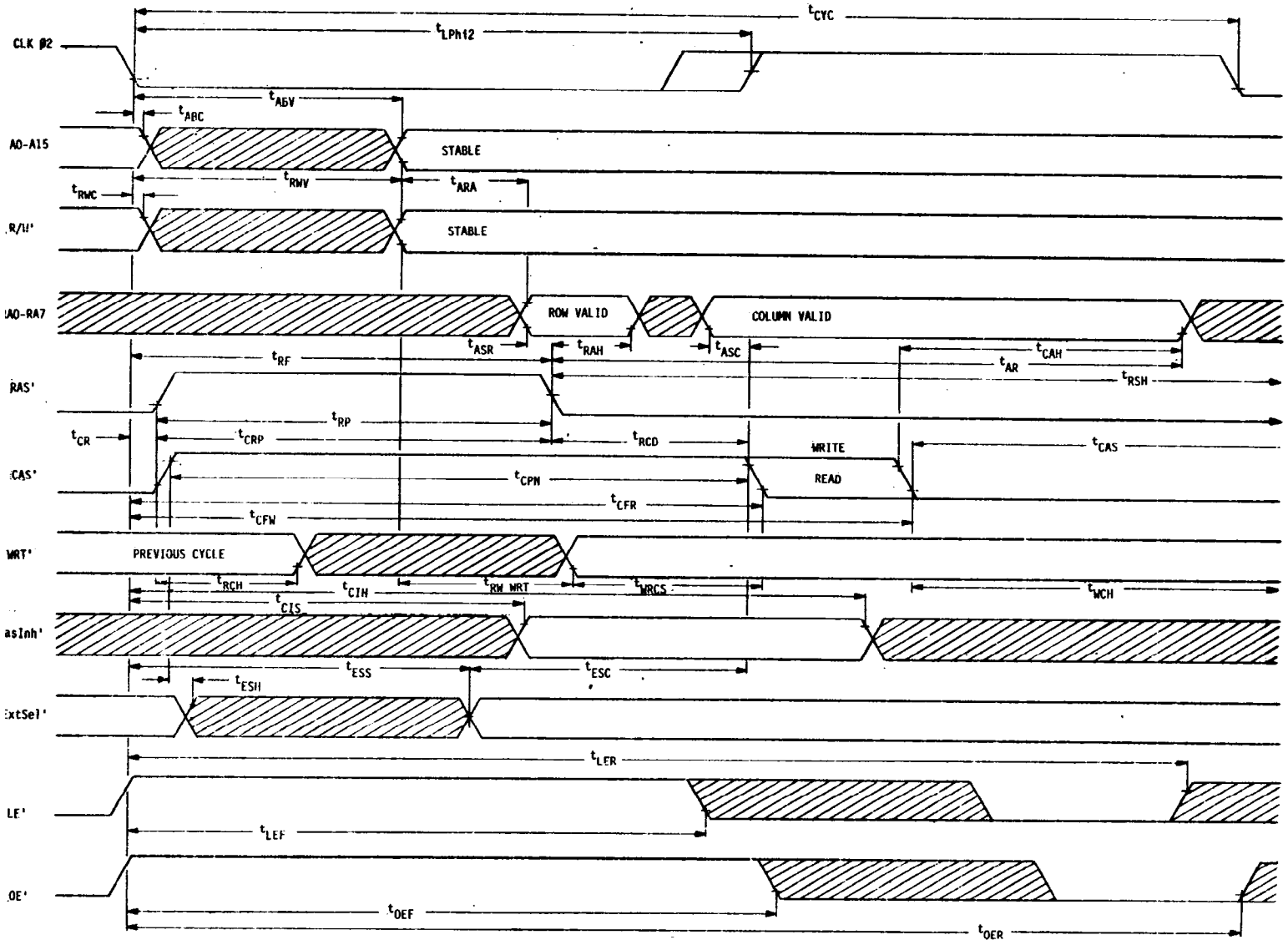
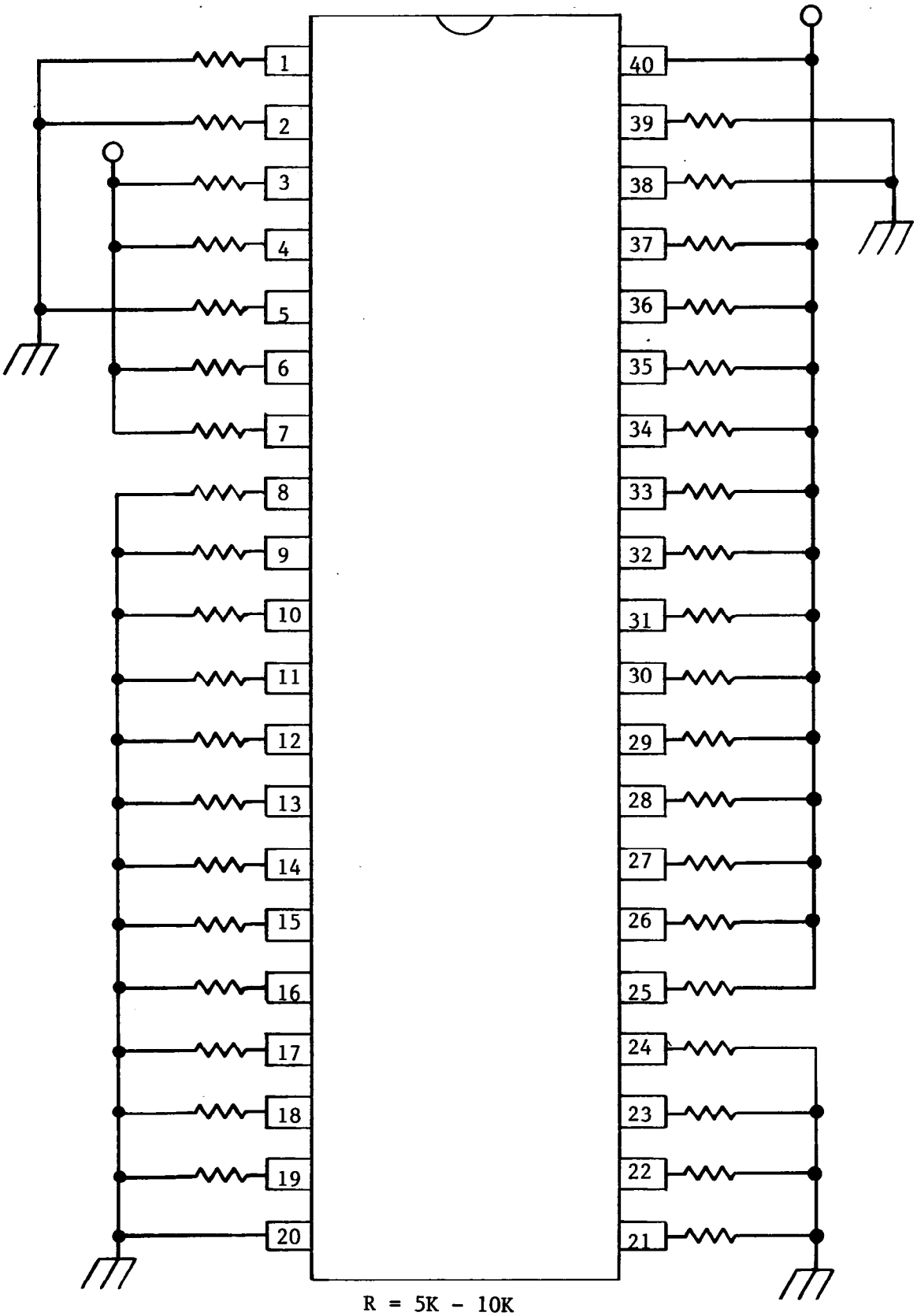

CLK Ø2
A0-A15
R/W'
RA0-RA7
RAS'
CAS'
WRT'
asInh'
ExtSel'
LE'
OE'
PREVIOUS CYCLE
STABLE
STABLE
ROW VALID
COLUMN VALID
WRITE
READ
tCYC
tLPh12
tABV
tABC
tRWV
tRWC
tARA
tRF
tASR
tRAH
tASC
tCAH
tAR
tRSH
tRP
tCR
tCRP
tRCD
tCAS
tCPN
tCFR
tCFW
tRCH
tCIH
tRW WRT
tWRCS
tWCH
tCIS
tESS
tESC
tESH
tLER
tLEF
tOEF
tOER

FIGURE 2



R = 5K - 10K

ANY CHANGES TO THIS CIRCUIT MUST BE APPROVED BY ATARI ENGINEERING

FIGURE 3 - BURN-IN CIRCUIT

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