REV	REVISIONS DESCRIPTION	DATE	APPROVED

NEXT ASSY	USED ON

DRAWN BY DATE

CHECKED

ENGINEER 12/4/84
Randy Hoopar

APPROVED

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ATARI®

ATARI CORP.
1196 Borregas
Sunnyvale, CA 94086

TITLE
IC;CMOS MMU

SIZE	DRAWING NO.	REV
A	CO61618A-XX	A

SCALE	SHEET 1 OF 11

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1.0 SCOPE

This specification covers the electrical, packaging, marking, and quality requirements for a proprietary integrated circuit device. The component is for use in some of ATARI's 8-bit 6502 based computers. Its primary function is memory management and it is called, appropriately, a Memory Management Unit (MMU). This document addresses CMOS versions of the device. Bipolar Hard Array Logic (HAL) and Programmable Array Logic (PAL) versions are covered in C061618.

2.0 APPLICABLE DOCUMENTS

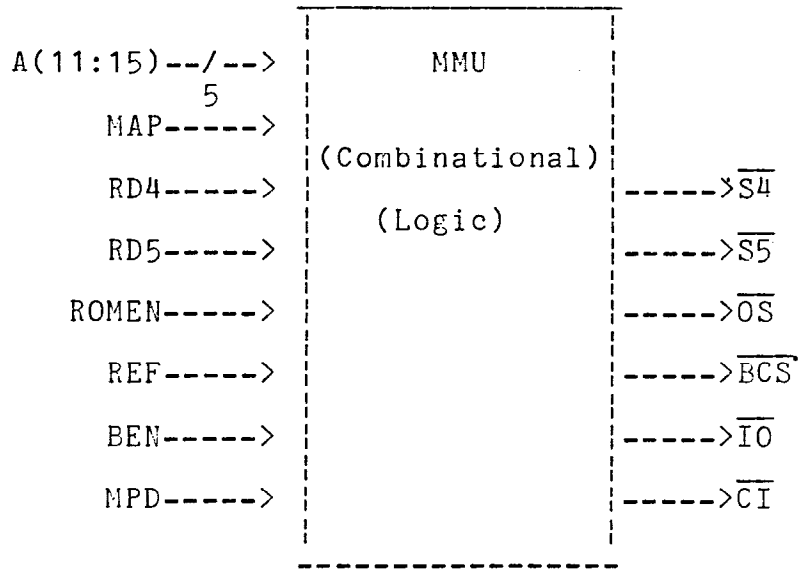
The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the issue in effect on date of latest revision of this specification shall apply.

2.1 ATARI Documents

C099901	Qualification, Reliability Acceptance Specification for - Discrete Semiconductors and Integrated Circuits.
C099931	20-Lead, Dual in-line package.

3.0 ELECTRICAL REQUIREMENTS

3.1 Functional Block Diagram



3.2 Logic Equations

$\overline{S4}$ (19) = $\overline{A13}$*$\overline{A14}$*A15*RD4*REF

$\overline{S5}$ (12) = A13*$\overline{A14}$*A15*RD5*REF

$\overline{BCS}$ (13) = A13*$\overline{A14}$*A15*$\overline{RD5}$*$\overline{BEN}$*REF

$\overline{IO}$ (17) = $\overline{A11}$*A12*$\overline{A13}$*A14*A15*REF

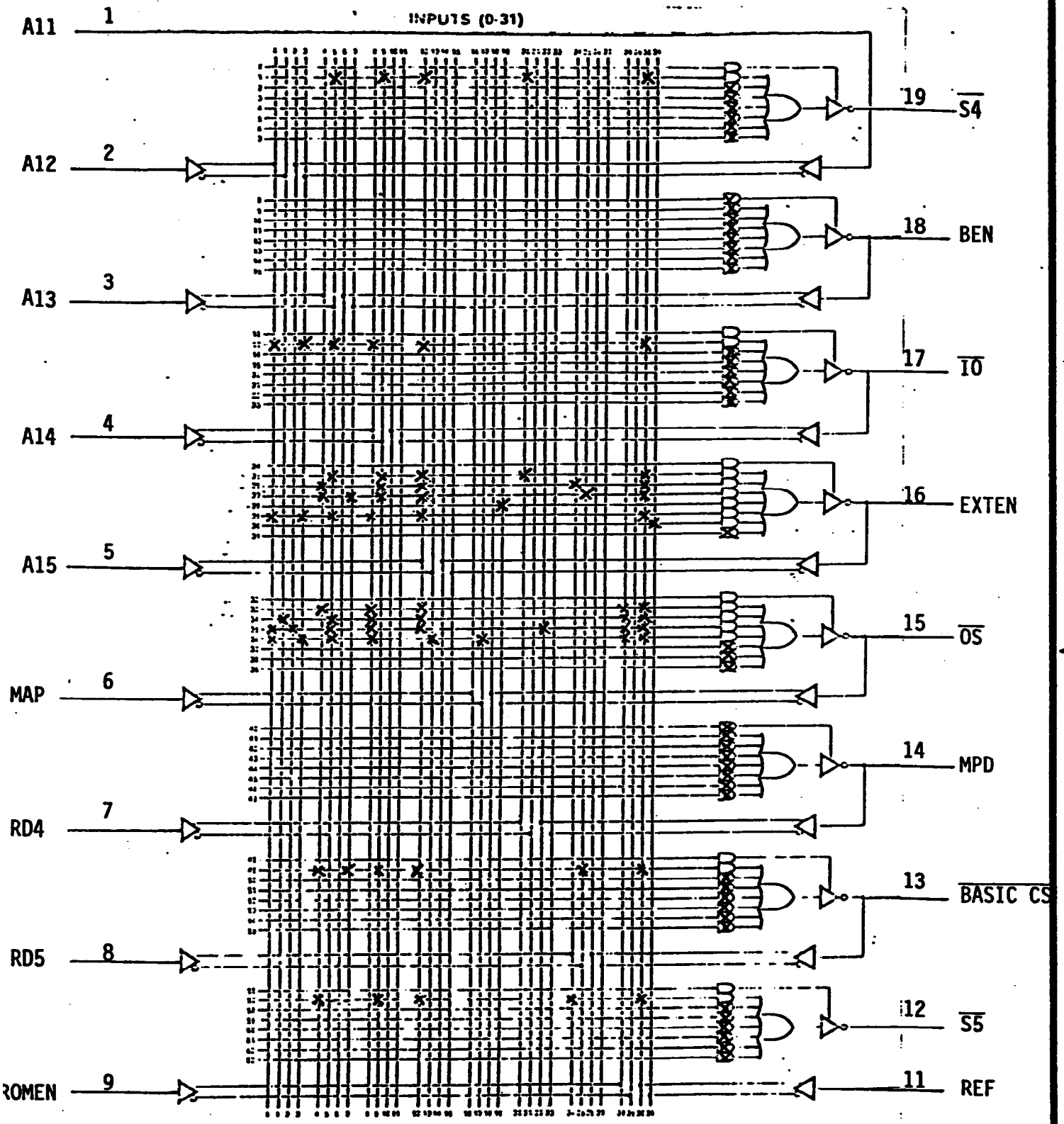
$\overline{OS}$ (15) = A13*A14*A15*ROMEN*REF
+ $\overline{A12}$*A14*A15*ROMEN*REF
+ A11*A12*$\overline{A13}$*A14*A15*ROMEN*MPD*REF
+ $\overline{A11}$*A12*$\overline{A13}$*A14*$\overline{A15}$*ROMEN*$\overline{MAP}$*REF

$\overline{CI}$ (16) = $\overline{A13}$*$\overline{A14}$*A15*RD4*REF
+ A13*$\overline{A14}$*A15*RD5*REF
+ A13*$\overline{A14}$*A15*$\overline{RD5}$*$\overline{BEN}$*REF
+ OS
+ $\overline{A11}$*A12*$\overline{A13}$*A14*A15*REF
+ $\overline{REF}$

LOGIC CONVENTION: When the right hand side of an equation is true or Logic 1, the left hand side is a Logic 0.

3.3 PAL Fuse Map (For Information Only)

Logic Diagram HAL16LB



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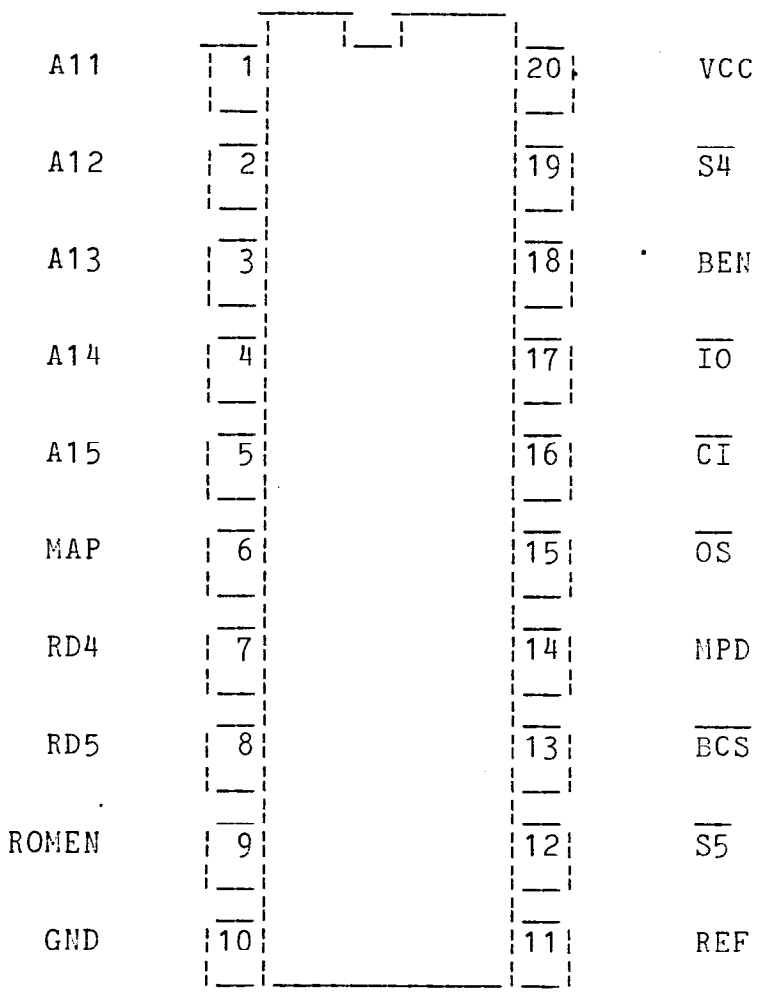
3.4 Pin Assignment

Pin assignment shall be depicted as follows when related to package configuration.



3.5 Absolute Maximum Ratings

Absolute Maximum ratings in Free Air. Exceeding the "absolute maximum ratings", may result in failure or permanent damage to the part. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

	Operating
Supply Voltage V_{CC}	7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	-65 to 150 degrees C
Output short circuit duration	Infinite

3.6 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	4.75	5.25	V
High-level output current (source)	I_{OH}		-3.2	mA
Low-level output current (sink)	I_{OL}		4.0	mA
Operating free air temperature	T_A	0	70	°C

3.7 DC Electrical Characteristics (TA=0 degrees C TO 70 degrees C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High-level input voltage	V_{IH}		2.0		V
Low-level input voltage	V_{IL}			0.8	V
High-level output voltage	V_{OH}	V_{CC}=MIN, V_{IH}=2.0V V_{IL}=0.8, I_{OH}=MAX	2.4		V
Low-level output voltage	V_{OL}	V_{CC}=MIN, V_{IH}=2.0V V_{IL}=0.8, I_{OL}=MAX		0.5	V
Input current at max input voltage	I_I	V_{CC}=MAX, V_I=5.5V		1.0	mA
High-level input current	I_{IH}	V_{CC}=MAX, V_I=2.4V		10	uA
Low-level input current	I_{IL}	V_{CC}=MAX, V_I=0.4V		-10	uA
Quiescent Current [1]	Iccq	Vdd=MAX		100	uA
Operating Current	Icco	Vdd=5V+/-5%		10	mA

1 - Measured with inputs at Vdd or Vss, outputs floating

3.8 Switching Characteristics
(TA=0 degrees C TO 70 degrees C, VCC=5.0V =/- 5%)

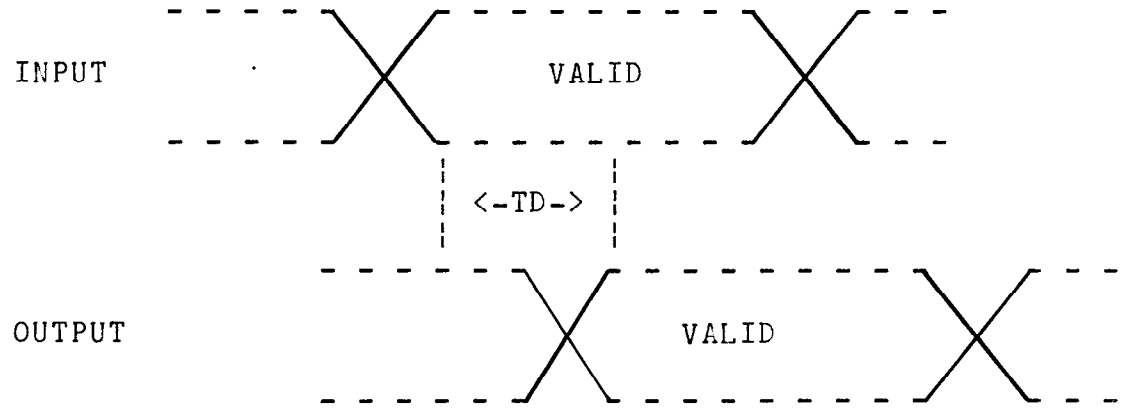
PARAMETER	SYMBOL	MAX	UNIT
Input valid to output valid pins 12, 13, 15, 19	tpd	40	ns
Input valid to output valid pin 17	tpd	35	ns
Input valid to output valid pin 16	tpd	70	ns

*Inputs are pins 1-9, 11, 14, 18

*C_L = 45pF

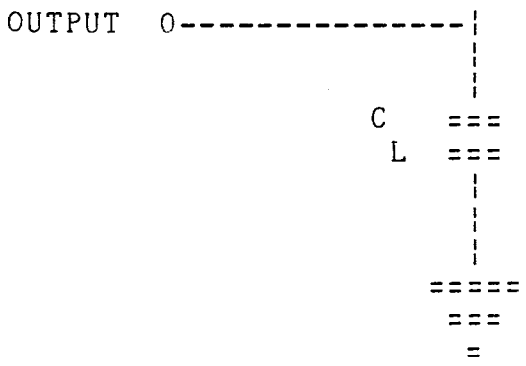
See Standard Test Load and Definition of Waveforms below.

SWITCHING WAVEFORMS



NOTES:
1. All voltages measured with respect to Pin 10 (VSS) of device.
2. Outputs are guaranteed stable after maximum specified delays.

AC TEST LOAD



NOTES:

1. Typical limits are at VCC=5.0V and T_A =25degrees C

2. tpd is tested with C_L = 45pF

4.0 PACKAGE CONFIGURATION

Package configuration shall conform to the requirements of drawing C099931 Dual in-line package.

5.0 MARKING

The part shall be marked with manufacturer's name or logo, type number, lot date code, and Pin Number 1 identification. Lot date code shall be on top.

6.0 QUALITY ASSURANCE PROVISIONS

Must meet the ATARI Specification C099901, "Qualification, Reliability Acceptance Specification".

7.0 PACKAGE FOR SHIPMENT

All parts shipped to this specification shall be packed in accordance with C099901 to prevent physical damage, corrosion, static discharge and deterioration during shipment.