PAL A 1400

BASIC MEMORY MAP DECODER

A ' mark denotes an active low signal.

1. BA15 (I) BUFFERED ADDRESS 15
2. BA14 (I) BUFFERED ADDRESS 14
3. BA13 (I) BUFFERED ADDRESS 13
4. BA12 (I) BUFFERED ADDRESS 12
5. BA11 (I) BUFFERED ADDRESS 11
6. RD4' (I) FROM CARTRIDGE SLOT, ADDRESS 8000-9FFF
7. RD5' (I) FROM CARTRIDGE SLOT, ADDRESS A000-BFFF
8. REF' (I) REFRESH SIGNAL FROM ANTIC
9. ROMEN (I) PIA B-PORT BIT 7. OS ROM ENABLED WHEN HIGH.
10. GROUND
11. BASICEN'(I) PIA B-PORT BIT 1. ENABLES INTERNAL BASIC ROM WHEN LOW
12. RAMINH' (O) ACTIVE LOW WHEN ANY ROM IS ACTIVE.
13. MAP' (I) PIA B-PORT BIT 0. ENABLES SELF TEST CODE AT 5000-57FF WHEN LOW
14. MPE (I) FROM PALC1400 ENABLES MATH PACK WHEN NO PARALLEL BUS HANDLER IS ACTIVE
15. BASIC CS' (O) CHIP SELECT FOR INTERNAL BASIC ROM
16. OS' (O) CHIP SELECT FOR OS ROM
17. DXXX' (O) ENCODED ADDRESS FOR PALC1400
18. S5' (O) SELECT FOR CARTRIDGE ROM
19. S4' (O) SELECT FOR CARTRIDGE ROM
20. VCC

PAL B 1400

PBI GLUE DECODER (B)

A ' mark denotes an active low signal.

1. A765' (I) ADDRESSES 7,6 & 5
2. BA4 (I) BUFFERED ADDRESS 4
3. BA3 (I) BUFFERED ADDRESS 3
4. BA2 (I) BUFFERED ADDRESS 2
5. BA1 (I) BUFFERED ADDRESS 1
6. BA0 (I) BUFFERED ADDRESS 0
7. DS0' (I) DEVICE SELECT 0 FROM PALC1400 D1FFWR LATCH
8. DS1' (I) DEVICE SELECT 1 FROM PALC1400 D1FFWR LATCH
9. D1XX' (I) D1XX ENCODED ADDRESS
10. GROUND
11. BR/W' (I) BUFFERED R/W FROM CPU
12. ACIACS' (O) ACIA CHIP SELECT
13. BPHI2 (I) PHASE 2 CLOCK INPUT
14. REF' (I) REFRESH FROM ANTIC
15. MODEM LTCH' (O) STROBE FOR MODEM CONFIGURATION LATCH
16. VOTRAX LTCH' (O) STROBE FOR VOTRAX DATA HOLD REG.
17. VOTRAX STB' (O) STROBE FOR VOTRAX DATA.
18. D1FFWR' (O) STROBE FOR DEVICE SELECT LATCH IN PALC1400 AND PBI.
19. D1FFRD' (O) READ SIGNAL FOR PBI INTERRUPT REG.
20. VCC

PAL C 1400

DEVICE SELECT LATCH

A ' mark denotes an active low signal.

1. DIFFWR' (I) STROBE FROM PALB1400 FOR DEVICE SELECT LATCH
2. BA11 (I) BUFFERED ADDRESS 11
3. DXXX' (I) ENCODED ADDRESS DXXX
4. PBID7 (I) PARALLEL BUS DATA BIT 7
5. PBID1 (I) PARALLEL BUS DATA BIT 1
6. EXTSEL' (I) EXTERNAL SELECT FROM PBI.
7. ACIACS' (I) ACIACS FROM PALB1400.
8. D1XX' (I) ENCODED ADDRESS D1XX
9. REF' (I) REFRESH LINE FROM ANTIC
10. GROUND
11. GND (I) INTERNAL LATCH OUTPUT ENABLE, GROUNDED
12. RESET' (I) SYSTEM RESET LINE
13. PBIDEN' (O) PARALLEL BUS DATA DRIVER ENABLE
14. UNUSED LATCH OUTPUT
15. UNUSED LATCH OUTPUT
16. DS1' (O) DEVICE SELECT 1
17. DS0' (O) DEVICE SELECT 0
18. MPE (O) MATH PACK ENABLE, ACTIVE WHEN DS0 & DS1 ARE BOTH HIGH
19. HANDLERCS' (O) CHIP SELECT FOR HANDLER ROM
20. VCC

1400 PAL 'A' EQUATIONS

S4' = A15*A14'*A13'*RD4*REF' 8000-9FFF

S5' = A15*A14'*A13*RD5*REF'*~~BASICEN~~ A000-BFFF

DXXX' = A15*A14*A13'*A12*REF'

CS' = ROMEN*A15*A14*A13*REF' E000-FFFF OS ROM
+ ROMEN*A15*A14*A13'*A12'*REF' C000-CFFF OS ROM
+ ROMEN*A15*A14*A13'*A12*A11*MPE*REF' D800-DFFF MATH PACK
+ ROMEN*A15'*A14*A13'*A12*A11'*REF'*MAP 5000-57FF SELF TEST

BASICCS' = A15*A14'*A13*REF'*BASICEN*RD5' A000-BFFF

RAMINH = A15*A14'*A13'*RD4*REF' S4
+ A15*A14'*A13*RD5*BASICEN'*REF' S5
+ A15*A14'*A13*REF'*BASICEN*RD5' BASIC
+ A15*A14*A13'*A12*A11'*REF' I/O
+ OS (SEE ABOVE EQUATION)
+ REF

1400 PAL 'B' EQUATIONS

D1FFRD' = D1XX*A765*A4*A3*A2*A1*A0*R/W'*BPHI2*REF'

D1FFWR' = D1XX*A765*A4*A3*A2*A1*A0*R'/W*BPHI2*REF'

VOTRAXLTCH' = D1XX*A4'*A3'*A2'*BPHI2*REF'*DS0 D100-D103

VOTRAXSTB' = D1XX*A4'*A3'*A2*BPHI2*REF'*DS0 D104-D107

MODEMLTCH' = D1XX*A4'*A3*A2'*BPHI2*REF'*DS1 D108-D10B

ACIACS' = D1XX*A4'*A3*A2*REF'*DS1 D10C-D10F

1400 PAL 'C' EQUATIONS

HANDLERCS' = (DXXX*A11*DS0*REF') + (DXXX*A11*DS1*REF')

MPE = HANDLERCS (ATTACHED TO ENABLE OF OUTPUT)

DS0' = D1FFWR'*PBD0*RESET (LATCHED BIT)

DS1' = D1FFWR'*PBD1*RESET (LATCHED BIT)

PBIDEN' = (D1XX*ACIACS'*REF') + EXTSEL