T-49-17-06

UMC

UM6502/07/12

8-bit Microprocessor

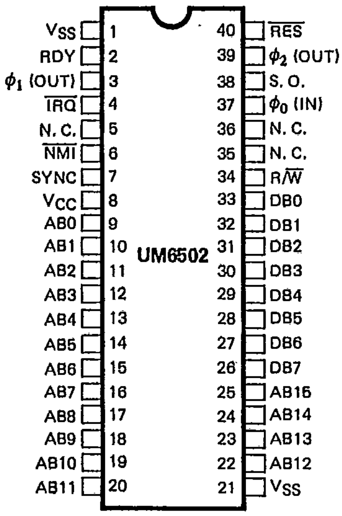
Features

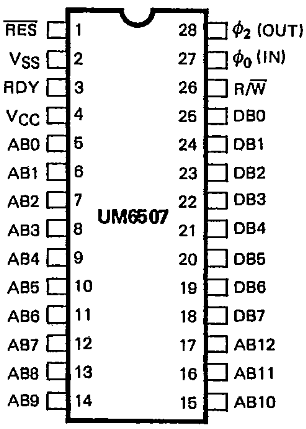
- Single 5V ± 5% power supply
- N channel, silicon gate, depletion load technology
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Bi-directional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1MHz, 2MHz, 3MHz and 4MHz versions
- On-chip clock options
  - —External single clock input
  - —Crystal time base input
- Pipeline architecture

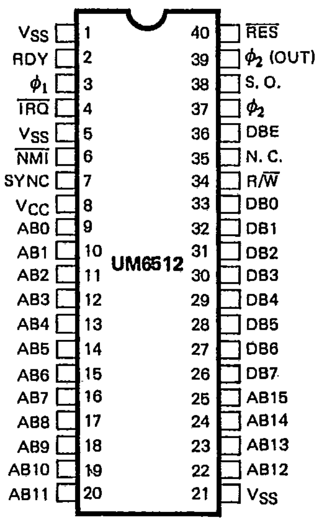
General Description

The UM6502/07/12 microprocessors are totally software compatible with one another. These products provide a wide selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. The UM6502/07 on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The UM6512 external clock version is geared to multiprocessor system applications where maximum timing control is mandatory. These products are bus compatible with the MC6800.

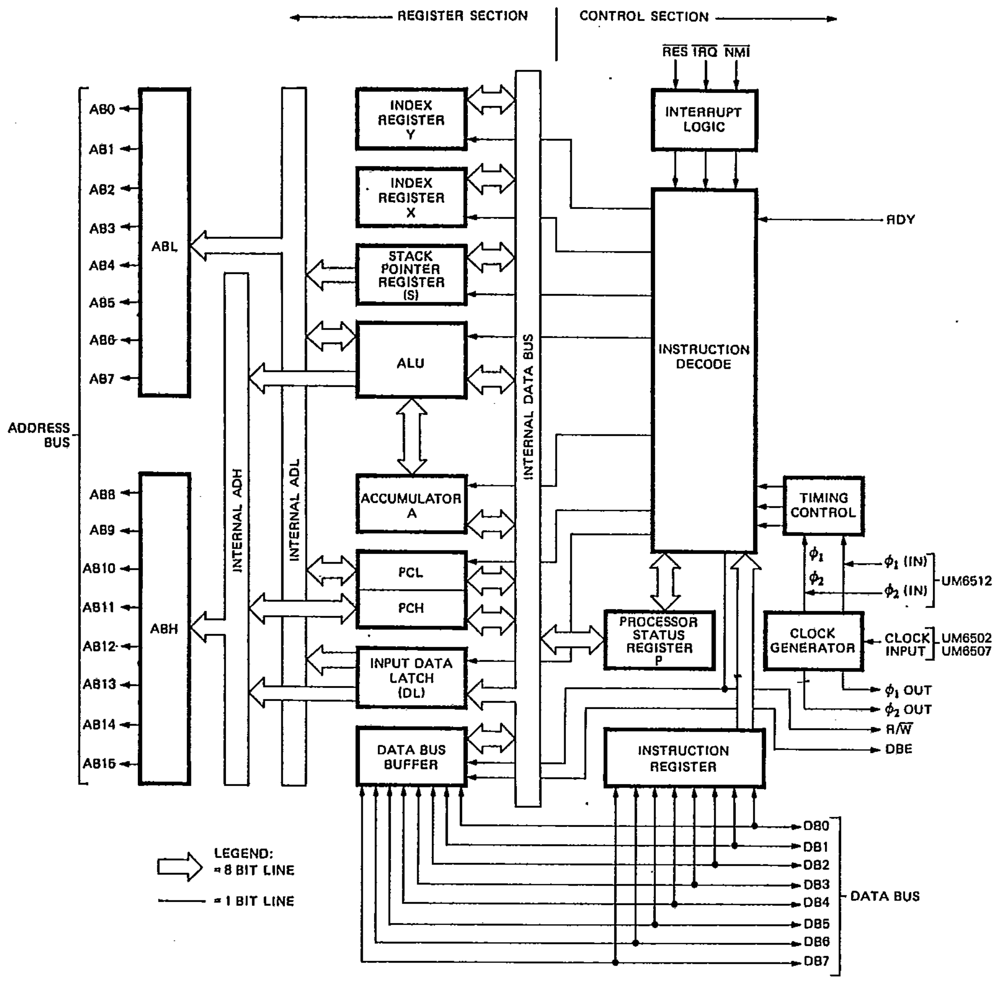
Pin Configurations







Block Diagram



Notes:
1. CLOCK GENERATOR IS NOT INCLUDED ON UM6512
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH PRODUCT

Absolute Maximum Ratings*

Supply Voltage V_{CC} .... −0.3 to +7.0V
Input Voltage V_{IN} .... −0.3 to +7.0V
Operating Temperature T_A .... 0 to 70°C
Storage Temperature T_{STG} .... −55 to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C)
(ϕ_1, ϕ_2 applies to UM6512, ϕ_0 (in) applies to UM6502/UM6507)

Symbol	Characteristics	Min.	Max.	Units
V_{IH}	Input High Voltage Logic and ϕ_0 (in) for UM6502/UM6507 — 1, 2, 3 MHz 4 MHz ϕ_1 and ϕ_2 only for UM6512 — All Speeds	 +2.0 +3.3 V_{CC} – 0.5	 V_{CC} V_{CC} V_{CC} + 0.25	 V V V
V_{IL}	Input Low Voltage Logic, ϕ_0(in) (UM6502/UM6507) ϕ_1, ϕ_2 (UM6512)	 –0.3 –0.3	 +0.8 +0.2	 V
I_{IL}	Input Loading (V_{IN} = 0V, V_{CC} = 5.25V) RDY, S.O.	 –10	 –300	 μA
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = 0) Logic (Excl. RDY, S.O.) ϕ_1, ϕ_2 (UM6512) ϕ_0(In) (UM6502/UM6507)	 – – –	 2.5 100 10.0	 μA μA μA
I_{TSI}	Three-State (Off State) Input Current (V_{IN} = 0.4 to 2.4V, V_{CC} = 5.25V) DB0-DB7	 –	 ±10	 μA
V_{OH}	Output High Voltage (I_{LOAD} = –100μAdc, V_{CC} = 4.75V) 1, 2 MHz SYNC, DB0-DB7, AB0-AB15, R/$\overline{W}$	2.4	–	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = 4.75V) 1, 2 MHz SYNC, DB0-DB7, AB0-AB15, R/$\overline{W}$	–	0.4	V
P_D	Power Dissipation 1MHz and 2MHz (V_{CC} = 5.25V)	–	700	mW
C C_{IN} C_{OUT} C_{ϕ_0} (In) C_{ϕ_1} C_{ϕ_2}	Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz) $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE DB0-DB7 AB0-AB15, R/$\overline{W}$, SYNC ϕ_0 (in) (UM6502/UM6507) ϕ_1 (UM6512) ϕ_2 (UM6512)	 – – – – – –	 10 15 12 15 50 80	 pF

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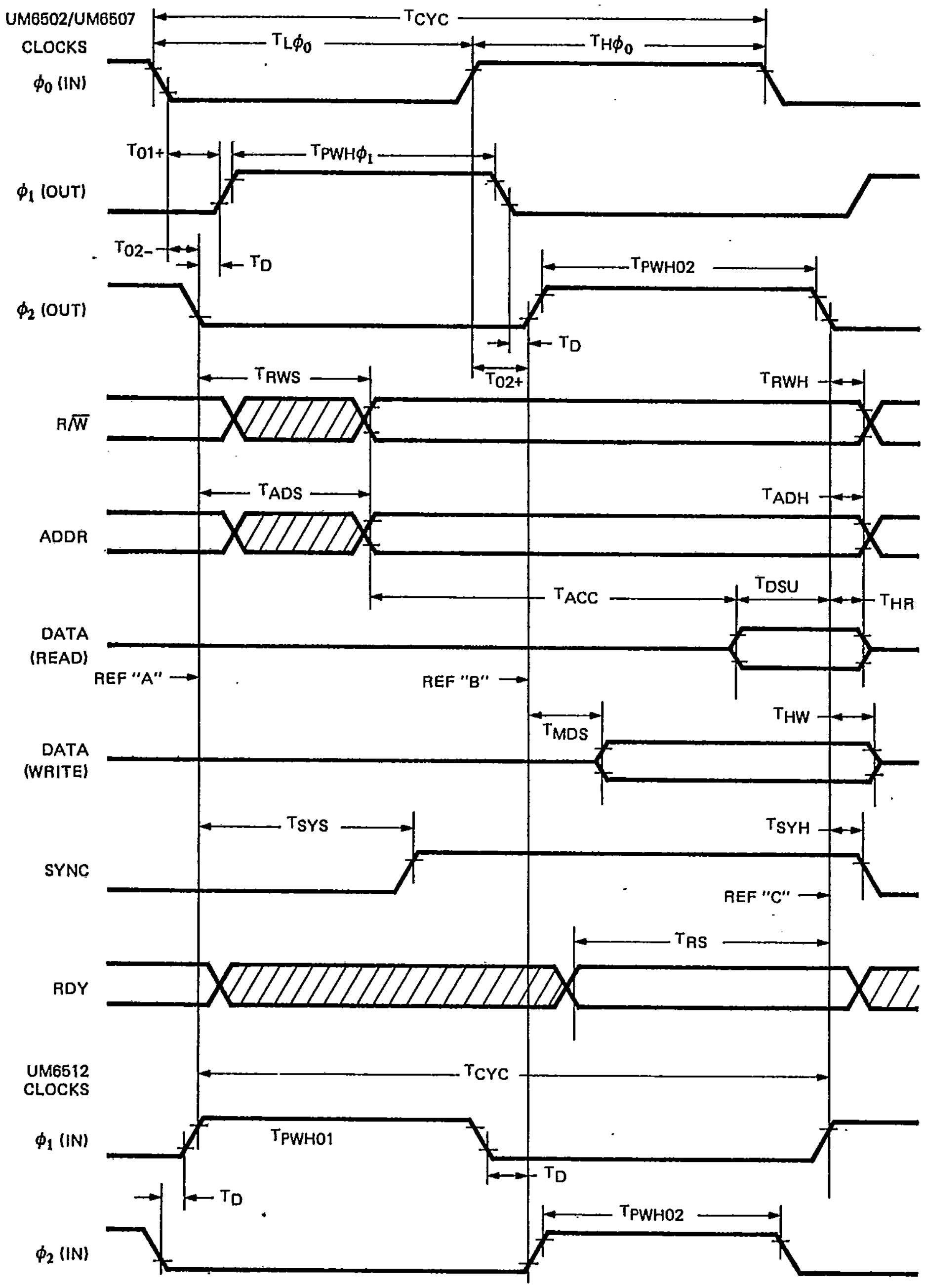
Timing Waveforms



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Dynamic Operating Characteristics

(V_{CC} = 5.0 ± 5%, T_A = 0° to 70°C)

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
UM6512										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	µs
ϕ_1 Pulse Width	$T_{PWH\phi_1}$	430	–	215	–	150	–			ns
ϕ_2 Pulse Width	$T_{PWH\phi_2}$	470	–	235	–	160	–			ns
Delay Between ϕ_1 and ϕ_2	T_D	0	–	0	–	0	–			ns
ϕ_1 and ϕ_2 Rise and Fall Times(1)	T_R, T_F	0	25	0	20	0	15			ns
UM6502/UM6507										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	µs
ϕ_0(IN) Low Time(2)	$T_{L\phi_0}$	480	–	240	–	160	–	110	–	ns
ϕ_0(IN) High Time(2)	$T_{H\phi_0}$	460	–	240	–	160	–	115	–	ns
ϕ_0 Neg to ϕ_1 Pos Delay(5)	T_{01+}	10	70	10	70	10	70	10	70	ns
ϕ_0 Neg to ϕ_2 Neg Delay(5)	T_{02-}	5	65	5	65	5	65	5	65	ns
ϕ_0 Pos to ϕ_1 Neg Delay(5)	T_{01-}	5	65	5	65	5	65	5	65	ns
ϕ_0 Pos to ϕ_2 Pos Delay(5)	T_{02+}	15	75	15	75	15	75	15	75	ns
ϕ_0(IN) Rise and Fall Time(1)	T_{RO}, T_{FO}	0	30	0	20	0	15	0	10	ns
ϕ_1 (OUT), Pulse Width	$T_{PWH\phi_1}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	$T_{L\phi_0}$-20	$T_{L\phi_0}$	ns
ϕ_2 (OUT), Pulse Width	$T_{PWH\phi_2}$	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	$T_{L\phi_0}$-40	$T_{L\phi_0}$-10	ns
Delay Between ϕ_1 and ϕ_2	T_D	5	–	5	–	5	–	5	–	ns
ϕ_1 and ϕ_2 Rise and Fall Times(1, 3)	T_R, T_F	–	25	–	25	–	15	–	15	ns
UM6502/UM6507/UM6512										
R/W Setup Time	T_{RWS}	–	225	–	140	–	110	–	90	ns
R/W Hold Time	T_{RWH}	30	–	30	–	15	–	10	–	ns
Address Setup Time	T_{ADS}	–	225	–	140	–	110	–	90	ns
Address Hold Time	T_{ADH}	30	–	30	–	15	–	10	–	ns
Read Access Time	T_{ACC}	–	650	–	310	–	170	–	110	ns
Read Data Setup Time	T_{DSU}	100	–	50	–	50	–	50	–	ns
Read Data Hold Time	T_{HR}	10	–	10	–	10	–	10	–	ns
Write Data Setup Time	T_{MDS}	20	175	20	100	20	75	–	70	ns
Write Data Hold Time	T_{HW}	60	150	60	150	30	130	20	–	ns
Sync Setup Time	T_{SYS}	–	350	–	175	–	100	–	90	ns
Sync Hold Time	T_{SYH}	30	–	30	–	15	–	15	–	ns
RDY Setup Time(4)	T_{RS}	200	–	200	–	150	–	120	–	ns

Notes:

1. Measured between 10% and 90% points.
2. Measured at 50% point.
3. Load = 1 TTL load + 30 pF.
4. RDY must never switch states within T_{RS} to end of ϕ_2.
5. Load = 100 pF.
6. The 2 MHz devices are identified by an "A" suffix.
7. The 3 MHz devices are identified by a "B" suffix.
8. The 4 MHz devices are identified by a "C" suffix.

Timing Diagram Note:

Because the clock generation for the UM6502/UM6507 and UM6512 is different, the two clock timing sections are referenced to the main timing diagram by three reference lines marked REF 'A', REF 'B' and REF 'C'. Reference between the two sets of clock timings is without meaning. Timing parameters referring to these line and scale variations in the diagrams are of no consequence.

Pin Description

Clocks (ϕ_1, ϕ_2)
The UM6512 requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The UM6502/UM6507 clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

Address Bus (AB0-AB15)
(See sections on each micro processor for respective address lines on these devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (DB0-DB7)
Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)
This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from the microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable the data bus drivers externally, DEB should be held low. This signal is available on the UM6512 only.

Ready (RDY)
This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during, or coincident with phase one, (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMs as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read operation. Ready transitions must not be permitted during ϕ_2 time.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At the time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ resistor to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S. O.)
A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1.

SYNC
This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OPCODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset ($\overline{RES}$)
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signals will become valid. When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Read/Write (R/$\overline{W}$)
This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/$\overline{W}$ signifies data into the processor; a low is for the data transfer out of the processor.

Programming Characteristics

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set	ORA	"OR" Memory with Accumulator
BEQ	Branch on Result Zero	PHA	Push Accumulator on Stack
BIT	Test Bits in Memory with Accumulator	PHP	Push Processor Status on Stack
BMI	Branch on Result Minus	PLA	Pull Accumulator from Stack
BNE	Branch on Result not Zero	PLP	Pull Processor Status from Stack
BPL	Branch on Result Plus	ROL	Rotate One Bit Left (Memory or Accumulator)
BNK	Force Break	ROR	Rotate One Bit Right (Memory or Accumulator)
BVC	Branch on Overflow Clear	RTI	Return from Interrupt
BVS	Branch on Overflow Set	RTS	Return from Subroutine
CLC	Clear Carry Flag	SBC	Subtract Memory from Accumulator with Borrow
CLD	Clear Decimal Mode	SEC	Set Carry Flag
CLI	Clear Interrupt Disable Bit	SED	Set Decimal Mode
CLV	Clear Overflow Flag	SEI	Set Interrupt Disable Status
CMP	Compare Memory and Accumulator	STA	Store Accumulator in Memory
CPX	Compare Memory and Index X	STX	Store Index X in Memory
CPY	Compare Memory and Index Y	STY	Store Index Y in Memory
DEC	Decrement Memory by One	TAX	Transfer Accumulator to Index X
DEX	Decrement Index X by One	TAY	Transfer Accumulator to Index Y
DEY	Decrement Index Y by One	TSX	Transfer Stack Pointer to Index X
EOR	"Exclusive-OR" Memory with Accumulator	TXA	Transfer Index X to Accumulator
INC	Increment Memory by One	TXS	Transfer Index X to Stack Pointer
INX	Increment Index X by One	TYA	Transfer Index Y to Accumulator
INY	Increment Index Y by One		
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

ADDRESSING MODES

Accumulator Addressing
This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing
In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing
In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero Page Addressing
The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in a significant increase in code efficiency.

Indexed Zero Page Addressing – (X, Y indexing)
This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location on page zero. In addition due to the "Zero Page" addressing

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nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing – (X, Y indexing)
This form of addressing is used in conjunction with the X and Y index registers and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index, or count value, and the instruction to contain the base address. This type of indexing allows any location reference and the index to modify multiple fields, resulting in reduced coding and execution time.

Implied Addressing
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing
Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

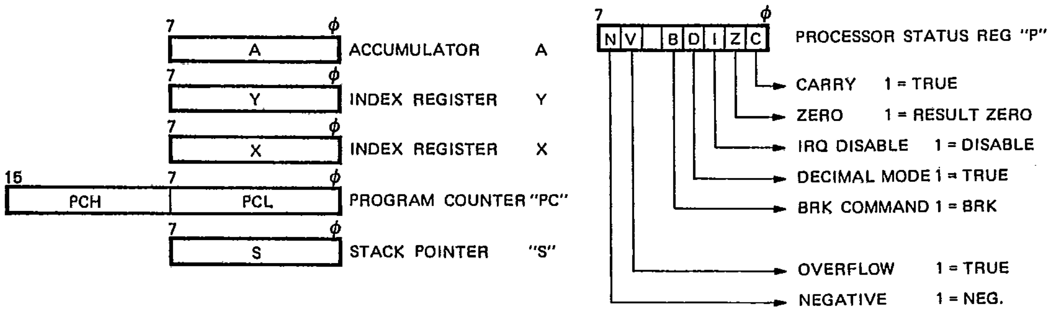
The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set to the next instruction. The range of the offset is-128 to + 127 bytes from the next instruction.

Indexed Indirect Addressing
In indexed indirect addressing (referred to as "Indirect, X"), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location on page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be on page zero.

Indirect Indexed Addressing
In indirect indexed addressing (referred to as "Indirect, Y"), the second byte of the instruction points to a memory location on page zero. The content of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Absolute Indirect
The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The content of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

PROGRAMMING MODEL



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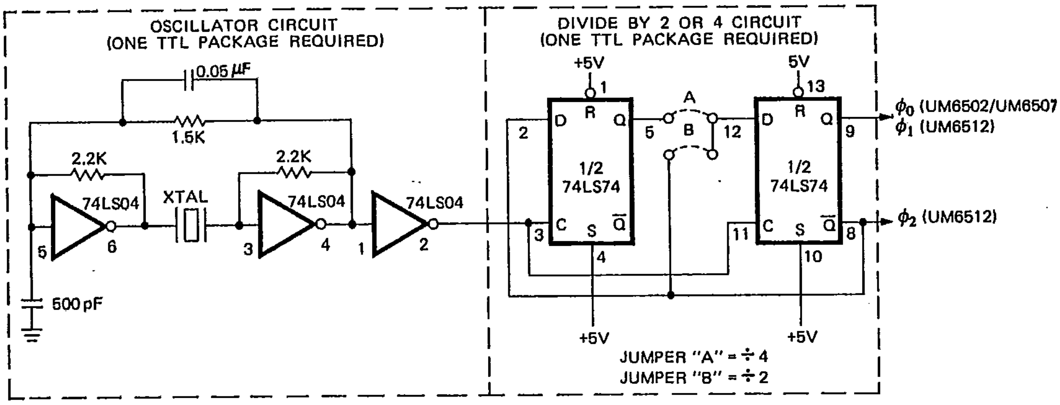
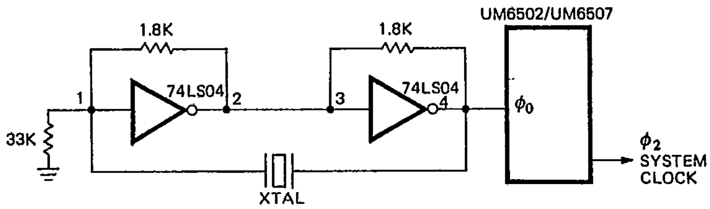
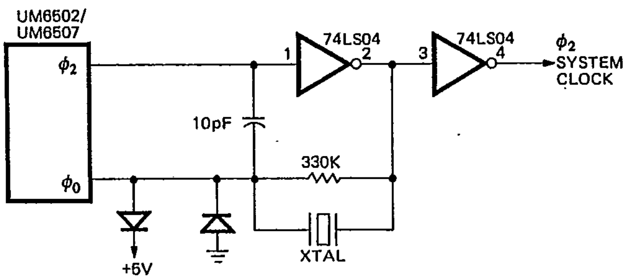
Clock Generation Circuits*

* Crystals used are CTS Knight MP Series or equivalents. (Series Mode)



Crystal Frequency	Output Frequency	
	÷2	÷4
3.579545 MHz	1.7897 MHz	0.894886 MHz
4.194304 MHz	2.097152 MHz	1.048576 MHz





Instruction Set

Instructions		Immediate			Absolute			Zero page			Accum.			Implied			(Ind. X)			((Ind. Y)		
Mnemonic	Operation	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC	A+M+C→A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2
AND	A∧M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2
ASL	C←[7 0]←0				0E	6	3	06	5	2	0A	2	1									
BCC	BRANCH ON C=0 (2)																					
BCS	BRANCH ON C=1 (2)																					
BEQ	BRANCH ON Z=1 (2)																					
BIT	A∧M				2C	4	3	24	3	2												
BMI	BRANCH ON N=1 (2)																					
BNE	BRANCH ON Z=0 (2)																					
BPL	BRANCH ON N=0 (2)																					
BRK	BREAK													00	7	1						
BVC	BRANCH ON V=0 (2)																					
BVS	BRANCH ON V=1 (2)																					
CLC	0→C													18	2	1						
CLD	0→D													D8	2	1						
CLI	0→1													58	2	1						
CLV	0→V													B8	2	1						
CMP	A−M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2
CPX	X−M	E0	2	2	EC	4	3	E4	3	2												
CPY	Y−M	C0	2	2	CC	4	3	C4	3	2												
DEC	M−1→M				CE	6	3	C6	5	2												
DEX	X−1→X													CA	2	1						
DEY	Y−1→Y													88	2	1						
EOR	A∨M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2
INC	M+1→M				EE	6	3	E6	5	2												
INX	X+1→X													E8	2	1						
INY	Y+1→Y													C8	2	1						
JMP	JUMP TO NEW LOC				4C	3	3															
JSR	JUMP SUB				20	6	3															
LDA	M A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2												
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2												
LSR	0→[7 0]→C				4E	6	3	46	5	2	4A	2	1									
NOP	NO OPERATION													EA	2	1						
ORA	A∨M→A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2
PHA	A→Ms S−1→S													48	3	1						
PHP	P→Ms S−1→S													08	3	2						
PLA	S+1→S Ms→A													68	4	1						
PLP	S+1→S Ms→P													28	4	1						
ROL	←[7 0]←[C]←				2E	6	3	26	5	2	2A	2	1									
ROR	[C]→[0 7]→				6E	6	3	66	5	2	6A	2	1									
RTI	RTRN INT													40	6	1						
RTS	RTRN SUB													60	6	1						
SBC	A−M−C̄→A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2
SEC	1→C													38	2	1						
SED	1→D													F8	2	1						
SEI	1→1													78	2	1						
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2
STX	X→M				8E	4	3	86	3	2												
STY	Y→M				8C	4	3	84	3	2												
TAX	A→X													AA	2	1						
TAY	A→Y													A8	2	1						
TSX	S→X													BA	2	1						
TXA	X→A													8A	2	1						
TXS	X→S													9A	2	1						
TYA	Y→A													98	2	1						

(1) ADD 1 TO N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

Microprocessor

Z Page,X OP	Z Page,X n	Z Page,X #	Abs. X OP	Abs. X n	Abs. X #	Abs. Y OP	Abs. Y n	Abs. Y #	Relative OP	Relative n	Relative #	Indirect OP	Indirect n	Indirect #	Z Page. Y OP	Z Page. Y n	Z Page. Y #	7 N	6 V	5 .	4 B	3 D	2 I	1 Z	0 C	Mnemonic
75	4	2	7D	4	3	79	4	3										N	V	.	.	.	.	Z	C	ADC
35	4	2	3D	4	3	39	4	3										N	.	.	.	.	.	Z	.	AND
16	6	2	1E	7	3													N	.	.	.	.	.	Z	C	ASL
									90	7	2							.	.	.	.	.	.	.	.	BCC
									B0	2	2							.	.	.	.	.	.	.	.	BCS
									F0	2	2							.	.	.	.	.	.	.	.	BEQ
																		M_7	M_6	.	.	.	.	Z	.	BIT
									30	2	2							.	.	.	.	.	.	.	.	BMI
									D0	2	2							.	.	.	.	.	.	.	.	BNE
									10	2	2							.	.	.	.	.	.	.	.	BPL
																		.	.	.	1	.	1	.	.	BRK
									50	2	2							.	.	.	.	.	.	.	.	BVC
									70	2	2							.	.	.	.	.	.	.	.	BVS
																		.	.	.	.	.	.	.	0	CLC
																		.	.	.	.	0	.	.	.	CLD
																		.	.	.	.	.	0	.	.	CLI
																		.	0	.	.	.	.	.	.	CLV
D5	4	2	DD	4	3	D9	4	3										N	.	.	.	.	.	Z	C	CMP
																		N	.	.	.	.	.	Z	C	CPX
																		N	.	.	.	.	.	Z	C	CPY
D6	6	2	DE	7	3													N	.	.	.	.	.	Z	.	DEC
																		N	.	.	.	.	.	Z	.	DEX
																		N	.	.	.	.	.	Z	.	DEY
55	4	2	5D	4	3	59	4	3										N	.	.	.	.	.	Z	.	EOR
F6	6	2	FE	7	3													N	.	.	.	.	.	Z	.	INC
																		N	.	.	.	.	.	Z	.	INX
																		N	.	.	.	.	.	Z	.	INY
												6C	5	3				.	.	.	.	.	.	.	.	JMP
																		.	.	.	.	.	.	.	.	JSR
B5	4	2	BD	4	3	B9	4	3										N	.	.	.	.	.	Z	.	LDA
						BE	4	3							B6	4	2	N	.	.	.	.	.	Z	.	LDX
B4	4	2	BC	4	3													N	.	.	.	.	.	Z	.	LDY
56	6	2	5E	7	3													0	.	.	.	.	.	Z	C	LSR
																		.	.	.	.	.	.	.	.	NOP
15	4	2	1D	4	3	19	4	3										N	.	.	.	.	.	Z	.	ORA
																		.	.	.	.	.	.	.	.	PHA
																		.	.	.	.	.	.	.	.	PHP
																		N	.	.	.	.	.	Z	.	PLA
																		(RESTORED)								PLP
36	6	2	3E	7	3													N	.	.	.	.	.	Z	C	ROL
76	6	2	7E	7	3													N	.	.	.	.	.	Z	C	ROR
																		(RESTORED)								RTI
																		.	.	.	.	.	.	.	.	RTS
F5	4	2	FD	4	3	F9	4	3										N	V	.	.	.	.	Z	(3)	SBC
																		.	.	.	.	.	.	.	1	SEC
																		.	.	.	.	1	.	.	.	SED
																		.	.	.	.	.	1	.	.	SEI
95	4	2	9D	5	3	99	5	3										.	.	.	.	.	.	.	.	STA
															96	4	2	.	.	.	.	.	.	.	.	STX
94	4	2																.	.	.	.	.	.	.	.	STY
																		N	.	.	.	.	.	Z	.	TAX
																		N	.	.	.	.	.	Z	.	TAY
																		N	.	.	.	.	.	Z	.	TSX
																		N	.	.	.	.	.	Z	.	TXA
																		.	.	.	.	.	.	.	.	TXS
																		N	.	.	.	.	.	Z	.	TYA

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

\+ ADD
− SUBTRACT
∧ AND
V OR
⊻ EXCLUSIVE OR

M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
n NO. CYCLES
\# NO. BYTES

Ordering Information

1 MHz	2 MHz	3 MHz	4 MHz
UM6502	UM6502A	UM6502B	UM6502C
UM6507	–	–	–
UM6512	UM6512A	UM6512B	UM6512C

Part Number	Clocks	Pins	IRQ	NMI	RYD	Addressing
UM6502	On-Chip	40	√	√	√	64K
UM6507	On-Chip	28			√	8K
UM6512	External	40	√	√	√	64K